

In the Matter of

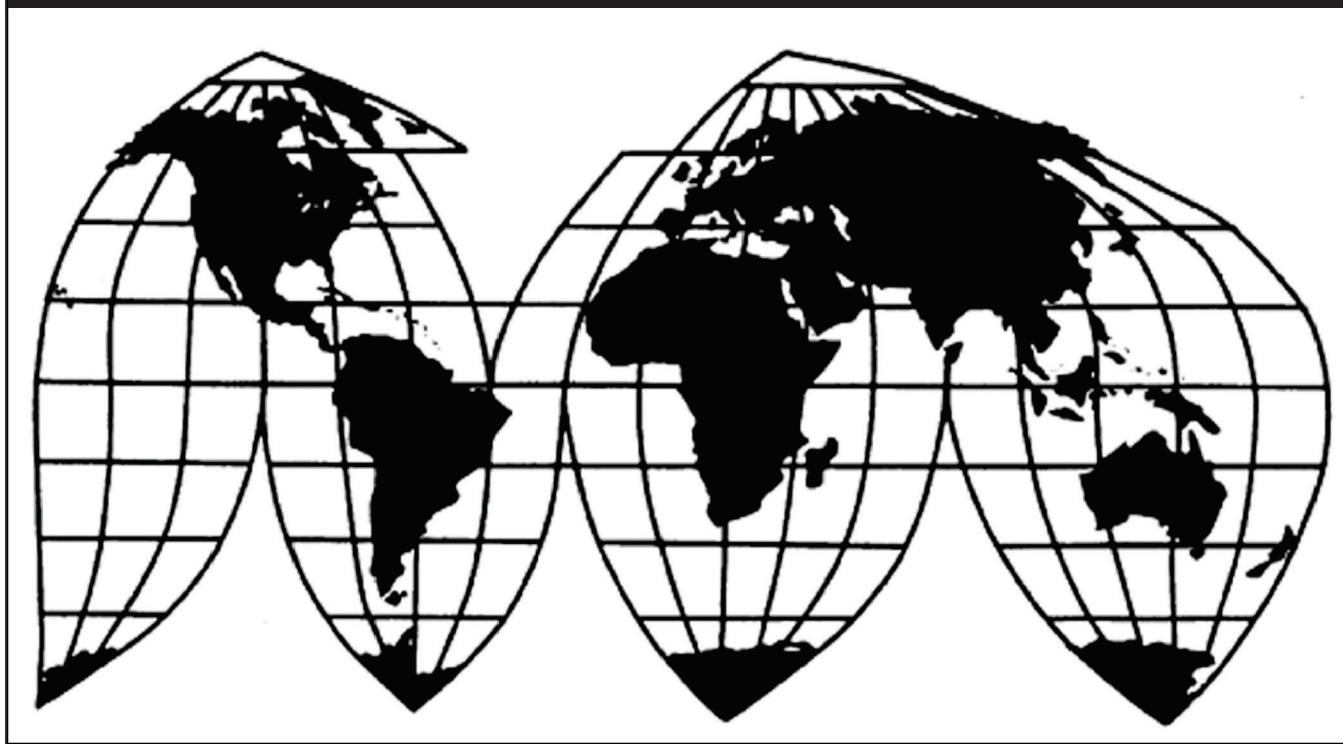
**CERTAIN MEMORY MODULES AND
COMPONENTS THEREOF, AND
PRODUCTS CONTAINING SAME**

Investigation No. 337-TA-1023

Publication 4935

September 2019

U.S. International Trade Commission



Washington, DC 20436

U.S. International Trade Commission

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Washington, DC 20436**

U.S. International Trade Commission

Washington, DC 20436
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In the Matter of

CERTAIN MEMORY MODULES AND COMPONENTS THEREOF, AND PRODUCTS CONTAINING SAME

Investigation No. 337-TA-1023



UNITED STATES INTERNATIONAL TRADE COMMISSION
Washington, D.C.

In the Matter of

CERTAIN MEMORY MODULES AND
COMPONENTS THEROF, AND
PRODUCTS CONTAINING SAME

Investigation No. 337-TA-1023

**NOTICE OF A COMMISSION DETERMINATION TO REVIEW-IN-PART AN INITIAL
DETERMINATION FINDING NO VIOLATION OF SECTION 337; ON REVIEW, TO
TAKE NO POSITION ON ONE ISSUE; AFFIRMANCE OF THE FINDING OF NO
VIOLATION AND TERMINATION OF THE INVESTIGATION**

AGENCY: U.S. International Trade Commission.

ACTION: Notice.

SUMMARY: Notice is hereby given that the U.S. International Trade Commission has determined to review-in-part a final initial determination ("ID") of the presiding administrative law judge ("ALJ") finding no violation of section 337. On review, the Commission has determined to take no position on the issue under review. The Commission has also determined to affirm the ID's finding of no violation of section 337 and has terminated the investigation.

FOR FURTHER INFORMATION CONTACT: Clint Gerdine, Esq., Office of the General Counsel, U.S. International Trade Commission, 500 E Street, SW., Washington, D.C. 20436, telephone (202) 708-2310. Copies of non-confidential documents filed in connection with this investigation are or will be available for inspection during official business hours (8:45 a.m. to 5:15 p.m.) in the Office of the Secretary, U.S. International Trade Commission, 500 E Street, SW., Washington, D.C. 20436, telephone (202) 205-2000. General information concerning the Commission may also be obtained by accessing its Internet server at <https://www.usitc.gov>. The public record for this investigation may be viewed on the Commission's electronic docket (EDIS) at <https://edis.usitc.gov>. Hearing-impaired persons are advised that information on this matter can be obtained by contacting the Commission's TDD terminal on (202) 205-1810.

SUPPLEMENTARY INFORMATION: The Commission instituted this investigation on October 7, 2016, based on a complaint filed on behalf of Netlist, Inc. of Irvine, California. 81 FR 69853-54. The complaint, as supplemented, alleged violations of section 337 of the Tariff Act of 1930, as amended, 19 U.S.C. 1337, by reason of infringement of certain claims of the following U.S. Patent Nos.: 8,756,364 ("the '364 patent"); 8,689,064; 8,516,185; 8,001,434 ("the '434 patent"); 8,359,501 ("the '501 patent"); and 8,489,837. The Commission's notice of investigation named SK Hynix Inc. of Gyeonggi-do, Republic of Korea; and SK Hynix America

Inc. and SK Hynix Memory Solutions Inc., both of San Jose, California, as respondents. The Office of Unfair Import Investigations (“OUII”) is also a party to the investigation. *Id.*

On May 31, 2017, the Commission issued notice of its determination not to review the ALJ’s ID (Order No. 21) terminating the investigation as to the ’364 patent based on partial withdrawal of the complaint.

On November 14, 2017, the ALJ issued his final ID and recommended determination (RD) on remedy and bonding in one document. The ID finds, *inter alia*, that none of respondents’ accused products infringe any of the remaining asserted patents. The ID also finds that claims 1-3 and 5-7 of the ’434 patent and claim 1 of the ’501 patent are not invalid as anticipated in view of U.S. Patent Publication No. 2005/0257109 A1 (“Averbuj”).

On November 27, 2017, complainant and respondents petitioned for review of the final ID. On December 5, 2017, complainant, respondents, and OUII each filed a response in opposition to the opposing petition for review. On December 5, 2017, the Chairman granted respondents’ motion for leave to refile its petition for review out of time.

Having examined the record of this investigation, including the ID, the parties’ petitions for review, and the responses thereto, the Commission has determined to review-in-part the final ID. Specifically, the Commission has determined to review the ID’s finding that claims 1-3 and 5-7 of the ’434 patent and claim 1 of the ’501 patent are not anticipated by Averbuj. The Commission has determined not to review the remainder of the final ID.

On review, the Commission determines to take no position on the ID’s finding that claims 1-3 and 5-7 of the ’434 patent and claim 1 of the ’501 patent are not invalid as anticipated in view of Averbuj. *See Beloit Corp. v. Valmet Oy*, 742 F.2d 1421 (Fed. Cir. 1984). The Commission therefore affirms the ID’s finding of no violation of section 337 and terminates the investigation.

The authority for the Commission’s determination is contained in section 337 of the Tariff Act of 1930, as amended, 19 U.S.C. 1337, and in part 210 of the Commission’s Rules of Practice and Procedure, 19 CFR part 210.

By order of the Commission.



Lisa R. Barton
Secretary to the Commission

Issued: January 16, 2018

PUBLIC CERTIFICATE OF SERVICE

I, Lisa R. Barton, hereby certify that the attached **NOTICE** has been served by hand upon the Commission Investigative Attorney, Vu Bui, Esq., and the following parties as indicated, on **January 16, 2018**.



Lisa R. Barton, Secretary
U.S. International Trade Commission
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Washington, DC 20436

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PUBLIC VERSION

UNITED STATES INTERNATIONAL TRADE COMMISSION

Washington, D.C.

In the Matter of

**CERTAIN MEMORY MODULES AND
COMPONENTS THEREOF, AND PRODUCTS
CONTAINING SAME**

INV. NO. 337-TA-1023

**INITIAL DETERMINATION ON VIOLATION OF SECTION 337 AND
RECOMMENDED DETERMINATION ON REMEDY AND BOND**

Chief Administrative Law Judge Charles E. Bullock

(November 14, 2017)

Appearances:

For the Complainants Netlist, Inc.:

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Aarti Shah, Esq., Andy Yu, Esq. of Mintz, Levin, Cohn, Ferris, Glovsky and Popeo PC of Washington, DC.

For the Respondents SK hynix Inc., SK hynix America Inc. and SK hynix memory solutions Inc.:

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For the Commission Investigative Staff:

Margaret D. Macdonald, Esq., Director; David O. Lloyd, Esq., Supervisory Attorney; Vu Q. Bui, Esq., Investigative Attorney of the Office of Unfair Import Investigations, U.S. International Trade Commission, of Washington, D.C.

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CDX	Complainant's demonstrative exhibit
CIB	Complainant's initial post-hearing brief
CPB	Complainant's pre-hearing brief
CPX	Complainant's physical exhibit
CRB	Complainant's reply post-hearing brief
CX	Complainant's exhibit
Dep.	Deposition
JX	Joint Exhibit
RDX	Respondent's demonstrative exhibit
RIB	Respondent's initial post-hearing brief
RPX	Respondent's physical exhibit
RPB	Respondent's Pre-hearing brief
RRB	Respondent's reply post-hearing brief
RRX	Respondent's rebuttal exhibit
RX	Respondent's exhibit
SIB	Staff's initial post-hearing brief
SRB	Staff's reply post-hearing brief
Tr.	Transcript

PUBLIC VERSION

UNITED STATES INTERNATIONAL TRADE COMMISSION

Washington, D.C.

In the Matter of

**CERTAIN MEMORY MODULES AND
COMPONENTS THEREOF, AND PRODUCTS
CONTAINING SAME**

INV. NO. 337-TA-1023

**INITIAL DETERMINATION ON VIOLATION OF SECTION 337 AND
RECOMMENDED DETERMINATION ON REMEDY AND BOND**

Chief Administrative Law Judge Charles E. Bullock

(November 14, 2017)

Pursuant to the Notice of Investigation, 81 *Fed. Reg.* 69853 (Oct. 7, 2016), this is the Initial Determination in the matter of *Certain Memory Modules and Components thereof, and Products Containing Same*, Investigation No. 337-TA-1023.

For the reasons stated herein, the undersigned has determined that no violation of section 337 of the Tariff Act of 1930, as amended, has occurred in the importation into the United States, the sale for importation, or the sale within the United States after importation of certain memory modules and components thereof, and products containing same with respect to U.S. Patents Nos. 8,001,434; 8,359,501; 8,689,064; 8,489,837; and 8,516,185.

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I. INTRODUCTION

A. Procedural History

On September 1, 2016, Complainant Netlist, Inc. (“Netlist” or “Complainant”) filed a Complaint alleging violations of section 337 based upon the sale for importation, importation, or sale within the United States after importation of certain memory modules and components thereof, and products containing same. *See* 81 *Fed. Reg.* 69853 (Oct. 7, 2016). On September 22 and 23, 2016, Netlist supplemented the complaint. *Id.*

On October 7, 2016, the Commission instituted this Investigation to determine:

whether there is a violation of subsection (a)(1)(B) of section 337 in the importation into the United States, the sale for importation, or the sale within the United States after importation of certain memory modules and components thereof, and products containing same by reason of infringement of one or more of claims 1-4, 6, 7, 10, 13, 17, and 23 of the '364 patent¹; claims 1-3, 7, 8, and 10-12 of the '185 patent; claims 2,3 and 5-7 of the '434 patent; claim 4 of the '501 patent; claim 16 of the '064 patent; and claims 1-3, 5, and 6 of the '837 patent, and whether an industry in the United States exists or is in the process of being established as required by subsection (a)(2) of section 337;

Id. at 69853-54.

The named respondents are SK Hynix Inc. of Gyeonggi-do, Republic of Korea; SK Hynix America, Inc. of San Jose, California; and SK Hynix memory solutions Inc. of San Jose, California (collectively, “SK hynix” or “Respondents”). (*Id.* at 69854.) The Commission Investigative Staff (“Staff”) is also a party to this Investigation. (*Id.*)

The evidentiary hearing was held May 8-11, 2017.

¹ On May 4, 2017, Netlist moved for partial termination of the investigation with respect to the '364 patent. (Mot. No. 1023-032.) The presiding ALJ at that time issued an Initial Determination granting that motion and terminating the investigation with respect to the '364 patent. Order No. 21 (May 5, 2017); *see also* Notice of Comm'n. Determination Not to Review an Initial Determination Terminating-in-Part the Investigation Based on Partial Withdrawal of the Compl. (May 31, 2017).

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B. The Parties

1. Complainant

Complainant Netlist, Inc. is a Delaware corporation with a principal place of business at 175 Technology Drive, Suite 150, Irvine, California. (Complaint at ¶7; CX-0001C at Q/A 49.) Netlist is in the business of designing, developing, manufacturing, and supporting high-performance memory modules. (CX-0001C at Q/A 51, 55.)

2. Respondents

a) SK hynix Inc.

SK hynix Inc. is a Korean corporation, having a principal place of business at 2091, Gyeonghung-daero, Bubal-eub, Icheon-si, Gyeonggi-do, Korea. (Resp. to Complaint at ¶30.) SK hynix Inc. is the parent corporation of Respondents SK hynix America Inc. and SK hynix memory solutions Inc. (*Id.*) SK hynix Inc. is a manufacturer and supplier of dynamic random-access memory (“DRAM”) chips and memory modules, including the accused DDR4 LRDIMM and RDIMM products in this investigation. (See RX-0002C at Q/A 7.)

b) SK hynix America Inc.

Respondent SK hynix America Inc. is a California corporation, having a principal place of business at 3101 North 1st Street, San Jose, California. (Resp. to Complaint at ¶31.) SK hynix America provides sales and technical support, and assists with customer relationships in the United States for SK hynix Inc. (*Id.*; RX-0001C at Q/A 45.)

c) SK hynix memory solutions Inc.

SK hynix memory solutions Inc. is a Delaware corporation, having a principal place of business at 3103 North 1st Street, San Jose, California. (Resp. to Complaint at ¶32.) SK hynix memory solutions Inc. is a wholly-owned subsidiary of SK hynix Inc. that performs research and

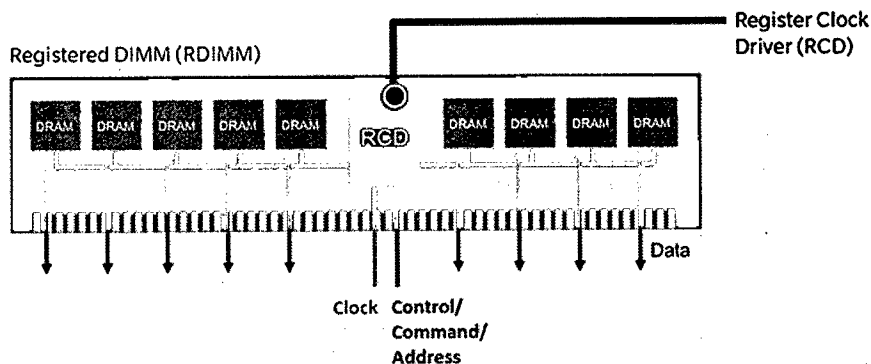
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development and provides customers with controller hardware and flash management systems and firmware for devices. (*Id.*; RX-0001C at Q/A 50.)

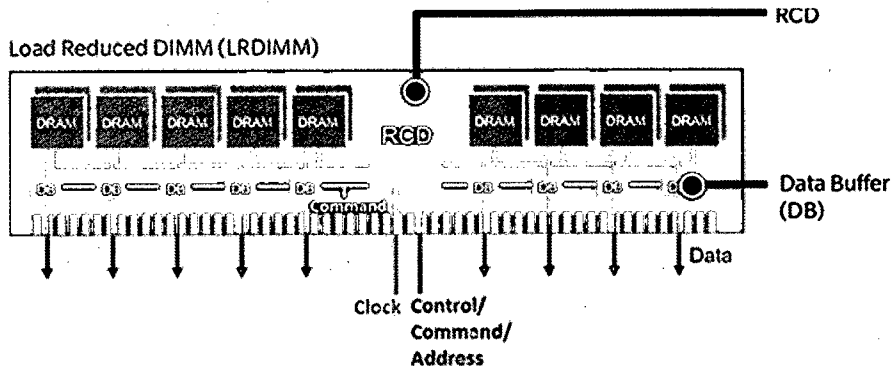
C. Overview of the Technology

The technology in this investigation relates to two types of memory modules: DDR4 Registered Dual In-Line Memory Modules (“RDIMMs”) and DDR4 Load-Reduced Dual In-Line Memory Modules (“LRDIMMs”). (Complaint at ¶35.) Both RDIMMs and LRDIMMs are designed for use in servers to store data that must be readily available for certain software applications, and to allow quick and efficient retrieval of that data. (RX-0004C at Q/A 204.) The DDR4 designation refers to the particular generation of the DRAM chips on the memory module. DDR4 is the most recent generation of these DRAM chips, preceded by DDR3, then DDR2, *etc.* (*Id.* at Q/A 201.)

RDIMMs and LRDIMMS share several similar components, including a printed circuit board, DRAM chips, and a Register/ing Clock Driver (“RCD”). (*See* CX-0840 at 3; CX-0005C at Q/A 69, 71.) LRDIMMS also contain Data Buffers (“DBs”) on the printed circuit board. (*See* CX-0840 at 3; CX-0005C at Q/A 71.) Complainants provide the following diagrammatic examples of an RDIMM and a LRDIMM, respectively:



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(CIB at 12-14.)

D. Asserted Patents

1. U.S. Patent No. 8,001,434 (the “434 patent”)

The ’434 patent is titled “Memory Board with Self-Testing Capability.” (JX-0003 (’434 Patent) at Cover.) It issued August 16, 2011 from a patent application filed April 13, 2009. (*Id.*) The patent lists Hyun Lee of Ladera Ranch, CA, Jayesh R. Bhakta of Cerritos, CA, and Soonju Choi of Irvine, CA as the inventors. (*Id.*) Netlist, Inc. of Irvine, CA is listed as the assignee. (*Id.*) The ’434 patent generally relates to self-testing memory modules. (*See id.* at Abstract.) Complainant asserts claims 2, 3, and 5-7 in this investigation.

The ’434 patent is one of three asserted patents that share a common specification. The parties refer to these three patents collectively as the “Self-Test Patents.” (*See* SIB at 11, n.3.)

2. U.S. Patent No. 8,359,501 (the “501 patent”)

The ’501 patent is also titled “Memory Board with Self-Testing Capability.” (JX-0004 (’501 Patent) at Cover.) It issued January 22, 2013 from a patent application filed July 14, 2011. (*Id.*) The patent lists Hyun Lee of Ladera Ranch, CA, Jayesh R. Bhakta of Cerritos, CA and Soonju Choi of Irvine, CA as the inventors. (*Id.*) Netlist, Inc. of Irvine, CA is listed as the

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assignee. (*Id.*) Like the '434 patent, the '501 patent generally relates to self-testing memory modules. (*See id.* at Abstract.) Complainant asserts claim 4 of the '501 patent in this investigation.

The '501 patent is the second of the “self-test patents” and it issued from a continuation application of the '434 patent, and shares a common specification with the '434 patent. (*See id.* at Cover.)

3. U.S. Patent No. 8,689,064 (the “'064 patent”)

The '064 patent is titled “Apparatus and Method for Self-Test in a Multi-Rank Memory Module.” (JX-0005 ('064 Patent) at Cover.) It issued on April 1, 2014 from a patent application filed January 19, 2013. (*Id.*) The patent lists Hyun Lee of Ladera Ranch, CA, Jayesh R. Bhakta of Cerritos, CA, and Soonju Choi of Irvine, CA as the inventors. (*Id.*) Netlist, Inc. of Irvine, CA is listed as the assignee. (*Id.*) Like the '434 and '501 patents, the '064 patent generally relates to self-testing memory modules. (*See id.* at Abstract.) Complainant asserts claim 16 of the '064 patent in this investigation.

The '064 patent is the third of the “self-test patents.” The '064 patent issued from a continuation application of the '501 patent, and shares a common specification with the '501 and '434 patents. (*See id.* at Cover.)

4. U.S. Patent No. 8,489,837 (the “'837 patent”)

The '837 patent is titled “Systems and Methods for Handshaking with a Memory Module.” (JX-0006 ('837 Patent)² at Cover.) It issued on July 16, 2013 from a patent application filed June 14, 2010. (*Id.*) The patent lists Hyun Lee of Ladera Ranch, CA as the inventor. (*Id.*) Netlist, Inc. of Irvine, CA is listed as the assignee. (*Id.*) The '837 patent generally relates to memory modules

² Staff indicates that the '837 patent has also been referred to as the “Handshake Patent” in this investigation. (SIB at 13, n.5.)

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that perform handshaking during or upon completion of initialization. (*Id.* at 1:15-17.) Complainant asserts claims 1-3, 5 and 6 of the '837 patent in this investigation.

5. U.S. Patent No. 8,516,185 (the "185 patent")

The '185 patent is titled "System and Method Utilizing Distributed Byte-Wise Buffers on a Memory Module." (JX-0002 ('185 Patent)³ at Cover.) It issued on August 20, 2013 from a patent application filed April 15, 2010. (*Id.*) The patent lists Hyun Lee of Ladera Ranch, CA and Jayesh R. Bhakta of Cerritos, CA as the inventors. (*Id.*) Netlist, Inc. of Irvine, CA is listed as the assignee. (*Id.*) The '185 patent generally relates to "memory subsystems of computer systems, and more specifically to systems, devices, and methods for improving the performance and the memory capacity of memory subsystems or memory 'boards,' particularly memory boards that include dual inline memory modules (DIMMs)." (*Id.* at 1:13-19.) Complainant asserts claims 1-3, 7, 8 and 10-12 of the '185 patent in this investigation.

II. JURISDICTION & IMPORTATION

A. Subject Matter Jurisdiction

Section 337 confers subject matter jurisdiction on the Commission to investigate, and if appropriate, to provide a remedy for, unfair acts and unfair methods of competition in the importation, the sale for importation, or the sale after importation of articles into the United States. *See* 19 U.S.C. §§ 1337(a)(1)(B) and (a)(2). Netlist filed a complaint alleging a violation of this subsection. Accordingly, the Commission has subject matter jurisdiction over this Investigation under section 337 of the Tariff Act of 1930. *See Amgen, Inc. v. U.S. Int'l. Trade Comm'n.*, 902 F.2d 1532, 1536 (Fed. Cir. 1990).

³ Staff indicates that the '185 patent has also been referred to as the "Load Reduction Patent" in this investigation. (SIB at 15 n.6.)

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B. Personal Jurisdiction

Respondents have appeared and participated in this Investigation. The Commission therefore has personal jurisdiction over Respondents. *See, e.g., Certain Optical Disk Controller Chips & Chipsets & Prods. Containing Same, Including DVD Players & PC Optical Storage Devices*, Inv. No. 337-TA-506, Initial Determination at 4-5 (May 16, 2005) (unreviewed in relevant part).

C. In Rem Jurisdiction

Respondents do not dispute that the Commission has *in rem* jurisdiction over the SK hynix accused products that have been imported into the United States. (RIB at 6.) In fact, Respondents admit that “SK hynix America Inc. imports the accused DDR4 LRDIMM and RDIMM memory modules into the United States.” (*Id.*) Accordingly, the Commission has *in rem* jurisdiction over the accused products.

D. Importation

As noted above, Respondents do not dispute that they import the accused RDIMM and LRDIMM memory modules. (*See* RIB at 6; Respondents’ Answer at Conf. Ex. A; CX-0218C at RFA No. 472-653.) Accordingly, the importation requirement of section 337 is satisfied.

E. Standing

Netlist asserts that it has standing to bring this investigation based on its rights and interest in the asserted patents. (CIB at 19 (citing JX-0013; JX-0014; JX-0015; JX-0016; JX-0017; JX-0018).) However, SK hynix argues that Netlist lacks standing because it has not satisfied the domestic industry requirement of section 337. (RIB at 6.) Staff submits that the assignment records for the asserted patents (*i.e.*, JX-0013; JX-0014; JX-0015; JX-0016; JX-0017; JX-0018) demonstrate that Netlist has standing, and argues that Respondents have improperly conflated standing with the domestic industry requirement. (SIB at 28.)

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SK hynix offers no precedent supporting its interpretation of the domestic industry requirement as a question of standing. Indeed, other than a single sentence in their initial post-hearing brief, Respondents never address the issue of standing again. (*Cf.* RIB at 6.) As Staff and Netlist both noted, the evidence of record shows that Netlist holds all of the rights and interests in the asserted patents in this investigation. (*See* JX-0013; JX-0014; JX-0015; JX-0016; JX-0017; JX-0018.) This showing is sufficient to establish Netlist's standing to bring this suit. Respondents have not presented argument or evidence that overcomes that showing. Accordingly, the undersigned finds that Netlist has standing in this investigation.

III. RELEVANT LAW

A. Claim Construction

“An infringement analysis entails two steps. The first step is determining the meaning and scope of the patent claims asserted to be infringed. The second step is comparing the properly construed claims to the device accused of infringing.” *Markman v. Westview Instruments, Inc.*, 52 F.3d 967, 976 (Fed. Cir. 1995) (*en banc*) (internal citations omitted), *aff'd*, 517 U.S. 370 (1996). Claim construction is a “matter of law exclusively for the court.” *Id.* at 970-71. “The construction of claims is simply a way of elaborating the normally terse claim language in order to understand and explain, but not to change, the scope of the claims.” *Embrex, Inc. v. Serv. Eng 'g Corp.*, 216 F.3d 1343, 1347 (Fed. Cir. 2000).

Claim construction focuses on the intrinsic evidence, which consists of the claims themselves, the specification, and the prosecution history. *See Phillips v. AWH Corp.*, 415 F.3d 1303, 1314 (Fed. Cir. 2005) (*en banc*); *see also Markman*, 52 F.3d at 979. As the United States Court of Appeals for the Federal Circuit (“Federal Circuit”) explained in *Phillips*, courts must analyze each of these components to determine the “ordinary and customary meaning of a claim

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term” as understood by a person of ordinary skill in the art at the time of the invention. 415 F.3d at 1313. “Such intrinsic evidence is the most significant source of the legally operative meaning of disputed claim language.” *Bell Atl. Network Servs., Inc. v. Covad Commc’ns Grp., Inc.*, 262 F.3d 1258, 1267 (Fed. Cir. 2001).

“It is a ‘bedrock principle’ of patent law that ‘the claims of a patent define the invention to which the patentee is entitled the right to exclude.’” *Phillips*, 415 F.3d at 1312 (quoting *Innova/Pure Water, Inc. v. Safari Water Filtration Sys., Inc.*, 381 F.3d 1111, 1115 (Fed. Cir. 2004)). “Quite apart from the written description and the prosecution history, the claims themselves provide substantial guidance as to the meaning of particular claims terms.” *Id.* at 1314; *see also Interactive Gift Express, Inc. v. CompuServe Inc.*, 256 F.3d 1323, 1331 (Fed. Cir. 2001) (“In construing claims, the analytical focus must begin and remain centered on the language of the claims themselves, for it is that language that the patentee chose to use to ‘particularly point[] out and distinctly claim[] the subject matter which the patentee regards as his invention.’”). The context in which a term is used in an asserted claim can be “highly instructive.” *Phillips*, 415 F.3d at 1314. Additionally, other claims in the same patent, asserted or unasserted, may also provide guidance as to the meaning of a claim term. *Id.*

The specification “is always highly relevant to the claim construction analysis. Usually, it is dispositive; it is the single best guide to the meaning of a disputed term.” *Id.* at 1315 (quoting *Vitronics Corp. v. Conceptoronic, Inc.*, 90 F.3d 1576, 1582 (Fed. Cir. 1996)). “[T]he specification may reveal a special definition given to a claim term by the patentee that differs from the meaning it would otherwise possess. In such cases, the inventor’s lexicography governs.” *Id.* at 1316. “In other cases, the specification may reveal an intentional disclaimer, or disavowal, of claim scope by the inventor.” *Id.* As a general rule, however, the particular examples or embodiments discussed

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in the specification are not to be read into the claims as limitations. *Id.* at 1323. In the end, “[t]he construction that stays true to the claim language and most naturally aligns with the patent’s description of the invention will be . . . the correct construction.” *Id.* at 1316 (quoting *Renishaw PLC v. Marposs Societa’ per Azioni*, 158 F.3d 1243, 1250 (Fed. Cir. 1998)).

In addition to the claims and the specification, the prosecution history should be examined, if in evidence. *Id.* at 1317; *see also Liebel-Flarsheim Co. v. Medrad Inc.*, 358 F.3d 898, 913 (Fed. Cir. 2004). The prosecution history can “often inform the meaning of the claim language by demonstrating how the inventor understood the invention and whether the inventor limited the invention in the course of prosecution, making the claim scope narrower than it would otherwise be.” *Phillips*, 415 F.3d at 1317; *see also Chimie v. PPG Indus. Inc.*, 402 F.3d 1371, 1384 (Fed. Cir. 2005) (“The purpose of consulting the prosecution history in construing a claim is to ‘exclude any interpretation that was disclaimed during prosecution.’”).

When the intrinsic evidence does not establish the meaning of a claim, then extrinsic evidence (*i.e.*, all evidence external to the patent and the prosecution history, including dictionaries, inventor testimony, expert testimony, and learned treatises) may be considered. *Phillips*, 415 F.3d at 1317. Extrinsic evidence is generally viewed as less reliable than the patent itself and its prosecution history in determining how to define claim terms. *Id.* at 1317. “The court may receive extrinsic evidence to educate itself about the invention and the relevant technology, but the court may not use extrinsic evidence to arrive at a claim construction that is clearly at odds with the construction mandated by the intrinsic evidence.” *Elkay Mfg. Co. v. Ebco Mfg. Co.*, 192 F.3d 973, 977 (Fed. Cir. 1999).

If, after a review of the intrinsic and extrinsic evidence, a claim term remains ambiguous, the claim should be construed so as to maintain its validity. *Phillips*, 415 F.3d at 1327. Claims,

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however, cannot be judicially rewritten in order to fulfill the axiom of preserving their validity. *See Rhine v. Casio, Inc.*, 183 F.3d 1342, 1345 (Fed. Cir. 1999). Thus, “if the only claim construction that is consistent with the claim’s language and the written description renders the claim invalid, then the axiom does not apply and the claim is simply invalid.” *Id.*

B. Infringement

In a section 337 investigation, the complainant bears the burden of proving infringement of the asserted patent claims by a preponderance of the evidence. *See Spansion, Inc. v. Int’l Trade Comm’n*, 629 F.3d 1331, 1349 (Fed. Cir. 2010). This standard “requires proving that infringement was more likely than not to have occurred.” *Warner-Lambert Co. v. Teva Pharm. USA, Inc.*, 418 F.3d 1326, 1341 n.15 (Fed. Cir. 2005).

1. Literal Infringement

Literal infringement is a question of fact. *See Finisar Corp. v. DirecTV Grp., Inc.*, 523 F.3d 1323, 1332 (Fed. Cir. 2008). Literal infringement requires the patentee to prove that the accused device contains each limitation of the asserted claim(s). If any claim limitation is absent, there is no literal infringement of that claim as a matter of law. *See Bayer AG v. Elan Pharm. Research Corp.*, 212 F.3d 1241, 1247 (Fed. Cir. 2000).

C. Validity

A patent is presumed valid. 35 U.S.C. § 282; *Microsoft Corp. v. i4i Ltd. P’ship*, 131 S. Ct. 2238, 2242 (2011). A respondent who has raised patent invalidity as an affirmative defense has the burden of overcoming this presumption by clear and convincing evidence. *See Microsoft*, 131 S. Ct. at 2242. As with an infringement analysis, an analysis of invalidity involves two steps: determining the scope of the claim and comparing the properly construed claim with the prior art to determine whether the claimed invention is anticipated and/or rendered obvious.

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1. Anticipation (35 U.S.C. § 102)

Under 35 U.S.C. § 102, a claim is anticipated and therefore invalid when “the four comers of a single, prior art document describe every element of the claimed invention, either expressly or inherently, such that a person of ordinary skill in the art could practice the invention without undue experimentation.” *Advanced Display Sys., Inc. v. Kent State Univ.*, 212 F.3d 1272, 1282 (Fed. Cir. 2000), *cert. denied*, 532 U.S. 904 (2001). To be considered anticipatory, the prior art reference must be enabling and describe the applicant’s claimed invention sufficiently to have placed it in possession of a person of ordinary skill in the field of the invention. *Helifix Ltd. v. Blok-Lok, Ltd.*, 208 F.3d 1339, 1346 (Fed. Cir. 2000).

2. Obviousness (35 U.S.C. § 103)

Under 35 U.S.C. §103, a patent may be found invalid as obvious if “the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains.” 35 U.S.C. §103(a). Because obviousness is determined at the time of invention, rather than the date of application or litigation, “[t]he great challenge of the obviousness judgment is proceeding without any hint of hindsight.” *Star Scientific, Inc. v. R.J. Reynolds Tobacco Co.*, 655 F.3d 1364, 1375 (Fed. Cir. 2011) (“*Star IP*”).

When a patent is challenged as obvious, the critical inquiry in determining the differences between the claimed invention and the prior art is whether there is an apparent reason to combine the known elements in the fashion claimed by the patent at issue. *See KSR Int’l Co. v. Teleflex, Inc.*, 550 U.S. 398, 417-418 (2007). The Federal Circuit has since held that when a patent is challenged as obvious, based on a combination of several prior art references, “the burden falls on the patent challenger to show by clear and convincing evidence that a person of ordinary skill in the art would

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have had reason to attempt to make the composition or device, or carry out the claimed process, and would have had a reasonable expectation of success in doing so.” *PharmaStem Therapeutics, Inc. v. ViaCell, Inc.*, 491 F.3d 1342, 1360 (Fed. Cir. 2007) (citations omitted).

Obviousness is a determination of law based on underlying determinations of fact. *Star II*, 655 F.3d at 1374. The factual determinations behind a finding of obviousness include: (1) the scope and content of the prior art, (2) the level and content of the prior art, (3) the differences between the claimed invention and the prior art, and (4) secondary considerations of non-obviousness. *KSR*, 550 U.S. at 399 (citing *Graham v. John Deere Co.*, 383 U.S. 1, 17 (1966)). These factual determinations are referred to collectively as the “*Graham* factors.” Secondary considerations of non-obviousness include commercial success, long felt but unresolved need, and the failure of others. *Id.* When present, secondary considerations “give light to the circumstances surrounding the origin of the subject matter sought to be patented,” but they are not dispositive on the issue of obviousness. *Geo. M. Martin Co. v. Alliance Mach. Sys. Int’l.*, 618 F.3d 1294, 1304-06 (Fed. Cir. 2010). A court must consider all of the evidence from the *Graham* factors before reaching a decision on obviousness. For evidence of secondary considerations to be given substantial weight in the obviousness determination, its proponent must establish a nexus between the evidence and the merits of the claimed invention. *See W. Union Co. v. MoneyGram Payment Sys. Inc.*, 626 F.3d 1361, 1372-73 (Fed. Cir. 2010) (citing *In re GPAC Inc.*, 57 F.3d 1573, 1580 (Fed. Cir. 1995)).

3. Written Description (35 U.S.C. § 112, (a)/(1))

The hallmark of the written description requirement is the disclosure of the invention. *See Ariad Pharm., Inc. v. Eli Lilly and Co.*, 598 F.3d 1336, 1351 (Fed. Cir. 2010) (*en banc*). The test for determining the sufficiency of the written description in a patent requires “an objective inquiry

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into the four corners of the specification from the perspective of a person of ordinary skill in the art. Based on that inquiry, the specification must describe an invention understandable to that skilled artisan and show that the inventor actually invented the invention claimed.” *Id.* Compliance with the written description requirement is a question of fact and “the level of detail required to satisfy the written description requirement varies depending on the nature and scope of the claims and on the complexity and predictability of the relevant technology.” *Id.*

4. Enablement (35 U.S.C. § 112, (a)/¶1)

To satisfy the enablement requirement a patent specification must “contain a written description of the invention . . . to enable any person skilled in the art . . . to make and use the same.” 35 U.S.C. §112, ¶1. The specification must enable a person of ordinary skill in the art to practice the claimed invention without undue experimentation. *Transocean Offshore Deepwater Drilling, Inc. v. Maersk Contractors USA, Inc.*, 617 F.3d 1296, 1305 (Fed. Cir. 2010). Although a specification need not disclose minor details that are well known in the art, this is “merely a rule of supplementation, not a substitute for a basic enabling disclosure.” *Auto. Tech. Int ’l Inc., v. BMW of N. Am.*, 501 F.3d 1274, 1283 (Fed. Cir. 2007) (quoting *Genentech, Inc. v. Novo Nordisk, A/S*, 108 F.3d 1361, 1366 (Fed. Cir. 1997)). “It is the specification, not the knowledge of one skilled in the art, that must supply the novel aspects of an invention in order to constitute adequate enablement.” *Auto. Tech.*, 501 F.3d at 1283.

Enablement is a question of law with underlying questions of fact regarding undue experimentation. *Transocean*, 617 F.3d at 1305. The factors weighed by a court in determining whether a disclosure requires undue experimentation include: (1) the quantity of experimentation necessary, (2) the amount of direction provided, (3) the presence of working examples, (4) the nature of the invention, (5) the state of the prior art, (6) the relative skill of those in the art, (7)

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the predictability of the art, and (8) the breadth of the claims. *In re Wands*, 858 F.2d 731, 737 (Fed. Cir. 1988). Undue experimentation is “a matter of degree” and “not merely quantitative, since a considerable amount of experimentation is permissible, if it is merely routine, or if the specification in question provides a reasonable amount of guidance with respect to the direction in which the experimentation should proceed.” *PPG Indus., Inc. v. Guardian Indus. Corp.*, 75 F.3d 1558, 1564 (Fed. Cir. 1996); *Northpoint Tech, Ltd. v. MDS Am, Inc.*, 413 F.3d 1301, 1318 (Fed. Cir. 2005).

5. Indefiniteness (35 U.S.C. § 112, (b)/¶2)

A claim must also be definite. Pursuant to 35 U.S.C. § 112(b): “The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the inventor or joint inventor regards as the invention.” 35 U.S.C. § 112(b). In *Nautilus, Inc. v. Biosig Instruments, Inc.*, 134 S. Ct. 2120 (2014), the Supreme Court held that § 112(b) requires “that a patent's claims, viewed in light of the specification and prosecution history inform those skilled in the art about the scope of the invention with reasonable certainty.” *Id.* at 2129. A patent claim that is indefinite is invalid. 35 U.S.C. § 282(b)(3)(A).

D. Domestic Industry

In a patent-based complaint, a violation of section 337 can be found “only if an industry in the United States, relating to the articles protected by the patent . . . concerned, exists or is in the process of being established.” 19 U.S.C. § 1337(a)(2). Under Commission precedent, this “domestic industry requirement” of section 337 consists of an economic prong and a technical prong. *See Certain Stringed Musical Instruments and Components Thereof*, Inv. No. 337-TA-586, Comm’n. Op. at 12-14, 2009 WL 5134139 (U.S.I.T.C. Dec. 2009). The complainant bears the burden of establishing that the domestic industry requirement is satisfied. *See Certain Set-*

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Top Boxes and Components Thereof, Inv. No. 337-TA-454, Final Initial Determination at 294, 2002 WL 31556392 (U.S.I.T.C. June 21, 2002) (unreviewed by Commission in relevant part).

1. Economic Prong

Section 337(a)(3) sets forth the following economic criteria for determining the existence of a domestic industry in such investigations:

(3) For purposes of paragraph (2), an industry in the United States shall be considered to exist if there is in the United States, with respect to the articles protected by the patent, copyright, trademark, mask work, or design concerned –

- (A) significant investment in plant and equipment;
- (B) significant employment of labor or capital; or
- (C) substantial investment in its exploitation, including engineering, research and development, or licensing.

Given that these criteria are listed in the disjunctive, satisfaction of any one of them will be sufficient to meet the economic prong of the domestic industry requirement. *See Certain Integrated Circuit Chipsets and Prods. Containing Same*, Inv. No. 337-TA-428, Order No. 10, Initial Determination (unreviewed) (May 4, 2000).

2. Technical Prong

The technical prong of the domestic industry requirement is satisfied when the complainant in a patent-based section 337 investigation establishes that it is practicing or exploiting the patents at issue. *See* 19 U.S.C. § 1337(a)(2) and (3); *Certain Microsphere Adhesives, Process for Making Same and Prods. Containing Same, Including Self-Stick Repositionable Notes*, Inv. No. 337-TA-366, Comm'n Op. at 8, 1996 WL 1056095 (U.S.I.T.C. Jan. 16, 1996). “The test for satisfying the ‘technical prong’ of the industry requirement is essentially [the] same as that for infringement, i.e., a comparison of domestic products to the asserted claims.” *Alloc, Inc. v. Int’l Trade Comm’n*, 342 F.3d 1361, 1375 (Fed. Cir. 2003). To prevail, the patentee must establish by a preponderance of

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the evidence that the domestic product practices one or more claims of the patent, either literally or under the doctrine of equivalents. *See Bayer*, 212 F.3d at 1247. It is sufficient to show that the products practice any claim of that patent, not necessarily an asserted claim of that patent. *See Certain Microsphere Adhesives*, Comm'n Op. at 7-16.

IV. U.S. PATENT NO. 8,001,434

A. Overview

1. Asserted Claims

Complainants assert claims 2, 3 and 5-7 of the '434 patent. Each of the asserted claims depends from independent claim 1. Those claims provide as follows:

1. A self-testing memory module, comprising:

a printed circuit board configured to be operatively coupled to a memory controller of a computer system;

a plurality of memory devices on the printed circuit board, each memory device of the plurality of memory devices comprising data, address, and control ports; and

a circuit comprising:

a control module configured to generate address and control signals for testing the memory devices; and

a data module comprising a plurality of data handlers, each data handler operable independently from each of the other data handlers of the plurality of data handlers and operatively coupled to a corresponding plurality of the data ports of one or more of the memory devices and configured to generate data for writing to the corresponding plurality of data ports, wherein the circuit is configured to test the memory devices using the address and control signals generated by the control module and the data generated by the plurality of data handlers.

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2. The self-testing memory module of claim 1, wherein the plurality of data handlers comprise at least two physically separate components mounted on the printed circuit board.

* * * * *

3. The self-testing memory module of claim 2, wherein the plurality of data handlers comprise at least two physically separate integrated circuit packages.

* * * * *

5. The self-testing memory module of claim 2, wherein each of the plurality of data handlers is positioned on the printed circuit board proximate to the corresponding plurality of data ports.

* * * * *

6. The self-testing memory module of claim 5, wherein each of the plurality of data handlers is positioned closer to the corresponding plurality of data ports than to the other data ports of the plurality of memory devices.

* * * * *

7. The self-testing memory module of claim 6, wherein each of the data handlers is further configured to read from the corresponding plurality of data ports and further comprises a verification element for checking for failures in the operation of the memory devices by verifying that data read from the corresponding plurality of data ports corresponds to the data generated by the data handler for writing to the corresponding plurality of data ports.

(JX-0003 at Cls. 1-3, 5-7.)

B. Level of Ordinary Skill in the Art

The parties and Staff agree that a person of ordinary skill in the art would have “a Bachelor’s degree in electrical engineering, computer engineering, or in a related field and at least one year of work experience relating to memory systems, and would be familiar with the design of memory devices, memory modules, and built-in-self test or BIST.” (SIB at 30 (quoting

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CPB at 87; RPB at 54).) The evidence of record further supports this definition of the level of ordinary skill in the art. (See CX-0005C at Q/A 96; CX-0931C at Q/A 101; RX-0008C at Q/A 30.) Accordingly, the undersigned finds that the level of ordinary skill in the art for the '434 patent is consistent with the definition proposed by the parties and Staff.

C. Claim Construction

There are four disputed claim terms relevant to the asserted claims of the '434 patent:

- 1. "self-testing memory module"
- 2. "generate"
- 3. "test"
- 4. "wherein the circuit is configured to test the memory devices"

Each is addressed in turn below.

1. "self-testing memory module"

The term "self-testing memory module" appears in independent claim 1, from which each of the asserted claims from the '434 patent depend. The parties propose the following constructions for this term:

<i>"self-testing memory module"</i>		
Complainant's Proposed Construction	Respondents' Proposed Construction	Staff's Proposed Construction
No construction proposed No construction necessary	memory module that is able to test one or more elements of the memory module without the use of an external device	plain and ordinary meaning, e.g., memory module that is able to test one or more elements of the memory module (either without the use of an external device or with the use of both an internal device and an external device)

(SIB at 32; see also CIB at 23-24; RIB at 58.)

Complainant frames the dispute regarding this term as whether an external device can be used for any portion of the memory module self-test. (See CIB at 24.) Complainant's position is

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that the term should not be construed to exclude the use of an external device during self-testing.

See id. In support of its position, Complainant points to the following portion of the specification:

Some embodiments described herein presents [*sic*] a self-testing memory module that can be configured through an I2C interface and that allows test results to be read out through the I2C interface. Certain embodiments described herein present a self-testing memory module that allows a test function to be configured, controlled, and/or executed without substantial system memory controller involvement. Some embodiments present a self-testing memory module that can be tested without any external test equipment.

(*Id.* (citing '434 patent at 3:46-54 (all emphases added)).) Complainant reads this passage to demonstrate that the '434 patent contemplates self-testing memory modules that interface with external devices. (*See id.* at 24-25.)

Complainant also points to a decision by the Patent Trial and Appeal Board (“PTAB” or “Board”) of the U.S. Patent and Trademark Office, wherein the Board construed “self-testing memory module” to include memory modules that can be tested with a combination of internal and external test equipment. (*See id.* at 25 (citing IPR 2014-00970, Final Written Decision (Paper 32) at 14 (emphasis added)).) Complainant also relies on the testimony of its expert to support its construction. (*See* Mangione-Smith, Tr. at 426:2-20.)

By contrast, Respondents submit that this term should be construed to exclude the use of any external devices in the self-test. (*See* RIB at 58.) To support that position, Respondents point to the language of independent claim 1—the word “self” particularly—and argue that the claim language excludes the use of an external device. (*See id.*) Respondents also argue that independent claim 1 and unasserted independent claim 29 both describe testing procedures that “internally generate[] the requisite address and control signals and the requisite data for executing the test without an external device providing such signals.” (*Id.*) Additionally, Respondents note that one of the stated purposes of the '434 patent is to obviate the expense associated with external testing of memory modules. (*See* JX-0003 at 1:58-2:5.)

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Respondents also argue that an amendment made during the prosecution of the '434 patent supports construing “self-testing memory module” to exclude the use of an external device during testing. (*See* RIB at 58-59.) Specifically, Respondents submit that the examiner rejected the original claim 1 because it lacked any limitation related to self-testing. (*See id.*) That rejection was overcome by an amendment that added the limitation “wherein the circuit is configured to test the memory devices using the address and control signals *generated* by the control module and the data *generated* by the plurality of data handlers.” (*See id.* at 59 (quoting JX-0009 at 151) (emphasis added).) Respondents interpret this portion of the prosecution history as a concession by the patentee “that ‘self-testing’ means testing using signals generated by circuits internal to the memory module and not signals provided by an external device.” (*Id.*)

Finally, Respondents argue that Complainant is estopped from advancing its current claim construction argument because it argued for a narrower construction before the PTAB. (*See id.*)

Staff joins Complainant and argues that “self-testing memory module” should be construed according to its plain and ordinary meaning. Acknowledging that simply stating “plain and ordinary meaning” does not clearly resolve the dispute between the parties, Staff includes a parenthetical example with its proposed construction that explicitly states that the memory module may perform its self-test function “either without the use of an external device or with the use of both an internal device and an external device.” (SIB at 32.) Staff argues that its construction is supported by the plain language of the claims, (*id.* at 33-36), and the specification, (*id.* at 36-40). Staff also argues that the prosecution history does not support construing “self-testing memory modules” to exclude any use of an external device. (*Id.* at 40-41.)

The undersigned agrees with the construction put forth by Complainant and Staff. Contrary to Respondents’ position, the claim term “self” does not provide a sufficient basis to

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exclude the use of any external device during self-testing by a “self-testing memory module.” This conclusion is particularly clear here, where the specification explicitly contemplates self-testing memory modules that make use of an external device. (See JX-0003 at 3:49-56.) Further, in its post-hearing reply brief, Respondents appear to concede that the proper construction of “self-testing memory module” should include configurations utilizing some external devices.⁴ (RRB at 31 (“SK hynix’s construction . . . allows some use of external equipment, such as configuring the memory module for testing and initiating the test but not actually executing the test . . .”).)

Accordingly, “self-testing memory modules” is construed to mean *“memory module that is able to test one or more elements of the memory module (either without the use of an external device or with the use of both an internal device and an external device).”*

2. “generate”

The claim term “generate” appears in independent claim 1, from which each of the asserted claims from the ’434 patent depend. The parties propose the following constructions for this term:

“generate”		
Complainant’s Proposed Construction	Respondents’ Proposed Construction	Staff’s Proposed Construction
produce or cause	produce (<i>i.e.</i> , bring into existence)	produce (<i>i.e.</i> , bring into existence, including by transformation or modification of information and/or data received from another component)

⁴ Respondents submit that their construction allows use of external devices that perform “insubstantial” or “peripheral” functions related to testing. (See RRB at 31.) That interpretation is not supported by the actual language of Respondents’ construction, nor was it raised in Respondents’ initial brief. As such, the undersigned will not consider this belated modification to Respondents’ proposed construction. Moreover, the undersigned notes that injecting the terms “insubstantial” and “peripheral” into the construction of “self-testing memory modules” would only add more uncertainty into the claim language.

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(SIB at 43; *see also* CIB at 19-20; RIB at 49.)

Here, Complainant notes that all parties agree that “generate” should mean “produce,” but that they disagree about whether that meaning includes transformation or modification of information and/or data received from another component. (*See* CIB at 20.) Complainant takes the position that transformation or modification of information and/or data received from another component is included within the proper construction of “generate.” (*See id.*)

First, Complainant points to the language of independent claim 1, which ties the “generate” function to the data handlers within the claimed data module. (*See id.* at 20–21 (citing JX-0003 at 16:43-47).) Next, Complainant points to the specification for the proposition that data generated by the data handlers is created from information provided by the data module to the data handlers. (*See id.* at 21 (citing JX-0003 at 10:30-37).) Also, Complainant submits that “[t]he specification also explicitly contemplates the act of transforming or modifying incoming data as generating data within the meaning of the claim term” (*Id.* (citing JX-0003 at 10:33-37).)

In addition to its reliance on the intrinsic evidence, Complainant also relies on expert testimony to support its construction. (*See id.*) Specifically, Complainant submits that Mr. Hoffman, one of Respondents’ experts, testified that “generate” includes transformation of data. (*Id.* (citing Hoffman, Tr. 844:8-20)). Further, Complainant submits that its expert, Dr. Mangione-Smith, and Respondents’ expert, Mr. Hoffman, agreed that Staff’s proposed construction is consistent with the plain and ordinary meaning of “generate.” (*See id.* at 21-22 (citing Mangione-Smith, Tr. at 427:2-18; Hoffman, Tr. at 834:9-18).)

Respondents also argue that Staff’s proposed construction is correct. (*See* RIB at 49-50.) However, Respondents elaborate on that construction by arguing that Staff’s construction includes data generated by the memory modules through transformation or modification of information

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received from another source, but does not include “signals and data received by the data and control modules from another component, and merely provided, propagated, sent, input to memory devices, without transformation or modification the data and control modules.” (*Id.* at 50 (quoting SPB at 49).) In short, Respondents’ position is that while transformation or modification of external data is allowed, simple receipt of external data without any modification or transformation does not fall within the scope of the term “generate.” (*See id.*) Respondents also take issue with the inclusion of the word “cause” in Complainant’s proposed construction. (*See id.* at 50.)

Respondents argue that “the claims and specification distinguish between ‘generate’ and merely providing, writing, or inputting (*i.e.*, causing) data produced by a component other than the data handler.” (*Id.* at 51 (citing RX-0348.028-32).) In support of that argument, Respondents point to the claims including both the words “generate” and “writing” as well as “generate” and “provide.” (*Id.* (citing ’434 patent at 16:42-48, JX-0004 at 16:42-46, JX-0005 at 18:16-20).) Respondents submit that the use of the words “writing” and “provide” in the same claim as “generate” means that “generate” cannot have the same meaning as those words. (*Id.* (citing *Z4 Tech., Inc. v. Microsoft Corp.*, 507 F.3d 1340, 1348 (Fed. Cir. 2007).)

Respondents also point to an example in the specification to support the proposition that “data generation involves an actual production of data.” (*Id.*) Specifically, Respondents point to a passage stating that “data may be generated *based on previously written data* (e.g., *inverting each of the bits* of a previously written data word) in some embodiments.” (*Id.* (citing JX-0003 at 10:57-60 (emphasis added by Respondents)).)

Respondents submit that construing “generate” to include “cause” would obviate one of the purposes of the patent—avoiding the use of expensive external memory testing equipment. (*See id.* at 52 (citing ’434 patent at 1:58-2:5).) They also point to examples in the specification

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where the memory module itself, as opposed to another testing device, actually produces the test data. (*Id.* (citing '434 patent at 3:28-41, Figs. 3, 5).)

Respondents argue that Complainant's own validity expert, Mr. Murphy, testified that simply using data provided without transforming it or modifying it would not meet the definition of "generate" to a person of ordinary skill in the art. (*Id.*) Somewhat confusingly though, Respondents support this assertion with a portion of their own expert's witness statement. (*See id.* (citing RX-1586C at Q/A 230, 232).)

A significant portion of Respondents' argument against construing "generate" to mean "cause" is based on the assertion that Complainant has taken a contradictory position before a district court in a parallel proceeding and before the PTAB in an *Inter Partes* Review ("IPR"). (*See id.* at 52-53.) With respect to the Complainant's position in the IPR, Respondents argue that *Aylus Networks, Inc. v. Apple, Inc.*, 856 F.3d 1353 (Fed. Cir. 2017) establishes that statements made by a patentee during an IPR are part of the prosecution history for that patent, and thus can effect an estoppel. (*See* RIB at 53.) Because Complainant did not argue for a construction for "generate" that included "cause" during the IPR, but instead argued that "generate" should be construed to mean "produce (*i.e.*, brought into existence)," Respondents submit that Complainant cannot argue for a construction of "generate" that encompasses "cause" in this Investigation. (*See id.*) Respondents go on to note that the PTAB construed "produce" to mean "originate," and not "merely providing, propagating, or sending the same information and/or data received from another component." (*See id.* (citing RX-0347 at 014).) Based on Complainant's statements during the IPR, Respondents argue that Complainant has disclaimed any construction of "generate" that includes "cause." (*See id.* at 53-54.)

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Finally, Respondents submit that, prosecution disclaimer aside, Complainant has simply failed to provide any evidence supporting a construction of “generate” to mean “cause.” (*See id.* at 54-55.)

Staff submits that the dispute between Complainant and Respondents over the construction of “generate” is one of form over substance. (SIB at 43.) Staff submits that despite providing different formulations of the construction for “generate,” both parties have in fact agreed in substance with Staff’s construction of “generate,” which is based on PTAB’s construction of “generate” in the IPR. (*Id.*) However, regardless of whether the parties agree with its construction, Staff submits that its construction is consistent with the intrinsic evidence, and thus should be adopted. (*Id.* at 45.)

First, Staff finds support for its construction in the language of the claims themselves. (*See id.* (citing JX-0003 at 16:42-48, 19:6-9).) Second, Staff points to Figure 3 of the specification, which discloses a “data generation element,” to support its construction. (*See id.* at 45-46 (citing JX-0003 at Fig. 3, 10:27-37).) Third, Staff finds support for its construction in the IPR proceedings where the PTAB explained that its construction of “generate” would include the transformation or modification of information or data from another component, but would not include simple receipt of information or data by the data and control modules from another component without any kind of transformation or modification. (*See id.* at 46-47.)

With respect to extrinsic evidence, Staff points to the testimony of the parties’ experts to further support its construction. Specifically, Staff submits that:

- i) Respondents’ expert, Mr. William Hoffman, testified that the Staff’s proposed construction is consistent with the understanding of one of ordinary skill in the art of the ’434 Patent who has reviewed the patent claims, specification, and prosecution history; and
- (ii) Complainant’s expert, Dr. William Mangione-Smith, also testified that the Staff’s proposed construction is consistent with the understanding of a person of ordinary skill in the art of the ’434 Patent.

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(*Id.* at 47 (citing Hoffman, Tr., 842:21-843:5; Mangione-Smith, Tr., 426:22-427:11).) Finally, addressing Respondents' prosecution disclaimer argument, Staff submits that the argument may provide an additional basis to reject a construction of "generate" that would encompass merely receiving or using data provided by another component. (*See id.* at 48.)

There appears to be a great amount of internal inconsistency in each party's arguments concerning the claim term "generate." Complainant, Respondents, and Staff all appear to agree that "generate" should be construed to mean: "produce (*i.e.*, bring into existence, including by transformation or modification of information and/or data received from another component)." (*See* CRB at 2, n.1; RRB at 24-25; SRB at 10.) Yet, Complainant insists that Respondents and Staff seek a narrower construction that would limit the transformation or modification to a specific method: bit inversion. (*See* CRB at 3-4.) Respondents further insist that Complainant seeks a broad construction by the inclusion of the word "cause" in its proposed construction. (*See* RRB at 24-25.) In short, each party insists that they agree with Staff's proposed construction, while insisting that the other side does not. In such a situation, the undersigned will take each party at its own word, *i.e.*, that a person of ordinary skill in the art would understand the plain and ordinary meaning of "generate" in the context of the '434 patent to mean "produce (*i.e.*, bring into existence, including by transformation or modification of information and/or data received from another component)."

This construction is supported by the intrinsic evidence as well as extrinsic evidence in the form of expert testing at the evidentiary hearing. Specifically, "generate" appears in independent claim 1 of the '434 patent as follows:

a control module configured to *generate* address and control signals for testing the memory devices; and a data module comprising a plurality of data handlers, each data handler operable independently from each of the other data handlers of the plurality of data handlers and operatively coupled to a corresponding plurality of the

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data ports of one or more of the memory devices and configured to *generate* data for writing to the corresponding plurality of data ports, wherein the circuit is configured to test the memory devices using the address and control signals *generated* by the control module and the data *generated* by the plurality of data handlers.

(JX-0003 at Cl. 1 (emphasis added).) Construing “generate” to mean “produce” or “bring into existence” is consistent with the manner in which “generate” is used in this claim. Construing “generate” to mean “cause,” however, is not. Construing “generate” to mean “cause” would produce nonsensical results, such as “a control module configured to [cause] address and control signals,” and a “plurality of data handlers . . . configured to [cause] data for writing to the corresponding plurality of data ports.” (*Cf. id.* (alterations substituting “cause” for “generate”).) Moreover, no part of the claim language suggests that production by transformation or modification should be excluded from the definition of “generate.”

Further, Figure 3 of the '434 patent discloses a data generation element numbered 54 in the figure. The specification provides the following discussion of that element:

Each of the data handlers 30 of certain embodiments further includes a data handler logic element 46. The data handler logic element 46 of certain embodiments comprises a data generation element 54 and a verification element 56. The data generation element 54 may be configured to generate data signals (e.g., patterns of data signals) for writing to the corresponding plurality of data ports, for example. The data signals and/or patterns of data signals may be based on information (e.g., programming or configuration information) the data handler logic element 46 receives from the control module 22, for example.

* * *

The data may be generated in a variety of ways. In one embodiment, the data is generated based on a current write address value. For example, in one example configuration, on a first write cycle, hexadecimal "A's" are generated and written to even address locations and hexadecimal "S's" are generated and written to odd address locations, and on a second write cycle, "S's" are written to even addresses and "A's" are written to odd addresses, and this pattern repeats in subsequent cycles. The data may be generated based previously written data (e.g., inverting each of the bits of a previously written data word) in 60 some embodiments. In general, any manner of generating a cyclic or otherwise deterministic data pattern may be compatible with embodiments described herein. In other embodiments, random or pseudorandom data may be generated and written to the corresponding

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plurality of data ports. For 65 example, a linear feedback shift register (LFSR) may be used in some embodiments.

(JX-0003 at 10:27-37, 10:49-66.) The specification’s explanation of the data generation element in Figure 3 supports the conclusion that “generate” should not be limited to the production of data and information out of nothing, but rather should include production by the transformation and modification of previously written data as well. Accordingly, construing “generate” to mean “produce (i.e., bring into existence, including by transformation or modification of information and/or data received from another component)” is supported by the intrinsic evidence. As Staff noted, this construction is also supported by testimony of the parties’ experts. (See Hoffman, Tr., 842:21-843:5; Mangione-Smith, Tr., 426:22-427:11.) Therefore, the undersigned finds that “generate” should be construed to mean *“produce (i.e., bring into existence, including by transformation or modification of information and/or data received from another component).”*

3. “Test”

The claim term “test” appears in independent claim 1, from which each of the asserted claims from the ’434 patent depend. The parties propose the following constructions for this term:

“test”		
Complainant’s Proposed Construction	Respondents’ Proposed Construction	Staff’s Proposed Construction
plain and ordinary meaning (e.g., check for failures, defects, correct memory access speed)	check for bit failures or defects	plain and ordinary meaning, e.g., check for failures or defects

(SIB at 49; see also CIB at 23; RIB at 55.)

The parties’ dispute here centers around whether the term “test” should be limited to checking for bit failures or defects in a memory module, or instead if checking for bit failures or defects is but one example of a “test” as that term is used in the ’434 patent. Complainants

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advocate the broader construction, and point to a portion of the specification that discusses various tests, which include checking for bit failures, as well as checking for correct memory access speed, among other examples. (CIB at 23 (citing '434 patent at 1:36-52).) Respondents advocate the narrower construction, and argue that “[a]ll of the embodiments describe testing whether memory cells stored data without defects or failures.” (RIB at 56.) Respondents dispute that “test” includes checking for correct memory access speed on the basis that “not a single embodiment evaluates the memory chips’ access speed.” (*Id.*) Respondents’ position is also based on the assertion that the “test” must be construed as limited to testing memory, and not other components. (*See id.* at 57.) Finally, Respondents complain that Complainant has advanced inconsistent claim construction positions for this term between this investigation and a parallel district court investigation.

For its part, Staff appears to advocate the same construction as Complainant, albeit while making it explicit that checking for bit failures is one example of the plain and ordinary meaning of “test.” (*See* SIB at 49.) In support of its position, Staff notes that Respondents have improperly attempted to read limitations from other claim terms into the term “test,” which would render other terms in the claim superfluous. (*Id.* at 50.) Pointing to the same portion of the specification as Complainant, Staff also argues that the '434 patent’s disclosure includes tests beyond just checking for bit failures. (*Id.* at 51.) Finally, Staff dismisses any inconsistency among the positions offered by Complainant’s expert in the district court proceeding and this investigation on the basis that “test” can be suitably construed by reference to the intrinsic evidence, effectively rendering extrinsic expert testimony on the meaning of “test” irrelevant. (*Id.* at 52-53.)

The undersigned agrees with Staff and Complainant that it would be improper to limit the term “test” to only checking for bit failures or defects in memory modules. The language of

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independent claim 1 itself does not support limiting the term “test” to a single, or even several, types of tests, such as checking memory for bit failures or defects. The same is true of limiting the term “test” to tests carried out on memory modules. As Staff correctly points out, other language of independent claim 1 defines the structure on which the test should be carried out. Accordingly, construing “test” to include a limitation on the type of structure being tested would render other portions of independent claim 1 superfluous; such a construction is disfavored.

Further, the specification uses “test” more broadly than the construction Respondents propose. As cited by both Complainant and Staff, the specification of the ’434 patent provides:

There are typically at least three test phases which memories undergo during system manufacture. Each phase generally **tests for memory defects and for the correct operation of the input/output interface**. The first test phase is typically conducted by the memory chip manufacturer and generally involves **checking for bit failures, correct memory access speed, etc.** The second test phase is typically done by memory module manufacturers and generally involves **testing the signal quality, the noise susceptibility, and the operational speed of the memory module as a single unit**. The second test phase may also include **checking for bit failures in individual memory chips**. The third phase is usually carried out by the system manufacturer. During the third phase, **the interaction of the memory subsystem with other components in the system is tested**. During the third phase, the **individual memory module operation is also tested again and the memory array is checked for defects**.

(JX-0003 at 1:36-52 (emphasis added).) This passage of the specification reinforces the conclusion that checking for bit failures or defects is but one example of a test; it is not the sole example, however.

Finally, with respect to Respondents’ argument that embodiments only use “test” in relation to checking for bit failures or defects, the undersigned believes that argument misses the mark in the context of claim construction. Particularly, Respondents have pointed to no rule that dictates the constriction of a term’s plain and ordinary meaning in accordance with the exemplary embodiments of the accompanying specification—nor could they. *See Innogenetics,*

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N.V. v. Abbott Labs., 512 F.3d 1363, 1370 (Fed. Cir. 2008) (“Abbott contends that the written description constricts the claim limitation to a method of contemporaneous detection because the described embodiments all feature detection of an actual complex. However, as is well established, an applicant is not required to describe in the specification every conceivable and possible future embodiment of his invention.”); *CCS Fitness, Inc. v. Brunswick Corp.*, 288 F.3d 1359, 1366 (Fed. Cir. 2002) (“our case law makes clear that a patentee need not ‘describe in the specification every conceivable and possible future embodiment of his invention.’”).

Accordingly, the undersigned finds that “test” should be given its *plain and ordinary meaning, which includes, but is not limited to, checking memory for bit failures or defects.*

4. “wherein the circuit is configured to test the memory devices”

The claim term “wherein the circuit is configured to test the memory devices” appears in independent claim 1, from which each of the asserted claims from the ’434 patent depend. The parties propose the following constructions for this term:

<i>“wherein the circuit is configured to test the memory devices”</i>		
Complainants’ Proposed Construction	Respondents’ Proposed Construction	Staff’s Proposed Construction
No construction proposed No construction necessary	wherein the circuit is configured to check for bit failures or defects in the memory devices without the use of an external device	plain and ordinary meaning, <i>e.g.</i> , wherein the circuit is configured to check for failures or defects in the memory devices

(SIB at 53; *see also* CIB at 25-26; RIB at 55.)

Complainant and Staff address this term separately from the term “test.” However, both concede that any dispute over this term is coextensive with the dispute over the term “test.” (SIB at 53-54; CIB at 25-26.) Respondents do not address this term separately, and instead include it in their discussion of “test.” (*See* RIB at 55.) Accordingly, there is no unique dispute with

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respect to this term. Thus, in light of the undersigned's finding that "test" should be given its plain and ordinary meaning, as explained *supra*, the undersigned finds that this term should also be given its *plain and ordinary meaning, which is not confined to a particular type of test, such as checking for bit failures.*

D. Infringement

1. Claim 1

a) *Element 1: "A self-testing memory module"*

The primary dispute regarding this element revolves around the construction of "self-testing memory module," which has been construed, *supra*. Complainant submits that, under the construction proposed by the Staff, which it adopts, the accused LRDIMM products implement a DB-to-DRAM Write Delay Training Mode, which is a self-testing function. (CIB at 28-29.) Respondents counter that the training mode upon which Complainant relies is directed by an external device, and thus does not qualify as "self-testing." (RRB at 42.) Staff submits that the evidence shows that the accused LRDIMM products satisfy this limitation, and that Respondents' opposition is based on an improper construction of "self-testing memory module." (SIB at 55.)

As explained in more detail, *supra*, "self-testing memory module" means "memory module that is able to test one or more elements of the memory module (either without the use of an external device or with the use of both an internal device and an external device)." Under this construction, the accused LRDIMM products practice the "A self-testing memory module" limitation by virtue of the Write Delay Training Mode function. (See CX-0005C at Q/A 360-382.)

b) *Element 2: "a printed circuit board configured to be operatively coupled to a memory controller of a computer system"*

Complainant points to a variety of evidence in support of its assertion that the accused LRDIMM products include "a printed circuit board configured to be operatively coupled to a

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memory controller of a computer system.” (See CIB at 30-31 (citing CX-0005C at Q/A 389-405, CX-0890.00017, CX-0288.66-67, CX-0283C at 152:6-154:15, 154:18-155:10 (Hyunjoong Kim Dep.) and CX-0326C at 30:2-31:15, 101:5-12 (Roland Knaack Dep.)) Respondents do not disagree that the accused products include printed circuit boards as required by this element, but instead argue that Complainant adopted a construction for this term that limited the element to only a *single* printed circuit board. (RIB at 77.) Respondents then assert that, because the accused products include a plurality of printed circuit boards, they do not meet this claim limitation. (*Id.*) Staff agrees with Complainant that this element is present in the accused LRDIMM products, and points to similar evidence in support of its position. (SIB at 55-56.) Staff further submits that Respondents’ opposition is based on a misinterpretation of Complainant’s invalidity contentions. (*Id.* at 56.)

The undersigned finds that the accused LRDIMM products satisfy the limitation of this element of claim 1. As Complainant and Staff point out, this finding is supported by the evidence of record. (See CX-0005C at Q/A 383-405; Hoffman, Tr. at 820:3-10.) Further, Respondents admit that “each accused product includes multiple ‘printed circuit boards.’” (RRB at 43.) Respondents’ argument that this element is missing from its products because the claim limitation should be construed to require *only* a single printed circuit board is rejected. Neither the specification nor the language of the claims supports such a construction. To the contrary, the use of “comprising” in claim 1 indicates an open ended interpretation is appropriate, wherein the claim is not restricted to only the elements listed. See *Stiftung v. Renishaw PLC*, 945 F.2d 1173, 1178 (Fed. Cir. 1991) (“claim 2, which uses the term ‘comprising,’ is an ‘open’ claim which will read on devices which add additional elements”). Accordingly, the undersigned finds that the accused LRDIMM products practice the “a printed circuit board configured to be operatively

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coupled to a memory controller of a computer system” limitation of claim 1. (See CX-0005C at Q/A 383-405; Hoffman, Tr. at 820:3-10.)

c) Element 3: “a plurality of memory devices on the printed circuit board, each memory device of the plurality of memory devices comprising data, address, and control ports”

Complainant contends that the accused LRDIMM products include “a plurality of memory devices on the printed circuit board, each memory device of the plurality of memory devices comprising data, address, and control ports.” (CIB at 32 (citing CX-0378 at 65; CX-0438 at 3; CX-0382 at 5-7; CX-0383 at 5-9; Hoffman, Tr. at 820:3-6; CX-0005C at Q/A 406-29).) Respondents do not dispute the presence of this element in the accused LRDIMM products. Staff also contends that the accused LRDIMM products satisfy this element. (See SIB at 56-57.)

Based on the evidence presented by Complainants and relied on by Staff, the undersigned finds that the accused LRDIMM products practice this element of independent claim 1. (See CX-0005C at Q/A 406-429; Hoffman, Tr. at 820:3-6; CX-0378 at 65; CX-0438 at 3; CX-0382 at 5-7; CX-0383 at 5-9.)

d) Element 4: “a circuit comprising a control module configured to generate address and control signals for testing the memory devices”

Complainants contend that the accused LRDIMM products include “a circuit comprising a control module configured to generate address and control signals for testing the memory devices,” and cite to various evidence of record in support of that contention. (CIB at 32-33 (citing CX-0288 at 24, 60-61, 63, 64, and 84; CX-0005C at Q/A 430-482).) Respondents do not dispute the presence of this element in the accused LRDIMM products. Staff also contends that the accused LRDIMM products satisfy this element. (See SIB at 57.)

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Based on the evidence presented by Complainants and relied on by Staff, the undersigned finds that the accused LRDIMM products practice this element of independent claim 1. (See CX-0005C at Q/A 431-482; CX-0288 at 24, 60-61, 63, 64, and 84.)

e) Element 5: “a data module comprising a plurality of data handlers, each data handler operable independently from each of the other data handlers of the plurality of data handlers and operatively coupled to a corresponding plurality of the data ports of one or more of the memory devices and configured to generate data for writing to the corresponding plurality of data ports”

The parties dispute whether the accused LRDIMM products satisfy this element. Specifically, their dispute revolves around whether the data handlers “generate” data, or instead merely pass along data generated by the memory controller. This dispute is tied closely to the construction of the term “generate” which is discussed at length, *supra*.

Complainant submits that this element is present in the accused products because the data buffer (“DB”) receives 28 bits of data from the Register Clock Driver (“RCD”), but only outputs 8 bits of data to the corresponding data ports. (See CIB at 34-37.) Complainant describes the process by which the data buffers receive the 28 bits of information and output 8 bits of information as a transformation, and thus concludes that the “generate” limitation is met by the accused products. (*Id.* at 37.)

Respondents counter that the 8 bits of training data that are ultimately output from the DBs originate from the memory controller. (RIB at 61.) Respondents submit that the 8 training bits are then transferred by the RCD to the DBs in the same form that the RCD received the bits from the memory controller. (*Id.*) Respondents then submit that the exact same 8 bits are written from the DB to the DRAM. (*Id.*) Respondents conclude that this translation of the same 8 bits from one component to another is not a form of modification or transformation, and does not satisfy the “generate” limitation of this claim element.

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With respect to the other 20 bits of information raised in Complainant's argument, Respondents argue that the 8 training bits that are actually used for testing are transferred in seven 4-bit packets by the RCD to the DB. (RIB at 65.) Respondents argue that the other 20 bits in the packet serve merely to ensure that the 8 training bits are written to the DRAM, and are irrelevant for the purposes of this limitation because they are never written to the memory. (*Id.*) Respondents also submit that unpacking the 28 bit packet is merely processing, which does not meet the proper definition of "generate." (*Id.* at 66.)

Staff's position substantially aligns with that of Respondents. Particularly, Staff submits that the "generate" limitation is not satisfied because the DBs of the accused LRDIMM products do not produce data, but instead merely move data from the memory controller to the DRAMs. (SIB at 58.) While acknowledging the fact that the 8 bits of training data are sent through a 4 bit wide BCOM bus over 7 clock cycles—thus producing 28 bits of data—and in the form of packets, (*see id.* at 64), Staff nonetheless asserts that it is the memory controller, not the DB, that generates the data that is written to the DRAMs. (*Id.* 66.) Accordingly, Staff concludes that the accused LRDIMM products do not satisfy this element of independent claim 1.

In response to Respondents' and Staff's arguments, Complainant alleges that both have improperly applied a definition of "generate" that requires inversion of at least one data bit. (CRB at 13.) Complainant also accuses Respondents and Staff of ignoring the operations performed by the DB. (*Id.*) Complainant goes on to reiterate its position that the 8 training bits are transformed or modified by virtue of being split up into 7 packets of 4 bits during the process of being sent from the RCD to the DB, and then transformed or modified again when the packets are unpacked and the training bits are sent to the DRAMs. (*See id.* at 15-17.)

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First, the undersigned notes that there is no dispute about the actual physical operation of the accused products with respect to this element of independent claim 1. While the parties provide demonstrative exhibits that differ in some respects, those differences are the result of variations in the level of detail provided. (*Compare* CDX-300 at 22-26 *with* RDX 1586C at 150-171.) They do not result from contradictory views of how the accused products operate. Particularly, with respect to the process by which the RCD sends training bits to the DBs, Complainant's demonstrative exhibit makes it explicit that the bits are broken into 4-bit packets, and not sent as a single 8-bit stream. (*See* CDX-300 at 22-26.) Neither Staff nor Respondents dispute this point, *i.e.*, that the training bits are transferred in 4-bit packets. At the same time, there is no dispute that the training bits provided to the DRAMs are identical to the training bits that were provided by the memory controller to the RCD. (Mangione-Smith, Tr. at 448:18-453:8; 455:14-456:22 RX-1586C at 304-306.) Accordingly, the operative dispute is whether the operations attendant to packing and unpacking the training bits during the course of transferring them from the memory controller to the DRAMs satisfy the "generate" limitation of this element. The undersigned finds that they do not.

The evidence of record shows that the training bits are not generated, produced, or brought into existence by the data buffer. (RX-1586C at Q/A 304-319; Mangione-Smith, Tr. at 448:18-453:8, 455:14-456:22.) To the contrary, those bits of data are generated upstream of the data buffer. (RX-1586C at Q/A 308-309; Mangione-Smith, Tr. at 448:18-24.) The fact that the bits are transferred to the DB in packets before being reassembled to be transferred to the DRAMs does not mean the DB generated those bits. (*See* Mangione-Smith, Tr. at 463:22-464:14.) Complainant's argument to the contrary is based on an over-expansive interpretation of the term "generate." Particularly, Complainant's arguments revolve almost entirely around whether a transformation or modification of data in the DB occurred. Transformation or

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modification, however, appears in the parties' (and the undersigned's) construction of this term as merely an example of how data may be "produced," or "brought into existence." (*See* CIB at 20; RIB at 51; SIB at 45-47.) No party, including Complainant, proposed construing "generate" to mean simply "transform or modify." And for good reason: to construe "generate" as equivalent to any transformation or modification of data would expand the term beyond its plain and ordinary meaning without any indication in the intrinsic or extrinsic evidence that such an expansion was intended, or even contemplated by the patentee.

Nonetheless, Complainant now attempts to jettison the requirement that data be "produced" or "brought into existence" in favor of a broader requirement that data need only be transformed or modified to meet the "generate" limitation. Implicit in Complainant's argument is the idea that "produce," "bring into existence," "transform," and "modify" are interchangeable, or at least that "transformation" and "modification" are specific examples wholly contained within the scope of "produce" and "bring into existence." If true, then logically it would be sufficient to show a transformation or modification of data to show the production of data, and thus the generation of data.

However, the undersigned finds no evidence that a person of ordinary skill in the art would, in the context of the intrinsic evidence, understand "transform or modify" to be coextensive with "produce" or "bring into existence." To the contrary, in scenarios such as this one, where the only "transformation" of data is a by-product of transferring that data, there is no element of production or bringing into existence. Moreover, to the extent the proper construction of "generate" explicitly references transformation or modification, the purpose was to make clear that generation does not necessarily require data to be conjured completely from a vacuum and absent of any other input.

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As explained *supra*, the proper construction of “generate” is “produce (*i.e.*, bring into existence, including by transformation or modification of information and/or data received from another component).” The training bits that are ultimately provided to the DRAMs are not produced or brought into existence by the DB, but rather are brought into existence by the memory controller. (RX-1586C at Q/A 308-309; Mangione-Smith, Tr. at 448:18-24.) While the DB unpacks those training bits from the 4-bit packets sent by RCD, (*see* RX-1586C at Q/A 342), thus arguably transforming the 4-bit packets, that unpacking operation in no way brought those training bits into existence; they were brought into existence before they ever reached the DB. To find otherwise would expand the meaning of “generate” well-beyond its plain and ordinary meaning and the adopted construction.

Accordingly, the undersigned finds that the accused LRDIMM products do not meet the limitations of element 5 of independent claim 1.

f) Element 6: “wherein the circuit is configured to test the memory devices using the address and control signals generated by the control module and the data generated by the plurality of data handlers”

Complainant points to a series of questions from its expert’s witness statement to establish that the accused LRDIMM products practice this element of claim 1. (CIB at 39 (citing CX-0005C at Q/A Nos. 533-557).) Acknowledging that the disputes regarding this element mirror the disputes regarding the “generate” limitation just discussed, as well as the construction of “self-testing memory modules,” Complainant relies on those portions of its brief for this element as well. (*Id.* (citing CIB at §§ III.A.3, III.B.1.e).) Respondents also do not address this element separately, but instead group their arguments together based on the “generate” limitation and the “test” limitation. (*See* RIB at §§ IV.D.1, IV.D.2.). Similarly, Staff addresses this

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element by focusing on the “data generated by the plurality of data handlers,” and relying on its arguments with respect to element 5 of independent claim 1. (SIB at 70.)

The undersigned generally agrees with the parties that this element rises and falls with at least element 5, based on the fact that this element presupposes that data has been generated by the plurality of data handlers. As discussed in the prior section, the data handlers in the accused LRDIMM products do not generate data. Accordingly, the undersigned finds that the accused LRDIMM products do not practice the limitations of element 6 of claim 1.

Given that every limitation of an asserted must be present in an accused device to establish infringement, the undersigned also finds that the accused LRDIMM products do not infringe independent claim 1 of the '434 patent.

2. Asserted Dependent Claims 2, 3 and 5-7

Claims 2, 3 and 5-7 all depend from independent claim 1. Because dependent claims incorporate all of the limitations of the claim from which they depend, dependent claims 2, 3 and 5-7 include all of the limitations of unasserted independent claim 1. Accordingly, the undersigned finds that the accused LRDIMM products do not infringe dependent claims 2, 3 and 5-7 for at least the same reasons they do not infringe independent claim 1, *i.e.*, they do not practice the “generate data” limitations.

E. Domestic Industry – Technical Prong

Complainant claims satisfaction of the technical prong of the domestic industry requirement based on two of its products: 1) the HyperCloud Products; and 2) the HybriDIMM Products. (CIB at 40.)

With respect to the HyperCloud product, Complainant submits that the products practice each limitation of claims 1, 2, and 3 of the '434 patent. (*See id.* at 41-42.) Neither Staff, nor

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Respondents dispute that assertion. (See RIB at 77-78; RRB at 44; SIB at 75-76.) Upon reviewing the evidence presented by Complainant, the undersigned finds that the HyperCloud products practice claims 1-3 of the '434 patent, and thus satisfy the technical prong of the domestic industry requirement. (CX-0005C at Q/A 987-1135; *see also* RX-1586C at Q/A 422-423.)

With respect to the HybriDIMM products, Complainant asserts that “[e]ach of the Netlist HybriDIMM Products practice the Asserted Claims of the '434 patent.” (CIB at 42.) Complainant submits that its HybriDIMM products function in the same way as the accused LRDIMM products, and thus practice the asserted claims of the '434 patent for the same reasons articulated by Complainant with respect to infringement. (*Id.*) Respondents and Staff agree that the HybriDIMM products function in the same manner as the accused LRDIMM products, and that if the accused LRDIMM products are found not to infringe the asserted claims of the '434 patent, then so too must the HybriDIMM products be found not to practice the asserted claims of the '434 patent. (RIB at 77-78; SIB at 78-79.)

Upon reviewing the evidence presented by the parties, the undersigned agrees that the record supports the conclusion that the HybriDIMM products function identically to the accused LRDIMM products for the purposes analyzing infringement and domestic industry with respect to the asserted claims of the '434 patent. (See CX-0005C at Q/A 647-662; RX-1586C at Q/A 340, 431-436). Accordingly, the undersigned finds that the HybriDIMM products do not practice the asserted claims of the '434 patent for the same reasons that the accused LRDIMM products do not infringe the asserted claims of the '434 patent. *See supra* at § IV.D. Therefore, the HybriDIMM products do not satisfy the technical prong of the domestic industry requirement.

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Based on the foregoing reasoning, the undersigned finds that Complainant has satisfied the technical prong of the domestic industry requirement for the '434 patent based on its HyperCloud products.

F. Validity

Respondents assert two grounds for invalidity with respect to the '434 patent. First, Respondents contend that each of the asserted claims of the '434 patent is invalid under 35 U.S.C. § 102 as anticipated. (RIB at 78-102.) Second Respondents assert that each of the asserted claims of the '434 patent is invalid under 35 U.S.C. § 112, second paragraph, because the term “generate,” if construed to mean “produce or cause,” is indefinite. (*Id.* at 102-103.)

1. Expert Testimony of Mr. Hoffman

Prior to addressing Respondents' anticipation and indefiniteness arguments specifically, the undersigned finds it necessary to address an issue raised by both Complainant and Staff with respect to the testimony of Respondents' expert witness, Mr. William Hoffman. Complainant and Staff assert that Mr. Hoffman's opinions on invalidity are unreliable because he did not have an understanding of the correct standard of proof applicable to invalidity challenges. Particularly, during his deposition, Mr. Hoffman indicated that he applied a “preponderance of the evidence” standard in forming his opinions on invalidity. (Hoffman, Tr. at 825:2-10.) Then, during the evidentiary hearing, Mr. Hoffman testified that he was still unsure that he fully understood the applicable, clear and convincing, standard of proof. (*Id.* at 828:13-18.) Given Mr. Hoffman's failure to identify the correct standard of proof as clear and convincing, and his failure to articulate a description of that standard, Complainant and Staff conclude that Mr. Hoffman's testimony is unreliable, and should be given little weight, if any. (CIB at 42-43; SIB at 79-80.) From there, Complainant and Staff conclude that, without Mr. Hoffman's testimony,

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Respondents lack any evidence to support their invalidity case. (CIB at 42-43; SIB at 80.)

Neither of these conclusions follows.

First, the undersigned finds that Mr. Hoffman has not been offered as, and does not purport to be, an expert in patent law. (See RX-0008C at Q/A 18-24.) Rather, Mr. Hoffman's expertise is in electrical engineering, including the development and operation of memory and microprocessor chips. (*Id.*) To the extent Mr. Hoffman's testimony is helpful, it will be because it leverages his specialized knowledge and technical expertise to explain and illuminate technically intensive questions of fact. These questions may include how the accused products operate, or what a person of ordinary skill in the art would understand a certain prior art reference to disclose.

Moreover, neither Complainant nor Staff explains why Mr. Hoffman's failure to comprehend the distinctions between various evidentiary standards of proof would render unreliable his opinions on technical questions of fact.⁵ Undoubtedly, Mr. Hoffman's failure to fully comprehend the clear and convincing standard of proof prevents him from reliably determining whether Respondents have met that standard. However, that determination is reserved for the undersigned. See *Iplearn, LLC v. Blackboard Inc.*, No. CV 11-876 (RGA), 2014 WL 4967122, at *2 (D. Del. Oct. 2, 2014) ("Clear and convincing evidence and the presumption of validity are not standards required of expert opinion on invalidity, but standards used by a factfinder. These are legal concepts that are for jury determinations, not for expert witnesses.") As explained previously in this investigation, "[a]n expert's dalliance into legal opinions beyond his expertise does not . . . automatically discredit his other opinions of factual matters underlying

⁵ *Icon Health & Fitness, Inc. v. Strava, Inc.*, 849 F.3d 1034, 1046 (Fed. Cir. 2017), which is the sole case cited by Complainant and Staff in support of the proposition that Respondents cannot make out an invalidity case without Mr. Hoffman's testimony, misses the mark here. The cited portion of that case criticized a PTAB decision for merely summarizing and then rejecting a party's arguments without making any factual findings or offering any explanation as to why those arguments failed. (See *id.*) The Federal Circuit was not asked, and did not decide, whether an invalidity argument must necessarily fail in the absence of expert testimony. (*Cf. id.*)

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those legal determinations.” (Order 19 at 4-5.) Here, to the extent Mr. Hoffman’s testimony strays into legal opinions and determinations, the undersigned has given that testimony no weight.⁶ The undersigned does not agree, however, that Mr. Hoffman’s testimony on technical questions of fact should be diminished based on his limited knowledge of evidentiary standards of proof. *See Zenith Elecs. Corp. v. PDI Commc’n Sys., Inc.*, 522 F.3d 1348, 1357 n.3 (Fed. Cir. 2008); *Formax, Inc. v. Alkar-Rapidpak-MP Equip., Inc.*, No. 11-C-298, 2014 WL 3057116, at *3 (E.D. Wis. July 7, 2014) (“The fact that an engineer does not know the burden of proof or the difference between anticipation and obviousness—something ninety-five percent of attorneys would not be able to explain—is not a reason to disqualify him.”)

2. Anticipation

a) *U.S. Patent Publication No. 2005/0257109 A1 (“Averbuj”)*

Respondents submit that *Averbuj*, which is titled “Built-In Self-Test (BIST) Architecture Having Distributed Interpretation and Generalized Command Protocol,” is prior art to the ’434 patent, and anticipates claims 1-3 and 5-7. (RIB at 78-84.) Respondents note that *Averbuj* was published on November 17, 2005, and contend that the reference “addresses an efficient built in self-test architecture for testing memory devices of an electronic device.” (*Id.* at 78; RX-0354 (“*Averbuj*”) at Title, (43).)

(1) Claim 1 – “[a] self-testing memory module, comprising: a printed circuit board configured to be operatively coupled to a memory controller of a computer system”

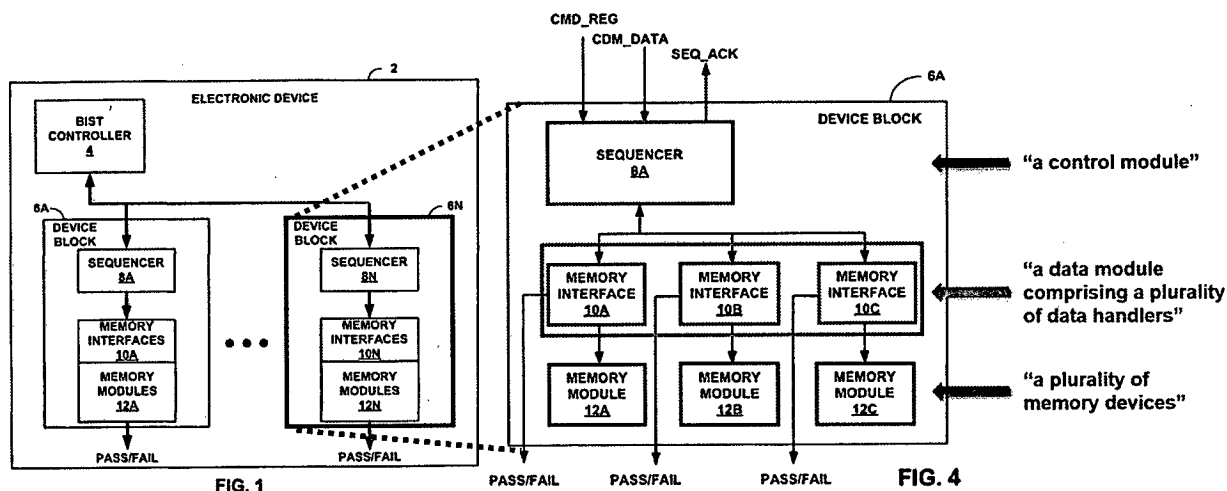
Respondents map the disclosure of *Averbuj* onto the elements of claim 1 as follows:

⁶ The undersigned has taken the same position with respect to all of the technical experts presented in this case. Their testimony is only helpful to the extent it is confined to questions of fact within their area of expertise. The application of facts to a given legal standard is a question of law on which a technical expert’s testimony is not helpful.

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(i) the device block (6) corresponds to the claim term “self-testing memory module”; (ii) the memory modules (12) in the device block correspond to “a plurality of memory devices”; (iii) the sequencer (8) in the device block corresponds to “a control module”; and (iv) the memory interfaces (10) correspond to “a data module comprising a plurality of data handlers.”

(*Id.* at 78-79.) Respondents also provide the following annotation of Figures 1 and 4 from *Averbuj* to further demonstrate how independent claim 1 of the '434 patent maps onto the disclosure of *Averbuj*:



RX-0354 at Figs. 1, 4 (annotated and highlighted).

(*Id.* at 79.)

To show that *Averbuj* discloses “[a] self-testing memory module, comprising: a printed circuit board configured to be operatively coupled to a memory controller of a computer system” Respondents point to a portion of *Averbuj* that explains that “electronic devices (2) are generally ‘constructed from many integrated circuit chips and many supporting components *mounted on a circuit board.*’” (*Id.* (emphasis Respondents’) (citing RX-0354 ¶ 5 (emphasis added); RX-0008C at Q/A 285).) Respondents also note that *Averbuj* states that the electronic device may be “any device that incorporates memory modules, such as embedded *computing systems, a computer, server.*” (*Id.* (emphasis Respondents’) (citing RX-0354 ¶ 32 (emphasis

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added); RX-0008C at Q/A 285.) Finally, Respondents argue that *Averbuj* “states that under normal operating conditions, those memory modules can be configured to receive address and control signals and data from an external programmable processor, *i.e.*, a ‘memory controller.’” (*Id.* (citing RX-0354 ¶ 48; RX-0008C at Q/A 285-87).)

Complainant counters that Respondents improperly refer to the “electronic device” disclosed in *Averbuj* as both a “self-testing memory module” and a “computer system.” (CIB at 55 (citing RX-0008C at Q/A 281, 283).) Complainant argues that the “electronic device” cannot be twisted to satisfy both claim elements. (*Id.* (citing CX-0931C, at Q/A 419-20).) Additionally, Complainant criticizes Respondents’ reliance on the “external programmable processor” of *Averbuj* to satisfy the “memory controller” element of claim 1. (*Id.*) Complainant notes that “[t]he portions of *Averbuj* cited by Mr. Hoffman do not even include the word ‘external,’” and that it is unclear what Mr. Hoffman is alleging the programmable processor is external to or from.” (*Id.* (citing RX-0008C at Q/A 287; RX-0354, at ¶ 0048).)

Staff does not address this element specifically in its briefing.

In response to Complainant’s criticisms, Respondents note that under their reading of *Averbuj*, “[e]ach device block within the electronic device of *Averbuj* is the claimed ‘memory module’” not the electronic device. (RRB at 46.)

The undersigned agrees with Complainant that Respondents have improperly relied on the “electronic device” disclosure of *Averbuj* to satisfy this element of independent claim 1. The issue, however, is not that Respondents claim the “electronic device” disclosed in *Averbuj* corresponds to the self-testing memory module of independent claim 1. Respondents clearly indicate that, under their interpretation of *Averbuj*, the “device block” elements correspond to the “self-testing memory module” of independent claim 1. (RIB at 78.) Rather, the issue is that

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Respondents point to the “electronic device” element of *Averbuj* to demonstrate the presence of the “printed circuit board” element of independent claim 1. (*Id.* at 79.) The problem with Respondents’ position is that independent claim 1 of the ’434 patent recites “[a] self-testing memory module, comprising: a printed circuit board configured to be operatively coupled to a memory controller of a computer system” (JX-0003 at Cl. 1.) Thus, the printed circuit board of independent claim 1 is a component of the self-testing memory module. (*See id.*) With respect to Respondents’ interpretation of *Averbuj*, under which the “device blocks” correspond to the self-testing memory modules of independent claim 1, Respondents must show that *Averbuj* discloses a device block comprising a printed circuit board, among other components. Respondents have not made that showing.

Instead, Respondents note that *Averbuj* discloses the uncontroversial fact that electronic devices, such as computers or computer systems, often include printed circuit boards. (RIB at 79 (citing RX-0354 ¶5).) That disclosure, however, is simply inapposite to what Respondents must show to establish anticipation by *Averbuj*. Neither Respondents in their briefing, nor their expert, Mr. Hoffman, identify any portion of *Averbuj* that discloses that the device blocks are comprised of a printed circuit board. (*See Id.* at 78-80; RRB at 46; RX-0008C at Q/A 284-285.) Further, testimony from Complainant’s expert, Mr. Murphy, suggests that the entire architecture disclosed in Figure 1 of *Averbuj* is located on a single integrated chip, as opposed to being multiple components placed on a printed circuit board. (*See CX-0931C* at Q/A 392, 395, 406, 411.)

In sum, the undersigned finds that Respondents have failed to show by clear and convincing evidence that *Averbuj* discloses “[a] self-testing memory module, comprising: a printed circuit board configured to be operatively coupled to a memory controller of a computer system” At best, Respondents have established that *Averbuj* discloses the use of printed

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circuit boards in electronic devices. That disclosure falls well-short of showing that *Averbuj* discloses a self-testing memory module comprised of a printed circuit board, which is what is required to establish anticipation of independent claim 1 of the '434 patent. Accordingly, the undersigned finds that *Averbuj* does not anticipate independent claim 1 of the '434 patent.

(2) Dependent Claims 2, 3 and 5-7

Each of claims 2, 3 and 5-7 depends from independent claim 1 of the '434 patent, and thus incorporate each limitation of independent claim 1, including “[a] self-testing memory module, comprising: a printed circuit board configured to be operatively coupled to a memory controller of a computer system” (See JX-0003 at Cls. 1-3, 5-7.) Further, none of the additional limitations in dependent claims 2, 3 and 5-7 obviate or alter the limitation of independent claim 1 that requires the self-testing memory module be comprised of a printed circuit board. (See *id.*) Accordingly, the undersigned finds that *Averbuj* does not anticipate dependent claims 2, 3 and 5-7 for the same reason it does not anticipate independent claim 1 of the '434 patent.

b) U.S. Patent No. 7,562,271 (“*Shaeffer*”)

Respondents submit that *Shaeffer*, which issued on July 14, 2009 from an application filed on April 6, 2007, anticipates each of asserted dependent claims 2, 3 and 5-7 of the '434 patent. (RIB at 89-95.) Respondents reference Figure 5 from *Shaeffer* and map its disclosure onto the elements of independent claim 1 as follows:

FIG. 5 shows a “memory module” (500); (ii) the memory devices 101a-d correspond to “a plurality of memory devices”; (iii) the buffer device 501 corresponds to “a control module”; and (iv) the buffer devices 100a-d correspond to “a data module comprising a plurality of data handlers.”

(*Id.* at 89.) Respondents provide the following annotated copy of Figure 5 to support their case:

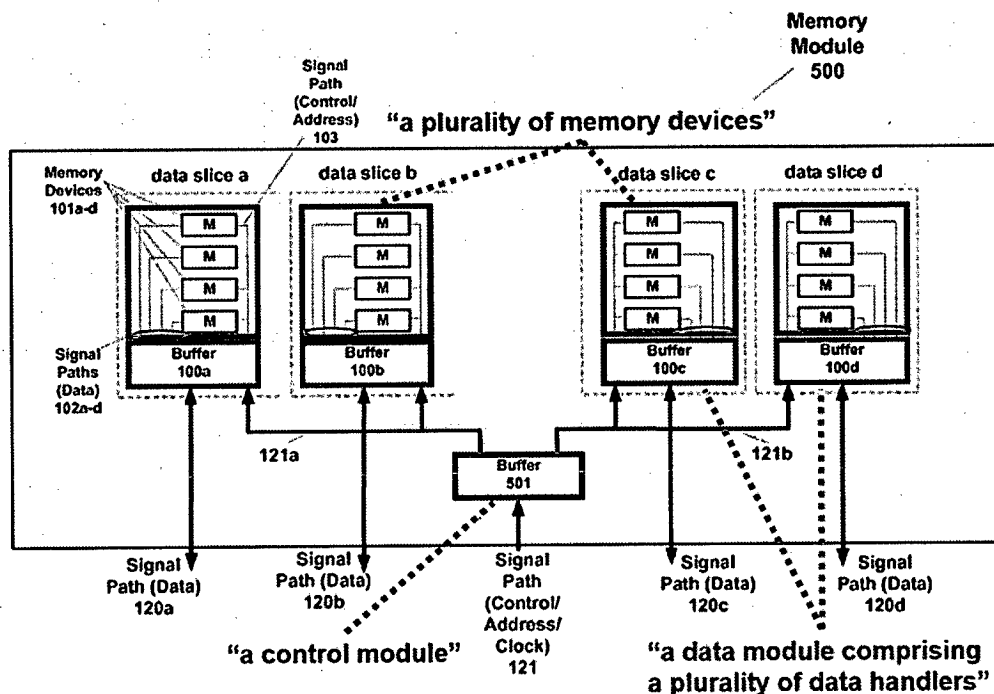


Fig. 5

(*Id.* at 90.)

(1) Claim 1 – “a control module configured to generate address and control signals for testing the memory devices”

Independent claim 1 of the '434 patent recites a self-testing memory module comprising, among other elements, a circuit comprising “a control module configured to generate address and control signals for testing the memory devices.” (JX-0003 at Cl. 1.) In *Shaeffer*, Respondents contend that “address and control buffer 501 in Figure 5 corresponds to a ‘control module.’” (RIB at 91.) However, Respondents note that their contention is based upon a construction for the term “generate” that would include merely decoding packets of data. (*See Id.* at 91-92.)

Complainant argues, *inter alia*, that buffer 501 cannot be the control module of independent claim 1 “because *Shaeffer* describes Buffer 501 as outputting control, address, and/or clock information.” (*Id.* at 50 (emphasis Complainant’s) (citing CX-0931C, at 588-601).) Accordingly, Complainant submits that buffer 501 of *Shaeffer* does not generate any address or

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control signals, but instead merely propagates address and control signals generated by a host. (*See id.*) Further, Complainant submits that none of the constructions proposed by the parties for “generate” would include buffer 501’s propagation of address and control signals. (*See id.*)

Staff also argues that *Shaeffer* does not anticipate independent claim 1 based at least on the absence of the control module limitation from *Shaeffer*’s disclosure. (*See* SIB at 87.) Similar to Complainant, Staff submits that the evidence shows that buffer 501 does not “generate” address and control signals, and thus cannot be the “control module” of independent claim 1. (*See id.* at 87-88.)

In response to Complainant’s and Staff’s positions, Respondents do not dispute that buffer 501 of *Shaeffer* receives address and control signals from a separate source prior to outputting them. Rather, Respondents argue that *Shaeffer* discloses buffer 501 receiving those signals in the form of packets, which the buffer must unpack prior to outputting them. (*See* RRB at 48-49.) Respondents contend that, on infringement, Complainant adopted the position that merely unpacking packets of data would satisfy the “generate” limitation, and thus Complainant should be bound by the same construction for “generate” with respect to this anticipation analysis. (*See id.* at 49.) Complainant disputes that *Shaeffer* actually discloses that buffer 501 decodes packets. (*See* CRB at 30 (“nothing in *Shaeffer* discloses that buffer 501 ever receives a packet, much less decodes it.”).)

The undersigned finds that *Shaeffer* does not disclose “a control module configured to generate address and control signals for testing the memory devices.” (’434 patent at Cl. 1.) With respect to whether *Shaeffer* discloses the “control module” of independent claim 1, Respondents are clear that their position is contingent upon a construction for the term “generate” that would include decoding packets of data that were first produced by a different component than the control

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module. (See RIB at 91-92; RRB at 48-49.) For the reasons explained in sections IV.C.2 and IV.D.1.e of this initial determination, the term “generate” as it appears in independent claim 1 of the '434 patent does not encompass merely decoding packets of data that were originally produced by a different component. The same holds true with respect to the generation of control signals.

Here, there is no dispute that the control signals that are output by buffer 501 are not produced by buffer 501. (RX-0008C at Q/A 400; RX-0351 at 9:35-52; CX-0931C, at Q/A 592.) They are produced by a separate component, such as a host, and then are received by buffer 501. (See RDX-0008C at Q/A 400 (“... the buffer device 501 shown in Figure 5 receives address and control signals from the host and outputs the corresponding address and control signals.”).) Accordingly, buffer 501 cannot be the “control module” of independent claim 1 of the '434 patent because it does not generate control signals. This conclusion would not change even if *Shaeffer* disclosed an embodiment where buffer 501 decoded data packets containing control signals, because there would still be no evidence that the control signals were produced, *i.e.*, brought into existence, by buffer 501. Just as it was improper to expand the plain and ordinary meaning of “generate” to include any transformation or modification of data in the context of infringement, so too is it inappropriate to expand the definition in the context of invalidity.

Because *Shaeffer* does not disclose at least the “control module” limitation of independent claim 1 of the '434 patent, the undersigned finds that Respondents have not shown by clear and convincing evidence that *Shaeffer* anticipates independent claim 1.

(2) Dependent Claims 2, 3 and 5-7

Each of claims 2, 3 and 5-7 depends from independent claim 1 of the '434 patent, and thus incorporate each limitation of claim 1, including “a control module configured to generate address and control signals for testing the memory devices” (See JX-0003 at Cls. 1-3, 5-7.)

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Further, none of the additional limitations in dependent claims 2, 3 and 5-7 obviate or alter that limitation. (*See id.*) Accordingly, the undersigned finds that *Shaeffer* does not anticipate dependent claims 2, 3 and 5-7 for at least the same reason it does not anticipate independent claim 1 of the '434 patent, *i.e.*, *Shaeffer* does not disclose “a control module configured to generate address and control signals for testing the memory devices.”

c) Fully-Buffered DIMMs with Intel Advanced Memory Buffers (“Intel AMB Datasheet”)

Respondents' third anticipation argument is based on the Intel 6400/6402 Advanced Memory Buffer Datasheet (“Intel AMB Datasheet”), which they contend was available to the public around October 2006. (RIB at 98; *see* RX-0353.) Respondents contend that “[t]he Intel AMB Datasheet describes the design and operations of the Intel 6400/6402 Advance Memory Buffers (“Intel AMB”), which were incorporated into Fully-Buffered DIMMs (“FB-DIMMs”) used prior to the alleged self-test invention dates.” (RIB at 99 (citing RX-0008C at Q/A 195-204).) Additionally, Respondents contend that “SK hynix’s HYMP564F72BP8N2 FB-DIMMs included the Intel AMB and were tested for compatibility with Intel’s Server Board S5000VSA as early as July 2006,” and were sold and used in the United States in August 2006. (*Id.* (citing RX-0903; RX-1540C; RX-0902; RX-0905C; RX-0906C; RX-0907C).) Thus, Respondents rely on its own FB-DIMMs as anticipatory prior art as well. (*Id.*)

(1) Claim 1 – “a data module comprising a plurality of data handlers”

Respondents argue that this element of independent claim 1 of the '434 patent is present in the Intel AMB Datasheet. (*See Id.* at 101.) Specifically, Respondents submit that “[t]he Intel Datasheet and the Intel S5000VSA Server Board Testing document show that a motherboard of a computer or a server may include a plurality of FBDIMMs that incorporate the Intel AMB.” (*Id.*

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(citing RX-0353.054 at Fig. 5-1; RX-0903.008 at Fig. 1; RX-0008C at Q/A 226.) While not stated explicitly, the clear implication here is that the plurality of FB-DIMMs disclosed by the prior art correspond to the plurality of data handlers recited as elements comprising the data module of independent claim 1. (*See id.*) Similarly, it appears that Respondents contend that the motherboard of a computer or a server corresponds to the data module of independent claim 1, inasmuch as the plurality of FB-DIMMs are components on those motherboards. (*See id.*)

Complainant rejects Respondents' interpretation of the datasheet and server board document, and points to its expert's testimony that "the reference to a motherboard including two or more DIMMs provides no explanation of which component(s) allegedly anticipate the claimed 'data module comprising a plurality of data handlers.'" (CIB at 47 (citing CX-0931C at Q/A 666-69).) Considering an alternative interpretation of Respondents' position, Complainant argues that "[t]o the extent the AMBs are alleged to be the claimed 'data handlers,' this argument fails because the '434 patent describes data modules as singular, discrete logic." (*Id.* (citing JX-0003 at 9:58-63, 12:30-37.)) Ultimately, Complainant submits that "[a]t best, Intel AMB discloses a plurality of memory modules each of which contains a single AMB or 'data handler,'" and thus "each DIMM only discloses a single 'data handler.'" (*Id.* (citing CX-0931C, at Q/A 646, 667).)

Staff also disagrees with the way Respondents map the prior art onto the data module element of independent claim 1. (*See* SIB at 82.) Particularly, Staff takes issue with the fact that Respondents appear to identify the same component from the prior art to satisfy both "control module" and "data module" limitations of independent claim 1. (*Id.* (citing CX-0931C at Q/A 659-663; '434 patent, at Figures 1-3, 8:33-52, 9:58-63, 12:30-37).) Further, Staff submits that Respondents expert "has failed to show how the Intel AMB 'generates' the claimed 'control signals' or 'data.'" (*Id.* (citing CX-0931C at Q/A 659-663; RX-0008C at Q/A 218-221).)

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The undersigned finds that Respondents have not carried their burden of demonstrating by clear and convincing evidence that the Intel AMB Datasheet, or its own FB-DIMMs incorporating the Intel AMB anticipate independent claim 1 of the '434 patent. As an initial matter, Respondents and their expert, Mr. Murphy, are less than clear about what element of the prior art corresponds to the "data module," and what elements correspond to the "plurality of data handlers." Unlike the other prior art references Respondents rely on for anticipation, the Respondents do not clearly map the disclosures of the Intel AMB Datasheet to the elements of independent claim 1 of the '434 patent. The result of that omission is considerable confusion as to how Respondents actually apply the prior art to the claim. Indeed, the undersigned has interpreted Respondents' position to be that the data module is the motherboard within a computer or server on which the plurality of FB-DIMMs are attached. The undersigned's interpretation is based on Respondents' briefing, as well as its expert's testimony. (*See* RIB at 101 ("The Intel Datasheet and the Intel S5000VSA Server Board Testing document show that a motherboard of a computer or a server may include a plurality of FBDIMMs that incorporate the Intel AMB."); RX-0008C at Q/A 226 ("a motherboard of a computer or a server may include a plurality of FBDIMMs that incorporate the Intel AMB.")) However, Complainant and Staff both address divergent, but not wholly unreasonable, interpretations where the Intel AMB itself is either the data module or the data handlers. (*See* CIB at 46-47; SIB at 82.)

Invalidity must be proven by clear and convincing evidence. Here, where it is unclear how exactly Respondents intend to map the disclosure of the prior art onto the data module and data handlers elements of independent claim 1, that clear and convincing standard of proof has not been met.

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Notwithstanding the ambiguity about how Respondents have mapped the disclosure of the prior art onto independent claim 1, Respondents' argument would fail under both the undersigned's and the Complainant's interpretation of Respondents' position. If Respondents intend to map the computer or server motherboard onto the "data module" limitation of independent claim 1, as Mr. Hoffman seems to do, (RX-0008C at Q/A 226), then Respondents have improperly ignored the language of independent claim 1 indicating that the self-testing memory module is *comprised* of a data module. (See '434 patent at Cl. 1.) Respondents clearly state that, with respect to the Intel AMB Datasheet, "FB-DIMMs with an Intel AMB are 'self-testing memory modules.'" (RIB at 99.) Accordingly, if an FB-DIMM with an Intel AMB corresponds to the self-testing memory module of independent claim 1, the data module, which is one element comprising the self-testing memory module, must correspond to some element that comprises an FB-DIMM with an Intel AMB. Under Mr. Hoffman's interpretation, this concept is flipped, as the FB-DIMM itself is an element on the motherboard of a computer or server, and thus the data module is comprised of a self-testing memory module. That is simply not what is claimed in the '434 patent.

A similar problem exists with the "plurality of data handlers" element of independent claim 1. Assuming that each FB-DIMM is a self-testing memory module, as Respondents have indicated, the plurality of data handlers, which comprise the data module, must also be elements that comprise the FB-DIMM. However, Respondents and their expert appear to contend that the FB-DIMMs distributed across a computer or server motherboard are the plurality of data handlers. Not only does this approach require a convoluted interpretation of independent claim 1 wherein the self-testing memory module is equivalent to the plurality of data handlers of which it is partly comprised, it ignores the requirement that there be a *plurality* of data handlers in the

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self-testing memory module. In other words, even assuming that an FB-DIMM can be both a self-testing memory module and a data handler, each self-testing memory module would then have, by definition, only one data handler—not a plurality of data handlers.

Finally, if alternatively the Intel AMB itself is considered to be the data handler, Respondents' anticipation argument would still fail. There is no evidence that there is more than one Intel AMB on a FB-DIMM, and thus there would be no plurality of data handlers on the self-testing memory module.

For the reasons discussed herein, the undersigned finds that Respondents have failed to establish by clear and convincing evidence that the Intel AMB Datasheet or SK Hynix's own FB-DIMMs anticipate independent claim 1 of the '434 patent.

(2) Dependent Claims 2, 3 and 5-7

Each of claims 2, 3 and 5-7 depends from independent claim 1 of the '434 patent, and thus incorporate each limitation of independent claim 1, including “a data module comprising a plurality of data handlers” (See JX-0003 at Cls. 1-3, 5-7.) Further, none of the additional limitations in dependent claims 2, 3 and 5-7 obviate or alter that limitation. (See *id.*) Accordingly, the undersigned finds that the Intel AMB Datasheet and SK Hynix DIMMs do not anticipate dependent claims 2, 3 and 5-7 for at least the same reason they do not anticipate independent claim 1 of the '434 patent, *i.e.*, the Intel AMB Datasheet and SK Hynix DIMMs does not disclose “a data module comprising a plurality of data handlers”

3. Indefiniteness

Respondents' indefiniteness argument is dependent on construing the term “generate” in the asserted claims to mean “produce or cause.” (RIB at 102.) As detailed *supra*, “generate” has not been construed to mean “produce or cause,” but rather has been construed to mean “produce

(i.e., bring into existence, including by transformation or modification of information and/or data received from another component).” Supra at IV.C.2. Because Respondents’ indefiniteness argument was dependent on construing “generate” to mean “produce or cause,” it necessarily fails in the absence of that construction. Accordingly, the undersigned finds that Respondents have failed to establish that the asserted claims of the ’434 patent “fail to inform, with reasonable certainty, those skilled in the art about the scope of the invention,” as required by *Nautilus, Inc. v. Biosig Instruments, Inc.*, 134 S. Ct. 2120, 2123 (2014). Thus, the undersigned also finds that Respondents have failed to show by clear and convincing evidence that the asserted claims of the ’434 patent are invalid as indefinite.

V. U.S. PATENT NO. 8,359,501

A. Overview

1. Asserted Claims

Complainant asserts dependent claim 4 of the ’501 patent. Claim 4 depends from independent claim 1. Those claims provide as follows:

1. A memory system configured to be operatively coupled to a memory controller of a computer system, the memory system comprising:

a plurality of memory chips;

a plurality of data handlers configured to be operated independently from one other, wherein one or more data handlers of the plurality of data handlers are configured to generate data for writing to a corresponding one or more memory chips of the plurality of memory chips;

a control circuit configured to generate address and control signals, wherein the memory system is configured to test the one or more memory chips using the address and control signals generated by the control circuit and using the data generated by the one or more data handlers.

* * * * *

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4. The memory system of claim 1, wherein the memory system comprises at least two physically separate integrated circuit packages, wherein each of the at least two physically separate integrated circuit packages comprises at least one data handler of the plurality of data handlers.

(JX-0004 at Cls. 1, 4.)

B. Level of Ordinary Skill in the Art

The parties all agree that, by virtue of sharing a common specification, the level of ordinary skill in the art for the '501 patent is the same as for the '434 patent. (See CIB at 65; RIB at 49; SIB at 95-96.) Accordingly, for the reasons explained *supra* in section IV.B, the undersigned finds that, with respect to the '501 patent, a person of ordinary skill in the art would have "a Bachelor's degree in electrical engineering, computer engineering, or in a related field and at least one year of work experience relating to memory systems, and would be familiar with the design of memory devices, memory modules, and built-in-self test or BIST."

C. Claim Construction

There are three disputed claim terms relevant to the asserted claims of the '501 patent:

1. "generate"
2. "test"
3. "wherein the memory system is configured to test the one or more chips"

(SIB at 96.) The parties submit that, because the '501 patent shares a common specification with the '434 patent, the first two terms should be construed consistently between the two patents. (See CIB at 65; RIB at 49; SIB at 96.) The undersigned agrees. Thus, "generate" and "test" shall be construed for the purposes of the '501 patent consistently with their construction in the '434 patent, which is detailed *supra* in section IV.C.2-3.

With respect to the third term, "wherein the memory system is configured to test the one or more chips," the parties also rely on their arguments with respect to the '434 patent. (See CIB

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at 65; RIB at 49.) Staff notes that, while this term does not appear in the '434 patent explicitly, “[t]he parties’ dispute over the phrase ‘the memory system is configured to test the one or more memory chips’ basically tracks their dispute over the term ‘test’ in the '434 Patent.” (SIB at 98.) Thus, Staff also relies on its claim constructions arguments with respect to the '434 patent.

As Staff points out, the dispute over the term “wherein the memory system is configured to test the one or more chips” is based on the dispute over the term “test.” Indeed, the parties proposed constructions differ only to the extent they substitute different constructions for the term “test” into the full phrase. (*See, e.g., id.*) Accordingly, and based upon the determination that “test” should be given its plain and ordinary meaning, *see supra* at § IV.C.3, the undersigned finds that “wherein the memory system is configured to test the one or more chips” should also be given its *plain and ordinary meaning*.

D. Infringement

1. Claim 1

Complainant does not raise any new arguments or present any new evidence to establish that the accused LRDIMM products infringe independent claim 1 of the '501 patent. Rather, Complainant relies exclusively on the arguments and evidence raised in the portion of its briefing addressing infringement of the '434 patent. (*See* CIB at 65-66.) Respondents and Staff adopted the same approach in responding to Complainant’s infringement allegations. (*See* RIB at 59; SIB at 98.)

In the absence of any new arguments or evidence, the undersigned finds that Complainant has not established by a preponderance of the evidence that the accused LRDIMM products infringe independent claim 1 of the '501 patent. Specifically, and for the reasons detailed *supra* in section IV.D.1.e-f, the undersigned finds that Complainant has failed to establish that the accused LRDIMM products include one or more data handlers that generate data. Because every

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limitation of an asserted must be present in an accused device to establish infringement, the undersigned also finds that the accused LRDIMM products do not infringe independent claim 1 of the '501 patent.

2. Dependent Claim 4

As with independent claim 1 of the '501 patent, the parties rely exclusively on their briefing of the '434 patent to address infringement of dependent claim 4 of the '501 patent. (*See* CIB at 66; RIB at 59; SIB at 99.) Moreover, claim 4 of the '501 patent depends from independent claim 1 of the '501 patent and thus incorporates every limitation of independent claim 1. Accordingly, because the undersigned has determined that independent claim 1 of the '501 patent is not infringed by the accused LRDIMM products, so too is dependent claim 4 not infringed by those products.

E. Domestic Industry – Technical Prong

As with the '434 patent, Complainant relies on its HybridDIMM Products and its HyperCloud products to satisfy the technical prong of the domestic industry requirement with respect to the '501 patent. (*See* CIB at 66-67.) With respect to the HyperCloud products, neither Respondents nor Staff dispute that the HyperCloud products satisfy the technical prong of the domestic industry requirement as applied to the '501 patent. (RIB at 77-78; SIB at 99-100.) Further, the evidence of record supports the conclusion that the Complainant's HyperCloud products do practice at least claims 1 and 4 of the '501 patent. (*See* CX-0005C at Q/A 925-982, 1159-1165; RX-1586C at Q/A 422-423.) Accordingly, the undersigned finds that Complainant's HyperCloud products satisfy the technical prong of the domestic industry requirement with respect to the '501 patent.

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Regarding Complainant's HybriDIMM products, the parties agree that the HybriDIMM products function identically to the accused LRDIMM products for the purposes of the domestic industry analysis. (CIB at 42, 67; RIB at 77-78; SIB at 78.) Consistent with that view, all parties rely on their arguments regarding infringement by the accused LRDIMM products to address whether the HybriDIMM products satisfy the technical prong of the domestic industry requirement for the '501 patent. (CIB at 67; RIB at 77-78; SIB at 100.) As noted *supra* in section IV.E, the record supports the conclusion that the HybriDIMM products function in the same way as the accused LRDIMM products for the purposes of analyzing the technical prong of the domestic industry requirement. Accordingly, for the same reasons that the accused LRDIMM products do not infringe claims 1 or 4 of the '501 patent, the undersigned also finds that the HybriDIMM products do not satisfy the technical prong of the domestic industry requirement with respect to the '501 patent. *See supra* at § V.D.

Based on the foregoing reasoning, the undersigned finds that Complainant has satisfied the technical prong of the domestic industry requirement for the '501 patent based on its HyperCloud products.

F. Validity

With respect to the '501 patent, Respondents raise both anticipation and indefiniteness invalidity arguments. The arguments closely track those made with respect to the '434 patent.

1. Anticipation

Respondents present two separate anticipation challenges to claims 1 and 4 of the '501 patent. The first is based on *Averbuj*, and the second is based on *Shaeffer*. Respondents do not contend that the Intel AMB FBDIMMs anticipate the '501 patent.

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a) U.S. Patent Publication No. 2005/0257109 A1 (*Averbuj*)

(1) Claim 1 (Unasserted)

As an initial matter, the undersigned notes that all of the parties treated the analysis of anticipation of the '501 patent by *Averbuj* as nearly co-extensive with anticipation of the '434 patent by *Averbuj*, notwithstanding the fact that the claims are not identical. This approach has created substantial confusion in the briefing.

For example, Respondents argue that “[e]ach limitation of claim 1 of the '501 patent is substantially the same as, or broader than, the corresponding limitation(s) of claim 1 of the '434 patent,” and thus “*Averbuj* anticipates claim 1 of the '501 patent for at least the same reasons *Averbuj* discloses claim 1 of the '434 patent.” (RIB at 84-85.) However, Respondents cite to no evidence supporting their conclusory assertion that independent claim 1 of the '501 patent is broader than independent claim 1 of the '434 patent. Indeed, Respondents’ expert, Mr. Hoffman, does not testify in his direct witness statement that such is the case. (*See* RX-0008C at Q/A 359-369.)

From this unsupported assertion that independent claim 1 of the '501 patent is broader than independent claim 1 of the '434 patent, Respondents attempt to show anticipation of the '501 patent by relying on their arguments with respect to the '434 patent. For example, Respondents argue that “[t]he preamble of claim 1 is broader than the preamble and the ‘printed circuit board’ limitation of '434 patent claim 1 because (a) '501 patent claim 1 is not limited to a ‘memory module’ but is instead directed to a ‘memory system’ that can include a memory module; and because (b) '501 patent claim 1 does not require ‘a printed circuit board.’” (RIB at 85.) Here again, Respondents cite no evidence to support the assertion that a “memory system” is broader than, and wholly contains, the structure of a “memory module.” (*See id.*) Indeed,

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neither the specification of the '501 patent, nor the testimony of Respondents' expert supports or contradicts that assertion. (See RX-0008C at Q/A 360-361.)

Respondents' expert's testimony on this portion of independent claim 1 of the '501 patent is as follows:

- a. **“A memory system configured to be operatively coupled to a memory controller of a computer system”**

Q360) *What is your opinion regarding the preamble of claim 1 of the 501 patent?*

A360) In my opinion, Averbuj discloses the preamble of claim 1 of the 501 patent under SK hynix's proposed construction and Netlist's apparent and/or proposed construction.

Q361) *What is your basis for your opinion?*

A361) Averbuj discloses the preamble for the same reasons Averbuj discloses the “a printed circuit board” element of claim 1 of the 434 patent. I already discussed how Averbuj discloses the “a printed circuit board” element of claim 1 of the 434 patent.

(*Id.*) As shown, rather than identify a portion of *Averbuj* that discloses a memory system, Mr. Hoffman focuses on the “printed circuit board” limitation of claim 1 of the '434 patent—a limitation that does not appear at all in independent claim 1 of the '501 patent. (*Id.*) Aside from the claims themselves, these two question and answer pairs are the only evidence cited by Respondents to establish that *Averbuj* discloses “a memory system configured to be operatively coupled to a memory controller of a computer system.” (JX-0004 at Cl. 1.)

There is no evidence in the record that a person of ordinary skill in the art would read *Averbuj* as disclosing “a memory system configured to be operatively coupled to a memory controller of a computer system,” or that a person of ordinary skill in the art would understand a “memory module” to be a type of “memory system.” The burden of proof on invalidity lies with Respondents, and here Respondents have failed to carry their burden to show how each element of independent claim 1 of the '501 patent is disclosed by *Averbuj*.

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The failure of proof is not limited to the preamble of independent claim 1 of the '501 patent either. Respondents, and Mr. Hoffman, give every element of independent claim 1 of the '501 patent the same cursory treatment. (See RX-0008C at Q/A 360-369.) By way of a second specific example, Respondents argue that the limitation “a control circuit configured to generate address and control signals” of independent claim 1 of the '501 patent “is broader than the ‘a control module’ limitation of claim 1 of the '434 patent because it is not limited to generating address and control signals for ‘testing the memory devices.’” (RIB at 86.) Here again, Respondents ask the undersigned to assume that a “control circuit” is equivalent to a “control module,” without providing any evidence to support that conclusion. The entirety of Mr. Hoffman’s direct testimony on the control circuit element is as follows:

d. “a control circuit configured to generate address and control signals”

Q366) *Claim 1 of the 501 patent recites “a control circuit configured to generate address and control signals.” What is your opinion regarding this claim element?*

A366) In my opinion, Averbuj discloses this claim element under both SK hynix’s proposed construction and Netlist’s apparent construction.

Q367) *What is your basis for your opinion?*

A367) Averbuj discloses this claim element for the same reasons each discloses the “a control module” element of claim 1 of the 434 patent. I already discussed how Averbuj discloses the “a control module” element of claim 1 of the 434 patent.

(RX-0008C at Q/A 366-367.) Nothing in Mr. Hoffman’s witness statement addresses why a person of ordinary skill in the art would interpret the “control module” element of independent claim 1 in the '434 patent to be coextensive with the “control circuit” element of independent claim 1 in the '501 patent. Respondents point to no other evidence to support that conclusion.

It is true that the '501 patent issued from a continuation of the '434 patent, and shares a common specification. (See '501 patent at Cover.) That relationship is not so strong though that it

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can relieve Respondents of their burden to prove invalidity by clear and convincing evidence. Anticipation requires showing the each element of a claim is disclosed, either explicitly or inherently, in a prior art reference. *See Kyocera Wireless Corp. v. Int'l Trade Comm'n*, 545 F.3d 1340, 1351 (Fed. Cir. 2008). Here, Respondents cannot make that showing by relying solely on arguments and evidence directed to anticipation of a claim from a different patent that utilizes different claim language. Accordingly, the undersigned finds that Respondents have failed to establish by clear and convincing evidence that independent claim 1 of the '501 patent is anticipated by *Averbuj*.

(2) Dependent Claim 4

Claim 4 depends from independent claim 1 of the '501 patent and thus incorporates all the limitations of independent claim 1. Thus, absent additional evidence establishing that *Averbuj* discloses all the elements of independent claim 1, Respondents' argument that *Averbuj* anticipates dependent claim 4 fails for the same reasons its argument that *Averbuj* anticipates independent claim 1 fails. Further, with respect to the additional limitations of dependent claim 4, Respondents again attempt to rely on equivalence to a claim of the '434 patent—dependent claim 3, specifically. (*See* RIB at 86-87.) Here again, Respondents lack evidence to support that equivalence. Mr. Hoffman's testimony—the only evidence cited by Respondents to support this anticipation argument—is not on point. It provides in its entirety:

- a. **“The memory system of claim 1, wherein the memory system comprises at least two physically separate integrated circuit packages, wherein each of the at least two physically separate integrated circuit packages comprises at least one data handler of the plurality of data handlers”**

Q370) What is your opinion regarding claim 4 of the 501 patent?

A370) In my opinion, *Averbuj* discloses claim 4 under both SK hynix's proposed construction and Netlist's apparent construction. To the extent it is found that *Averbuj* does not sufficiently disclose claim 4, *Averbuj* renders claim 4 obvious either alone or in combination with Tsern.

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Q371) *What is your basis for your opinion?*

A371) *Averbuj, either alone or in combination with Tsern, invalidates claim 4 of the 501 patent for the same reasons Averbuj, either alone or in combination with Tsern, invalidates claim 3 of the 434 patent.*

(RX-0008C at Q/A 370-371.) Mr. Hoffman's conclusory statements about anticipation are not sufficient to establish invalidity by clear and convincing evidence. Accordingly, the undersigned finds that Respondents have failed to establish that dependent claim 4 of the '501 patent is anticipated by *Averbuj*.

b) U.S. Patent No. 7,562,271 (*Shaeffer*)

(1) Claim 1 (Unasserted)

Like *Averbuj*, Respondents do not attempt to map each element of independent claim 1 of the '501 patent onto *Shaeffer*, but instead argue that "[e]ach limitation of claim 1 of the '501 patent is substantially same as, or broader than, the corresponding limitation(s) of claim 1 of the '434 patent," and therefore "*Shaeffer* discloses claim 1 for at least the same reasons it discloses claim 1 of the '434 patent." (RIB at 95.) Similarly, Respondents' expert, Mr. Hoffman, discusses anticipation of independent claim 1 of the '501 patent by *Shaeffer* exclusively by referring back to his testimony with respect to independent claim 1 of the '434 patent. (See RX-0008C at Q/A 418-428.) As explained in the previous section, the undersigned finds that this approach to establishing anticipation falls short of the clear and convincing evidence standard required given that the claims of the '434 and '501 patent, though from the same patent family, recite different claim limitations.⁷

⁷ The undersigned takes no position on whether there may be a scenario in which two claims from different patents of the same family may be so similar that proof of anticipation as to one necessarily proves anticipation of the other as well. That academic question is irrelevant to the instant investigation where the claims of the '434 and the '501 patent recite different claim limitations, and the evidentiary record lacks indicia that distinct terms such as "circuit" and "module" should be construed equivalently.

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Additionally, independent claim 1 of the '501 patent recites “a control circuit configured to generate address and control signals.” (JX-0004 at Cl. 1.) Even assuming that the control circuit of the '501 patent is equivalent to the control module of the '434 patent, Respondents' anticipation argument based on *Shaeffer* would fail. This is because, in the context of the '434 patent, Respondents argued that the control module generated data by virtue of unpacking data packets it received. That argument was based on a claim construction for “generate” that would have included merely decoding packets of data that were produced or brought into existence elsewhere. (See RIB at 91-92 (“Under Netlist’s novel claim construction and infringement positions advanced after fact discovery, decoding packets satisfies the term ‘generate.’”)) The undersigned has not adopted that construction, and thus, Respondents' argument that *Shaeffer* anticipates independent claim 1 of the '501 patent would fail because Respondents have not established by clear and convincing evidence that *Shaeffer* discloses “a control circuit configured to generate address and control signals.”

Accordingly, the undersigned finds that Respondents have failed to establish by clear and convincing evidence that *Shaeffer* anticipates independent claim 1 of the '501 patent.

(2) Dependent Claim 4

Claim 4 depends from independent claim 1 of the '501 patent and thus incorporates all the limitations of independent claim 1. Thus, absent additional evidence establishing that *Shaeffer* discloses all the elements of independent claim 1, Respondents' argument that *Shaeffer* anticipates dependent claim 4 fails for the same reasons its argument that *Shaeffer* anticipates independent claim 1 fails. Further, with respect to the additional limitations of dependent claim 4, Respondents again attempt to rely on equivalence to a claim of the '434 patent—claim 3, specifically. (See RIB at 97.) Here again, Respondents lack evidence to support that

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equivalence. Mr. Hoffman’s testimony—the only evidence cited by Respondents to support this anticipation argument—is not on point. It provides:

- a. **“The memory system of claim 1, wherein the memory system comprises at least two physically separate integrated circuit packages, wherein each of the at least two physically separate integrated circuit packages comprises at least one data handler of the plurality of data handlers”**

Q429) *What is your opinion regarding claim 4 of the 501 patent?*

A429) In my opinion, Shaeffer discloses claim 4 under both SK hynix’s proposed construction and Netlist’s apparent construction.

Q430) *What is your basis for your opinion?*

A430) Shaeffer discloses claim 4 of the 501 patent for the same reason Shaeffer discloses claim 3 of the 434 patent.

(RX-0008C at Q/A 429-430.) Mr. Hoffman’s conclusory statements about anticipation are not sufficient to establish invalidity by clear and convincing evidence. Accordingly, the undersigned finds that Respondents have also failed to establish that independent claim 4 of the ’501 patent is anticipated by *Shaeffer*.

2. Indefiniteness

Respondents raise the same indefiniteness argument for all three of the asserted self-test patents. (RIB at 102.) As noted *supra* in section IV.F.3, Respondents’ indefiniteness argument is dependent on construing the term “generate” in the asserted claims to mean “produce or cause.” (*Id.*) Here, however, “generate” has not been construed to mean “produce or cause,” but rather has been construed to mean “produce (*i.e.*, bring into existence, including by transformation or modification of information and/or data received from another component).” *Supra* at IV.C.2. Because Respondents’ indefiniteness argument was dependent on construing “generate” to mean “produce or cause,” it necessarily fails in the absence of that construction. Accordingly, the undersigned finds that Respondents have failed to establish that the asserted

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claims of the '501 patent "fail to inform, with reasonable certainty, those skilled in the art about the scope of the invention," as required by *Nautilus*, 134 S. Ct. at 2123. Thus, the undersigned also finds that Respondents have failed to show by clear and convincing evidence that the asserted claims of the '501 patent are invalid as indefinite.

VI. U.S. PATENT NO. 8,689,064

A. Overview

1. Asserted Claims

Complainant asserts independent claim 16 of the '064 patent. Independent claim 16 provides as follows:

16. A memory module for operating with a system memory controller, comprising:

a module controller to process input control signals from the system memory controller and to generate output control signals;

a plurality of memory devices configured to perform memory operations in response to signals from the module controller;

a plurality of data handlers, each respective data handler being configured to generate test data and to provide the test data to a respective set of at least one memory device of the plurality of memory devices in response to signals from the module controller; and

wherein the memory module is configured to obtain test results by reading from the respective set of at least one memory device in response to signals from the module controller and by comparing data read from the respective set of at least one memory device with the test data provided to the respective set of at least one memory device.

(JX-0005 at Cl. 16.)

B. Level of Ordinary Skill in the Art

The parties all agree that, by virtue of sharing a common specification, the level of ordinary skill in the art for the '064 patent is the same as for the '434 and '501 patents. (See CIB

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at 65; RIB at 49; SIB at 104.) Accordingly, for the reasons explained *supra* in section IV.B, the undersigned finds that, with respect to the '064 patent, a person of ordinary skill in the art would have “a Bachelor’s degree in electrical engineering, computer engineering, or in a related field and at least one year of work experience relating to memory systems, and would be familiar with the design of memory devices, memory modules, and built-in-self test or BIST.”

C. Claim Construction

There are three disputed claim terms relevant to the asserted claim of the '064 patent:

1. “generate”
2. “test”
3. “wherein the memory module is configured to obtain test results by”

(SIB at 104.) The parties submit that, because the '064 patent shares a specification with the '434 and '501 patents, the first two terms should be construed consistently between the two patents. (*See* CIB at 65; RIB at 49; SIB at 105.) The undersigned agrees. Thus, “generate” and “test” shall be construed for the purposes of the '064 patent consistently with their construction in the '434 and '501 patents, which is detailed *supra* in section IV.C.2-3.

With respect to the third term, “wherein the memory module is configured to obtain test results by,” Complainant and Respondents also rely on their arguments with respect to the '434 patent. (*See* CIB at 65; RIB at 49.) Staff notes that, while this term does not appear in the '434 patent explicitly, “[t]he parties’ dispute over the phrase ‘wherein the memory module is configured to obtain test results by’ in the '064 patent basically mirrors their dispute over the phrase ‘wherein the circuit is configured to test the memory devices’ in the '434 Patent.” (SIB at 107.) Thus, Staff also relies on its claim constructions arguments with respect to the '434 patent. (*See id.*)

The dispute over the term “wherein the memory module is configured to obtain test results by” is essentially wrapped up in the dispute over the term “test.” Indeed, the parties proposed constructions differ only to the extent they add elements of their proposed

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constructions for the term “test” by itself. (See, e.g., SIB at 106.) Accordingly, and based upon the determination that “test” should be given its plain and ordinary meaning, *see supra* at § IV.C.3, the undersigned finds that “wherein the memory module is configured to obtain test results by” should also be given its *plain and ordinary meaning*.

D. Infringement

1. Claim 16

Complainant does not raise any new arguments or present any new evidence to establish that the accused LRDIMM products infringe independent claim 16 of the '064 patent. Rather, Complainant cites back to the arguments and evidence raised in the portion of its briefing addressing infringement of the '434 patent. (See CIB at 66 (citing back to CIB at § III.A.1.) Respondents and Staff adopt the same approach in responding to Complainant's infringement allegations. (See RIB at 59; SIB at 107.)

In the absence of any new arguments or evidence, the undersigned finds that Complainant has not established by a preponderance of the evidence that the accused LRDIMM products infringe claim 16 of the '064 patent. Specifically, and for the reasons detailed *supra* in section IV.D.1.e-f, the undersigned finds that Complainant has failed to establish that the accused LRDIMM products include a plurality of data handlers, each being configured to generate test data. (See JX-0005 at Cl. 16.) Because every limitation of an asserted claim must be present in an accused device to establish infringement, the undersigned also finds that the accused LRDIMM products do not infringe independent claim 16 of the '064 patent.

E. Domestic Industry – Technical Prong

As with the '434 and '501 patents, Complainant relies on its HybriDIMM Products and its HyperCloud products to satisfy the technical prong of the domestic industry requirement with

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respect to the '064 patent. (See CIB at 66-68.) With respect to the HyperCloud products, neither Respondents nor Staff dispute that the HyperCloud products satisfy the technical prong of the domestic industry requirement as applied to the '064 patent. (RIB at 77-78; SIB at 107.) Further, the evidence of record supports the conclusion that the Complainant's HyperCloud products do practice at least claim 16 of the '064 patent. (See CX-0005C at Q/A 925-982, 1167-1175; RX-1586C at Q/A 422-423.) Accordingly, the undersigned finds that Complainant's HyperCloud products satisfy the technical prong of the domestic industry requirement with respect to the '064 patent.

Regarding Complainant's HybriDIMM products, the parties agree that the HybriDIMM products function identically to the accused LRDIMM products for the purposes of the domestic industry analysis. (CIB at 42, 67; RIB at 77-78; SIB at 108.) Consistent with that view, all parties rely on their arguments regarding infringement by the accused LRDIMM products to address whether the HybriDIMM products satisfy the technical prong of the domestic industry requirement for the '064 patent. (CIB at 67; RIB at 77-78; SIB at 108.) As noted *supra* in section IV.E, the record supports the conclusion that the HybriDIMM products function in the same manner as the accused LRDIMM products for the purposes of analyzing the technical prong of the domestic industry requirement. Accordingly, for the same reasons that the accused LRDIMM products do not infringe independent claim 16 the '064 patent, the undersigned also finds that the HybriDIMM products do not satisfy the technical prong of the domestic industry requirement with respect to the '064 patent. *See supra* at § VI.D.

Based on the foregoing reasoning, the undersigned finds that Complainant has satisfied the technical prong of the domestic industry requirement for the '064 patent based on its HyperCloud products.

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F. Validity

With respect to the '064 patent, Respondents raise both anticipation and indefiniteness invalidity arguments. The arguments closely track those made with respect to the '434 and '501 patents.

1. Anticipation

Respondents present two separate anticipation challenges to independent claim 16 of the '064 patent. The first is based on *Averbuj*, and the second is based on *Shaeffer*. Respondents do not contend that the Intel AMB FBDIMMs anticipate the '064 patent.

a) U.S. Patent Publication No. 2005/0257109 A1 (*Averbuj*)

(1) Claim 16

The parties adopt the same approach to addressing whether *Averbuj* anticipates independent claim 16 of the '064 patent as they did to address whether the reference anticipated claims 1 and 4 of the '501 patent, *i.e.*, they rely on their arguments with respect to whether *Averbuj* anticipates the asserted claims of the '434 patent. Particularly, rather than map the elements of independent claim 16 of the '064 patent onto *Averbuj*, Respondents go element by element stating that "*Averbuj* discloses this limitation for at least the same reasons *Averbuj* discloses" a limitation from independent claim 1 of the '434 patent.⁸ (RIB at 88; *see also* RIB at 87-89.) As noted above, the undersigned finds this approach to be insufficient to establish

⁸ There is a single exception where Respondents acknowledge that independent claim 16 of the '064 patent includes a limitation that is not in independent claim 1 of the '434 patent. Specifically, Respondents note that the limitation, "a module controller to process input control signals from the system memory controller and to generate output control signals" includes the additional limitation "processing input control signals from the system memory controller," which does not appear in the supposedly corresponding limitation from independent claim 1 of the '434 patent. (RIB at 87-88.) Accordingly, Respondents do provide somewhat more explanation regarding that limitation. (*See id.* at 88.)

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anticipation by clear and convincing evidence here, where independent claim 1 of the '434 patent and claim 16 of the '064 patent use different claim terms to recite different claim limitations.

For example, with respect to the limitation, “wherein the memory module is configured to obtain test results . . .” from independent claim 16 of the '064 patent, Respondents submit that “[t]his limitation is substantially identical to the ‘wherein the circuit is configured to test the memory devices’ limitation of claim 1 of the '434 patent.” (RIB at 89.) If true, then it would necessarily be the case that the “memory module” of independent claim 16 is interchangeable with the “circuit” of independent claim 1. But Respondents have presented no evidence to establish that a person of ordinary skill in the art would interpret the claims that way. To the contrary, Respondents cite only two question and answer pairs from their expert’s direct witness statement in connection with their anticipation arguments on this element of independent claim 16:

- e. **“wherein the memory module is configured to obtain test results by reading from the respective set of at least one memory device in response to signals from the module controller and by comparing data read from the respective set of at least one memory device with the test data provided to the respective set of at least one memory device”**

Q381) *Claim 1 of the 064 patent recites “wherein the memory module is configured to obtain test results by reading from the respective set of at least one memory device in response to signals from the module controller and by comparing data read from the respective set of at least one memory device with the test data provided to the respective set of at least one memory device.” What is your opinion regarding this claim element?*

A381) In my opinion, Averbuj discloses this claim element under both SK hynix’s proposed construction and Netlist’s apparent construction.

Q382) *What is your basis for your opinion?*

A382) Averbuj discloses this claim element for the same reasons Averbuj discloses the “where the circuit is configured to test the memory devices” element of claim 1 of the 434 patent. I already discussed how Averbuj discloses the “where the circuit is configured to test the memory devices” element of claim 1 of the 434 patent.

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(RX-0008C at Q/A 381-382.) These conclusory statements by Mr. Hoffman are not sufficient to meet Respondents' burden to show anticipation by clear and convincing evidence. Moreover, independent claim 1 of the '434 patent recites both a "memory module" and a "circuit." (JX-0003 at Cl. 1.) Respondents have not shown why, in the context of the '064 patent, "memory module" should be construed as synonymous to the "circuit" of the '434 patent, when "memory module" and "circuit" have distinct meanings within independent claim 1 of the '434 patent.

Accordingly, the undersigned finds that Respondents have failed to establish by clear and convincing evidence that independent claim 16 of the '064 patent is anticipated by *Averbuj*.

b) U.S. Patent No. 7,562,271 ("Shaeffer")

(1) Claim 16

Here again, Respondents rely primarily on their arguments with respect to anticipation of independent claim 1 of the '434 patent by *Shaeffer* to establish anticipation of independent claim 16 of the '064 patent by *Shaeffer*. (RIB at 97-98.) Respondents' expert, Mr. Hoffman, does the same. (See RX-0008C at Q/A 432-441.) As such, Respondents' anticipation argument again requires reading the "wherein the circuit is configured to test the memory devices" limitation of independent claim 1 of the '434 patent as synonymous to the "wherein the memory module is configured to obtain test results" limitation of independent claim 16 of the '064 patent. (See RIB at 98.) As noted in the previous section discussing *Averbuj*, Respondents have not offered evidence sufficient to support such a reading. Here again, Mr. Hoffman's expert testimony is wholly conclusory:

- e. **"wherein the memory module is configured to obtain test results by reading from the respective set of at least one memory device in response to signals from the module controller and by comparing data read from the respective set of at least one memory device with the test data provided to the respective set of at least one memory device"**

Q440) Claim 1 of the 064 patent recites, "wherein the memory module is configured to obtain test results by reading from the respective set of at least one

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memory device in response to signals from the module controller and by comparing data read from the respective set of at least one memory device with the test data provided to the respective set of at least one memory device.” What is your opinion regarding this claim element?

A440) In my opinion, Shaeffer discloses this claim element under both SK hynix’s proposed construction and Netlist’s apparent construction.

Q441) *What is your basis for your opinion?*

A441) Shaeffer discloses this claim element for the same reasons Shaeffer discloses the “where the circuit is configured to test the memory devices” element of claim 1 of the 434 patent. I already discussed how Shaeffer discloses the “where the circuit is configured to test the memory devices” element of claim 1 of the 434 patent.

(RX-0008C at Q/A 440-441.) As previously noted, these conclusory statements by Mr. Hoffman are not sufficient to meet Respondents’ burden to show anticipation by clear and convincing evidence. Accordingly, the undersigned finds that Respondents have failed to establish by clear and convincing evidence that independent claim 16 of the ’064 patent is anticipated by *Shaeffer*.

2. Indefiniteness

As previously noted, Respondents raise the same indefiniteness argument for all three of the asserted self-test patents. (RIB at 102.) As noted *supra* in section IV.F.3, Respondents’ indefiniteness argument is dependent on construing the term “generate” in the asserted claims to mean “produce or cause.” (*Id.*) Here, however, “generate” has not been construed to mean “produce or cause,” but rather has been construed to mean “produce (*i.e.*, bring into existence, including by transformation or modification of information and/or data received from another component).” *Supra* at IV.C.2. Because Respondents’ indefiniteness argument was dependent on construing “generate” to mean “produce or cause,” it necessarily fails in the absence of that construction. Accordingly, the undersigned finds that Respondents have failed to establish that the asserted claims of the ’064 patent “fail to inform, with reasonable certainty, those skilled in the art about the scope of the invention,” as required by *Nautilus*, 134 S. Ct. at 2123. Thus, the

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undersigned also finds that Respondents have failed to show by clear and convincing evidence that the asserted claims of the '064 patent are invalid as indefinite.

VII. U.S. PATENT NO. 8,489,837

A. Overview

1. Asserted Claims

Complainant alleges infringement of claims 1-3, 5 and 6 of the '837 patent. Claims 2, 3, 5 and 6 depend from independent claim 1. The asserted claims provide as follows:

1. A memory module comprising:

at least one output configured to be operatively coupled to a memory controller of a host computer system, the memory module configured to operate in at least two modes comprising an initialization mode during which the memory module executes at least one initialization sequence and an operational mode;

a controller circuit configured to cause the memory module to enter the initialization mode; and

a notification circuit configured to drive the at least one output while the memory module is in the initialization mode to provide at least one notification signal to the memory controller indicating at least one status of the at least one initialization sequence; and

wherein the at least one notification signal triggers the memory controller to execute an interrupt routine.

* * * * *

2. The memory module of claim 1, wherein the at least one status comprises completion of the at least one initialization sequence.

* * * * *

3. The memory module of claim 1, wherein the at least one status comprises execution of the at least one initialization sequence.

* * * * *

5. The memory module of claim 1, wherein the at least one output comprises

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an error-out pin of the memory module.

* * * * *

6. The memory module of claim 1, wherein the notification circuit is configured to drive the at least one output to a first state indicative of execution of the at least one initialization sequence or to a second state indicative of completion of the at least one initialization sequence.

(JX-0006 at Cls. 1-3, 5 and 6.)

B. Level of Ordinary Skill in the Art

Complainant contends that a person of ordinary skill in the art with respect to the '837 patent would have "a Bachelor's degree in electrical engineering, computer engineering, or in a related field and at least one year of work experience relating to memory systems, and would be familiar with the design of memory devices, memory modules, and built-in-self test or BIST."

(CIB at 70 citing CX-0005C at Q/A 96; CX-0931C at Q/A 111.)

Respondents do not agree with Complainant's proposed level of skill, and instead assert that a person with an appropriate level of skill in the art is

familiar with computer memory systems and basic CPU architecture as of 2009. He/she would have been familiar with techniques related to how computer components access a computer's memory, including the role of a memory controller, the basic operation of memory modules and devices, and the techniques used to couple memory devices to the other components of the computer system. He/she would have been familiar with techniques used for the initialization of computer systems, including initialization of memory components. Such a person would also have been familiar with the technical standards that govern the operation of memory devices. The person of ordinary skill in the art would have had a bachelor's degree in computer engineering, or a related field, and several years of additional experience working with computer memory systems.

(RIB at 105 (citing RX-1587C at Q/A 36).)

Staff indicates that Complainant's proposed level of skill "is more appropriate" owing to (i) the educational and professional experience of the inventor of the '837 patent as well as (ii) the subject matter disclosed therein. (SIB at 111-113 and SRB at 32-33.) In this regard, Staff notes,

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and Respondents acknowledge, that there are no material differences between the two proposed definitions of one of ordinary skill in the art. (SIB at 112-113, SRB at 32 and RRB at 52.)

Given (i) the evidence of record cited above by the parties and Staff, (ii) Respondents' acknowledged lack of material differences between the two proposed definitions and (iii) the educational and professional experience of the inventor of the '837 patent at the time of the invention, (*see* JX-0027C at 8:20-11:5 and *Phillips*, 415 F.3d at 1313 (explaining that it is a "well-settled understanding that inventors are typically persons skilled in the field of the invention and that patents are addressed to and intended to be read by others of skill in the pertinent art." (internal citations omitted))), the undersigned finds that the level of ordinary skill in the art for the '837 patent is consistent with the definition proposed by Complainant and Staff (*i.e.*, "a Bachelor's degree in electrical engineering, computer engineering, or in a related field and at least one year of work experience relating to memory systems, and would be familiar with the design of memory devices, memory modules, and built-in-self test or BIST").

C. Claim Construction

There are two disputed claim terms relevant to the asserted claims of the '837 patent each of which appears in all of the asserted claims of the '837 patent:⁹

1. "notification signal" and
2. "execute an interrupt routine."

Each is addressed in turn below.

⁹ Staff's Post Hearing Brief indicates that a third term (*i.e.*, "the at least one status comprises execution of the at least one initialization sequence") appearing in dependent claim 3 was initially in dispute. (SIB at 113-114.) At that time, Complainant and Staff agreed that this phrase should be given its plain and ordinary meaning. (CIB at 70; CX-0933C at Q/A 115, 126, 128, 148, 154, 162 and SIB at 114.) Although Respondents initially offered an express construction for this term, Respondents now agree that an express construction is not needed. (RIB at 111.)

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1. “notification signal”

The term “notification signal” appears in independent claim 1 from which claims 2, 3, 5 and 6 depend. The parties propose the following respective constructions for this term:

<i>“notification signal”</i>		
Complainant’s Proposed Construction	Respondents’ Proposed Construction	Staff’s Proposed Construction
plain and ordinary meaning	“signal notifying the memory controller of the status of the initialization sequence, not provided in response to polling”	plain and ordinary meaning

(SIB at 115; *see also* CIB at 70; RIB at 105.)

The parties and Staff all agree that the term “notification signal” should be interpreted consistent with its plain and ordinary meaning. (CIB at 70, CRB at 36-37, RRB at 53, SIB at 115 and SRB at 33-35) In this regard, neither the parties nor the Staff suggests that the ’837 patent provides an express definition or ascribes a “special meaning” to the term “notification signal.” As shown in the above table, however, Complainant and Staff disagree with Respondents as to what that plain and ordinary meaning is.

In particular, Complainant urges that “[t]he plain and ordinary meaning informs a person of ordinary skill in the art that ‘a notification signal’ is simply ‘a signal that notifies.’” (CIB at 73.) Complainant supports its position by way of the testimony of its expert. (*Id.* (citing CX-0005C, at Q/A 183); *see also* CX-0005C, at Q/A 186.)

Staff states that the plain and ordinary meaning of the term “notification signal” is “notification signal,” with the Staff further noting that this construction is warranted given that the term utilizes simple English-language words. (SIB at 115 and SRB at 35.)

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As between the constructions proffered by Complainant and Staff, the undersigned can find no discernible difference; a “notification signal” (*i.e.*, Staff’s plain and ordinary construction) is “a signal that notifies” (*i.e.*, Complainant’s plain and ordinary construction). Thus, it is unnecessary to adopt the term “a signal that notifies” in favor of the actual words (*i.e.*, “notification signal”) expressly recited in independent claim 1 where they both mean the same thing.

Respondents believe the term needs further clarification, and offers that it should be construed as a “signal notifying the memory controller of the status of the initialization sequence, not provided in response to polling.” (RIB at 105.) Respondents rely on both intrinsic and extrinsic evidence in support of its contentions. First, Respondents cite to the claims and various portions of the ’837 patent specification that the notification signal provides an indication regarding initialization and that polling is excluded as a trigger for the notification. (*Id.* at 105-106.) Respondents further assert that Complainant and its experts have each contended that the notification signal excludes polling. (*Id.* at 106 (citing Compl. at 23, Mangione-Smith, Tr., 437:19-438:16 and Murphy, Tr., 954:2-955:5).)

In considering Respondents’ proposed construction it can be viewed, as a matter of convenience to this analysis, as including three distinct parts: a “(i) signal notifying (ii) the memory controller of the status of the initialization sequence, (iii) not provided in response to polling.”

With respect to part (i), there appears to be no discernible substantive difference between the term “notification signal” as recited in independent claim 1 and Respondents’ proffered “signal notifying.” In this regard, this component of Respondents’ proposed language amounts to nothing more than the “plain and ordinary meaning” of the term “notification signal” offered by Complainant as discussed above. (CIB at 73, CX-0005C, at Q/A 183 and 186 (each indicating that a “notification signal” is “a signal that notifies”).) As was the case above, it is unnecessary—

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and there is no further clarity to be gained—by adopting the phraseology “signal notifying” in favor of the actual words (*i.e.*, “notification signal”) expressly recited in independent claim 1.

In view of the above, parts (ii) and (iii) of Respondents’ proposed construction can be considered to be modifications of the plain and ordinary meaning of “notification signal.” As discussed in detail below, such modifications are unnecessary.

With respect to part (ii), independent claim 1 of the ’837 patent recites, in relevant part, “a notification circuit configured to drive the at least one output while the memory module is in the initialization mode to provide at least one notification signal to *the memory controller indicating at least one status of the at least one initialization sequence.*” (Emphasis added). As can be seen, part (ii) of Respondents’ proposed construction merely adopts nearly identical modifying language already present in independent claim 1 to describe where the “notification signal” is delivered. Thus, this proposed additional language adds nothing to how the term “notification signal” should be construed or understood in the context of the rest of the claim that is not already recited. (*See* SIB at 115.) Indeed, it is redundant to the immediately succeeding claim language. Accordingly, it is unnecessary to adopt duplicative modifying language as part of a proposed claim construction.

With respect to point (iii), it would initially seem that Respondents have a point that the term “notification signal” should be construed to reflect that it is not provided in response to polling. Indeed, to the average or lay person the “plain and ordinary meaning” of the term “notification signal” would presumably include *any* signal that notifies, including in response to polling. However, the “plain and ordinary meaning” for a claim term is arrived at from the perspective of one of ordinary skill in that art who “is deemed to [have] read the claim term not only in the context of the particular claim in which the disputed term appears, but in the context of the entire patent,

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including the specification” and that “the ‘ordinary meaning’ of a claim term is its meaning to the ordinary artisan after reading the entire patent.” *Phillips*, 415 F.3d at 1313 and 1321 (internal citations omitted); *see also Vitronics*, 90 F.3d at 1582 (explaining that “it is always necessary to review the specification to determine whether the inventor has used any terms in a manner inconsistent with their ordinary meaning.”).

Here, the ’837 patent explicitly delineates between the “polling method” and “notifying method” and describes that “[c]ertain embodiments described herein provide a method of establishing a handshake mechanism based on notification signaling.” (JX-0006 at 3:24-55.) Accordingly, one of ordinary skill in the art arriving at the “plain and ordinary” meaning of the term “notification signal” *in the context* of the ’837 patent would recognize that it does not utilize polling. This conclusion is buttressed by the fact that the parties’ experts—each presumed to be persons of ordinary skill in the art—agreed that the term “notification signal” does not encompass “polling” given that the latter is disparaged in the ’837 patent. (*See Mangione-Smith*, Tr. at 437:19-438:16 and *Hoffman*, Tr. at 954:2-955:5.) Accordingly, it is unnecessary to expressly construe that the “notification signal” is “not provided in response to polling” given that the plain and ordinary meaning of the term “notification signal” to one of ordinary skill in the art based on the intrinsic teachings of the ’837 patent would exclude responding to polling.

In view of the forgoing, the undersigned finds that the term “notification signal” should be construed according to its *plain and ordinary meaning*.

2. “execute an interrupt routine”

The term “execute an interrupt routine” appears in independent claim 1 from which claims 2, 3 5 and 6 depend. The parties propose the following respective constructions for this term:

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<i>“execute an interrupt routine”</i>		
Complainant’s Proposed Construction	Respondents’ Proposed Construction	Staff’s Proposed Construction
plain and ordinary meaning	“process computer instructions that cause operations in response to a signal requesting attention from a computer’s processor”	plain and ordinary meaning

(SIB at 116; *see also* CIB at 74-75; RIB at 107-110.)

The parties and Staff all agree that the term “execute an interrupt routine” should be interpreted consistent with its plain and ordinary meaning. (CIB at 74, CRB at 37-39, RIB at 107-108, RRB at 54, SIB at 115 and SRB at 35-36.) Neither the parties nor the Staff suggests that the ‘837 patent provides an express definition or ascribes a “special meaning” to the term “execute an interrupt routine.” Nevertheless, Complainant and Staff disagree with Respondents as to what constitutes the plain and ordinary meaning.

Complainant urges that the plain and ordinary meaning should be adopted because “[t]he ‘837 patent specification discloses that a notification signal causing the memory module to ‘execute an interrupt routine’ causes the memory controller to execute appropriate operations for the status indicated by the notifying signal.” (CIB at 75 (citing the JX-0006 at 7:9-13, 7:18-29, and 7:38-41).) Thereafter, Complainant contends that Respondents’ proposed construction should not be adopted because it ignores the teachings of the ‘837 patent in favor of extrinsic evidence. (CIB at 75-77 and CRB at 37-39.)

Notably absent from Complainant’s contentions, however, is a clear indication as to what it exactly considers the plain and ordinary meaning to be, especially given that Complainant’s expert provided two different, albeit very similar, descriptions for the plain and ordinary meaning of “execute an interrupt routine”: (i) stating “that a person of ordinary skill in the art

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would understand that the term ‘execute an interrupt routine’ means to ‘take necessary steps in response to an interrupt signal,’” (CX-0005C at Q/A 190 (which reflects the construction set forth in CX-0933C at Q/A 146)), and (ii) citing Col. 7, lines 11-13 of the ’837 patent as “describe[ing] what executing an interrupt routine would mean to one of ordinary skill in the art: executing the necessary or appropriate steps in response to a status of a notification signal or interrupt signal.” (CX-0933C at Q/A 147.)

Staff asserts that the plain and ordinary meaning of the term “execute an interrupt routine” is “execute an interrupt routine.” (SIB at 116.) Staff, however, fails to support this assertion with, for example, citation to the ’837 patent. Instead, Staff contends only that Respondents are improperly attempting to import limitations from the specification into the claims. (*Id.* and SRB at 35-36.¹⁰)

Respondents contend that the “plain and ordinary” meaning of the term “execute an interrupt routine” is “process computer instructions that cause operations in response to a signal requesting attention from a computer’s processor.” (RIB at 107-110 and RRB at 54-56.) Respondents primarily rely on certain embodiments set forth in the written description of the ’837 patent for support. For example, Respondents point to Col. 7, lines 26-33 of the ’837 patent as describing that “the ‘notification signal... triggers execution of the interrupt routine, which interrupts the CPU’ and requires the CPU and/or memory controller to give ‘immediate attention’ to the completed initiation sequence.” (*Id.* at 108.) Respondents also point to the disclosure that “[i]n certain such embodiments, the system memory controller 14 can be responsive to the second state of the first memory module 10 and the fourth state of the second

¹⁰ It is unclear whether Complainant agrees with Staff’s exact language. However, Complainant does not appear to disagree with Staff’s specifically proposed language given it lodged no objection to the same in its Post-Hearing Reply Brief. (CRB at 37-39.)

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memory module 26 by *triggering execution of an interrupt routine by a processor of the system memory controller 14.*” (*Id.* at 108 (citing JX-0006 at 10:22-27 (emphasis added)).)

Based on the above, there appears to be some support for the contention that an instruction to “execute an interrupt routine” can come “from a computer’s processor.” However, as noted by both Complainant and Staff, these disclosures at most describe certain embodiments of the ’837 patent and appear to rest on the assumption that the memory controller is a computer’s processor. (CIB at 76-77, CRB at 37-39, SIB at 116, SRB at 35-36 and CX-0005C at Q/A 189.) Respondents do not cite to any portion of the ’837 patent or its prosecution file history to support that the ’837 patent claims are limited to embodiments where the “execute an interrupt routine” comes “from a computer’s processor.”

Moreover, the portions of the ’837 patent specification cited by Respondents are far from explicit on the point they are advocating (*i.e.*, that the “execute an interrupt routine” signal comes “from a computer’s processor”). For example, the portion of Col. 7, lines 26-33 of the ’837 patent indicates that “the ‘notification signal... triggers execution of the interrupt routine” and that the consequence of the triggering of the execution of the interrupt routine is an interruption of the CPU, not the other way around as Respondents assert. Similarly, Col. 10, ll. 22-27 of the ’837 patent indicates that system memory controller 14 responds to memory modules 10 and 14 results “by triggering execution of an interrupt routine by a processor of the system memory controller 14.” Nothing in this particular disclosure indicates that the “processor of the system memory controller 14” is “a computer’s processor.”

Respondents also cite various extrinsic dictionary sources to support their construction. (RIB at 108-109.) Extrinsic sources (*e.g.*, a technical or regular dictionary) can, under certain circumstances, be used to elucidate the meaning of a claim term. Respondents, however, have

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not provided any legal justification as to how or why a dictionary definition should delimit claim scope *vis-à-vis* the various embodiments described in the '837 patent. Rather, it is well-established that claims should not be confined to the specific embodiments described in the specification. *See Phillips*, 415 F.3d at 1323.

In view of the foregoing, therefore, the undersigned sees no basis to limit independent claim 1 to the embodiments cited by Respondents. Therefore, the undersigned finds that the term “execute an interrupt routine” should be construed according to its *plain and ordinary meaning*.

D. Infringement

1. Independent Claim 1

a. “A memory module comprising”

Complainant contends that the accused SKH RDIMM and LRDIMM products (“accused products”) are memory modules. (*See* CIB at 81 (citing, among other things, CX-0005C at Q/A 1185).) Respondents do not contest this fact as evidenced by the trial testimony of Respondents’ expert. (*See* Wedig, Tr. at 694:2-5.)

Staff does not set forth in its post-trial briefings any disagreement as to whether the accused products include this feature.

Thus, based on the evidence provided, the undersigned finds that the accused products include this feature of independent claim 1. (*See, e.g.*, CX-0005C at Q/A 1185.)

b. “at least one output configured to be operatively coupled to a memory controller of a host computer system, the memory module configured to operate in at least two modes comprising an initialization mode during which the memory module executes at least one initialization sequence and an operational mode”

There does not appear, based upon the post-trial briefing, to be a dispute among the parties as to whether the accused products include this claim feature.

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Complainant believes that the accused products include this feature, and cites to a variety of evidence purporting to establish the same. (CIB at 82-84.) Among other things, Complainant contends that the “ALERT_n” pin is an output. (*Id.* at 82 (citing CX-0005C at Q/A 1279-1291; Wedig, Tr. at 694:15-17).) Complainant also asserts that the “Clock-to-CA” training mode¹¹ of the accused products is an initialization mode. (*Id.* (citing CX-0005C, at Q/A 1293-97; CX-0288.66-67).)

Although Respondents do not appear to contest that the accused products include this feature, they do dispute that the “Clock-to-CA” training mode is an initialization mode. (RIB at 120-122 and RRB at 65-69.) In particular, Respondents argue that the “Clock-to-CA” training mode is not—and cannot be—an initialization mode because initialization occurs before the “Clock-to-CA” training mode begins and because the training of the “Clock-to-CA” mode is not “initializing.” (RIB at 120-121.) Thus, Respondents’ position appears to be, on the one hand, that the accused devices include an “initialization mode during which the memory module executes at least one initialization sequence” but, on the other hand, that the “Clock-to-CA” training mode does not perform that function.

Staff does not set forth in its post-trial briefings any disagreement as to whether the accused products include this feature.

With respect to whether the “Clock-to-CA” training is an initialization mode, the undersigned finds that it is. Aside from any potential semantic arguments regarding the relationship between “training” and “initialization,” the ’837 patent expressly indicates that (i) initialization mode “executes at least one initialization sequence” and (ii) “[t]he at least one initialization sequence (e.g., *comprising one or more training sequences*) may be initiated....” (JX-0006 at 5:44-51 (emphasis added); *see also* CRB at 39.) Thus, the ’837 patent makes clear

¹¹ Respondents refer to the “Clock-to-CA” training mode as “CA-Bus training.” (RIB at 116, *passim*.)

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that the initialization mode of independent claim 1 can include a training sequence. Given the absence of any evidence that such scope was surrendered during prosecution, the undersigned can find no basis to so restrict the term “initialization mode” now so as to exclude a training sequence.

Given (i) that the evidence shows and there being no dispute that the “ALERT_n” pin is an output and (ii) that the term “initialization mode” can include a training sequence, the undersigned finds that the accused products include this feature of independent claim 1.

c. “a controller circuit configured to cause the memory module to enter the initialization mode”

As noted above, the undersigned has determined that the “Clock-to-CA” training of the accused products corresponds to the “initialization mode” of independent claim 1. Thus, in order for Complainant to meet its burden of establishing that the accused products include this feature it must be shown that the accused controller circuit causes the accused products (which, as noted above, are memory modules) to enter the “Clock-to-CA” training mode. As described in detail below, the undersigned has determined that Complainant has failed to do so.

Complainant contends that the Register Clock Driver (“RCD”) corresponds to the claimed “controller circuit” and asserts that the RCD causes the memory modules to enter the accused initialization mode (*i.e.*, the “Clock-to-CA” training mode). (CIB at 84.) Complainant supports this contention with reference to (CX-0005C at Q/A 1303, 1330-1334; CX-0288 at 88, 91, and 100; Wedig, Tr. at 699:15-701:1; RPHB at 258; RX-1578C.40-41 at Q/A 105.)

Respondents and Staff both disagree with Complainant’s contention that the RCD “causes” the memory modules to enter the “Clock-to-CA” training mode and that Complainant has allegedly waived certain arguments regarding the prosecution history of the ’837 patent. (RIB at 122-124, RRB at 65-67, SIB at 117-118 and SRB at 36-37.) Respondents and Staff generally argue that the “memory controller” of the accused devices—and not the RCD—

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triggers the accused initialization mode (*i.e.*, the “Clock-to-CA” training mode).¹² (RIB at 122-124, RRB at 65-67, SIB at 117-118 and SRB at 36-37.)

The undersigned agrees with Respondents and Staff. Specifically, the evidence of record establishes that the RCD of the accused devices does not “cause” the accused products (*i.e.*, memory modules) to enter the “Clock-to-CA” training mode. Rather, the “memory controller” of the accused products causes entry into the accused initiation mode. (RX-1587C at Q/A 204-205 (*citing, inter alia*, RX-0320C (JEDEC Specifications) and RX-0283C (JEDEC Specifications).) Indeed, Complainant’s experts agreed. (Mangione-Smith, Tr. at 411:20-412:10 and RX-1587C at Q/A 211 (quoting Murphy Dep.).)

In the accused products, the “memory controller” controls when to enter/exit the accused “initialization mode” with control words and sets the registers in the memory module. (RIB at 122-124; RRB at 65, SIB at 117-118; SRB at 36-37; *see also* RX-1587C at Q/A 203-223.) To be clear, Complainant’s expert stated, with respect to the accused products, that “the Training Control Word is what determines what mode the memory module is in and *therefore is what causes the memory module to enter initialization mode,*” and those words are governed by actions of the memory controller. (CX-0005C at Q/A 1334 (emphasis added); Mangione-Smith, Tr. 409:9-412:3; RX-1587C at Q/A 211 (quoting Murphy dep. testimony).)

The ’837 patent underscores this conclusion. Specifically, the ’837 patent teaches that (i) “[i]n one embodiment, for example, the at least one initialization sequence may comprise one or more training sequences. The initialization sequence (e.g., comprising one or more training sequences) may be initiated by the system memory controller 14.” and (ii) “[i]n some

¹² According to Respondents, the “memory controllers” are not part of the accused products but instead “are part of the host computers in which the accused memory modules may be used.” (RIB at 112.)

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embodiments, the controller circuit 18 is configured to cause the memory module 10 to enter the initialization mode.” (JX-0006 at 5:46-51.) Thus, the ’837 patent sets forth at least two different embodiments; one in which the initialization sequence is initiated by the memory controller and a second in which the initialization sequence is initiated by the controller circuit (by way of the memory module). Regardless of their specific distinctions, the ’837 patent presents embodiments (i) and (ii) as being both different and mutually exclusive—otherwise describing them in terms of a plurality of different examples makes no sense.¹³ (RX1587C at Q/A 208-210.) Given that the embodiments are distinct from one another and that independent claim 1 relates exclusively to embodiment (ii), an accused product embracing an alternative and unclaimed embodiment cannot include that claim limitation (much less infringe that claim). *See Johnson & Johnson Assocs. v. R.E. Serv. Co.*, 285 F.3d 1046, 1054-55 (Fed. Cir. 2002) (*en banc*) (per curiam) (explaining that even under the doctrine of equivalents “when a patent drafter discloses but declines to claim subject matter ... [it] dedicates that unclaimed subject matter to the public”).

Thus, the undersigned finds that the accused products do not include this feature of independent claim 1.

- d. “a notification circuit configured to drive the at least one output while the memory module is in the initialization mode to provide at least one notification signal to the memory controller indicating at least one status of the at least one initialization sequence”**

Complainant contends that the RCD includes an “ALERT_n pin” and that during operation the RCD creates an “ALERT_n signal.” Based on this operation, Complainant asserts

¹³ Buttredding this conclusion is the fact that the ’837 patent does not describe memory controller 14 and memory module 10 (upon which controller circuit 18 acts) as being synonymous. If such were the case, then a plausible argument could be made that embodiments (i) and (ii) are mere variants of one another.

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that the RCD corresponds to the claimed “notification circuit.”¹⁴ (CIB at 86.) Complainant further contends that this sequence occurs during the accused initialization mode (*i.e.*, the “Clock-to-CA” training mode). (*Id.*) Complainant also asserts that the “ALERT_n signal” provides notification to the memory controller regarding the status of the “Clock-to-CA” training mode and that both the memory controller and memory module remain in the initialization mode until signaled otherwise by the “ALERT_n signal.” (*Id.* at 86-88.) Complainant supports this contention by pointing to the fact that “ALERT_n signal” of the accused products “indicates to the memory controller (1) when the ‘eye opening’ has started, (2) when Clock-to-CA training is seeking the ending boundary of the ‘eye opening,’ and (3) when the ending boundary of the ‘eye opening’ has been found.” (*Id.* at 86-87.)

Respondents and Staff counter that the “ALERT_n signal” generated from the memory module of the accused products does not indicate a status of the “Clock-to-CA” training mode,” and that providing status information is within the exclusive province of the memory controller. (RIB at 118, RRB at 63-65, SIB at 118 and SRB at 38-39.) Indeed, Respondents and Staff both note that “only the memory controller”—as opposed to the memory module—is aware of the “Clock-to-CA” training mode status. (RIB at 118, RRB at 63, SIB at 118-119 and SRB at 38.) Respondents and Staff also contend that the “eye opening” communications provided by the “ALERT_n signal” are (i) merely feedback signals from the memory module to the memory controller and (ii) that the only signals it provides (*i.e.*, “LOW” or “HIGH”) do not indicate whether the initialization has started, is occurring or has ended. (RIB at 118, RRB at 63-64, SIB at 119, SRB at 38, RX-1587C at Q/A 238-242.) Respondents explain that the memory

¹⁴ As noted above, Complainant also contends that the RCD corresponds to the claimed “controller circuit.” (CIB at 84.)

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module “is merely a slave that samples whatever signal (HIGH or LOW) it receives from the memory controller and sends the sampled signal back,” and thereafter aggregates that information in order to manage the “Clock-to-CA” training mode. (RIB at 118 (*citing* RX-1587C at Q/A 235-48 and RRB at 64; *see also* SIB at 119 and SRB at 38.)

In addition to the above, Respondents further argue that the accused products do not include this claim feature because they do not exercise the “handshaking” aspect of the ’837 patent and, even assuming they do, that such involves “polling” as opposed to “notifying.”¹⁵ (RIB at 115.) Respondents contend that there is no “handoff” of control of initialization from the memory controller to the memory module. (*Id.* at 115-116 and RRB at 60.)

The undersigned agrees with Respondents and Staff that the “ALERT_n signal” generated from the memory module does not indicate a status of the “Clock-to-CA” training mode” and, instead, that only the memory controller provides status information regarding the initialization sequence.

As discussed above in conjunction with claim feature (c), the evidence of record demonstrates that the RCD of the accused devices does not “cause” the accused memory modules to enter the “Clock-to-CA” training mode; rather that occurs by way of the operation of the “memory controller.” In doing so, to be sure, the memory controller utilizes information from the memory module by way of the “ALERT_n signal” (*i.e.*, “eye opening” communications). (RX-1587C at Q/A 238-242.) However, that information is not “status” information pertaining to, for example, whether the initialization sequence has been executed, is currently being execute or is completed. (*See* JX-0006 at 6:51-7:3.) Rather, the information provided by the “ALERT_n

¹⁵ As was addressed *supra* in section VII.C.1, in connection with construction of the term “notification signal.”

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signal” signal is aggregated data points (*i.e.*, “LOW” or “HIGH”) that are feedback signals that (i) initiate with the memory controller, (ii) merely pass through memory module and (iii) return to the memory controller which then utilizes that information to determine a status of the initialization sequence. (RX-1587C at Q/A 238-242.) Put differently, these feedback signals passing through the memory module do not amount to a “status” until the memory controller utilizes them to make a status determination. By way of analogy, placing all of the ingredients (*i.e.*, “eye opening” communications from the “ALERT_n signal”) of a cake in a shopping bag (*i.e.*, the memory module) at the grocery store does not transform them into a cake; that only occurs when they are blended and transferred into the oven and baked (*i.e.*, the memory controller). As such, the accused notification signal (*i.e.*, the “ALERT_n signal”) generated from the accused notification circuit (*i.e.*, the RCD) does not provide a status of the accused initiation sequence (*i.e.*, the “Clock-to-CA” training mode) to the memory controller as asserted by Complainant.

In view of the forgoing, therefore, the undersigned finds that the accused products do not include this feature of independent claim 1.

e. “wherein the at least one notification signal triggers the memory controller to execute an interrupt routine”

Complainant argues that the accused products include a notification signal (*i.e.*, the “ALERT_n signal”) that “triggers” an “interrupt routine” by virtue of being communicated to the memory controller of the accused devices. (CIB at 88.) Complainant states that in assessing this claim feature it is “critical” to “determin[e] whether a memory controller is required to perform operations in response to the notification signal.” (*Id.* and CRB at 47.) Consistent with this position, Complainant asserts, citing Respondents’ expert (Wedig), that there are ten (10) operations the memory controller is required to perform in response to the “ALERT_n signal.” (CRB at 47-48.)

Respondents counter that Complainant has failed to carry its burden primarily because

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there has been no evidence adduced that (i) the “ALERT_n signal” from the RCD communicates information that effects an “interrupt” operation (or is even capable of doing so) and (ii) even if the “ALERT_n signal” does include an “interrupt” operation, that such causes the memory controller to execute an interrupt routine. (RIB at 112-113.) Respondents further note that the accused products do not even include memory controllers but instead operate in conjunction with memory controllers supplied by third parties, and there has been no evidence provided regarding how they operate (*e.g.*, in response to the “ALERT_n signal”). (*Id.* and RRB at 57-58.) In support of this contention, Respondents point out that Complainant’s expert (Mangione-Smith) testified that (i) he had not analyzed the functionality of any memory controllers *vis-à-vis* the accused products and (ii) that different memory controllers will operate and/or respond differently to signals depending upon how they are implemented. (RIB at 113 and RRB at 57 (citing Mangione-Smith, Tr. 408:1-16; 416:8-419:23; 421:13-24; 422:7-10).)

Staff generally concurs with Respondents. Namely, Staff agrees that Complainant has failed to set forth evidence that the accused notification signal (*i.e.*, the “ALERT_n signal”) communicates with the memory controller to trigger an interrupt routine. (SIB at 119-120 and SRB at 39-40.) Staff also relies on the testimony of Complainant’s expert (Mangione-Smith) as showing that there has been no analysis of any memory controllers in conjunction with accused devices in order to assess how the memory controllers respond to the “ALERT_n signal.” (SIB at 120.)

The undersigned agrees with Respondents and Staff. As detailed below, the evidence of record fails to establish (i) that the “ALERT_n signal” actually communicates or is even capable of communicating any information effecting a “interrupt” operation and (ii) assuming such a communication occurs, that it is directed to the memory controller such that the memory controller executes an interrupt routine.

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To begin with, Complainant's assertion that it is "critical" to "determin[e] whether a memory controller is required to perform operations in response to the notification signal" is not, as a general proposition, correct. Rather, the "critical" analysis is far narrower and is specifically directed to whether the accused notification signal "triggers the memory controller to *execute an interrupt routine*"—not "operations" generally—as is recited in independent claim 1.¹⁶ Within that context, Complainant's lack of proof with respect to this claim feature becomes evident.

As noted above, Respondents disagree with Complainant as to whether there are ten (10) operations the memory controller is required to perform in response to the "ALERT_n signal." The undersigned finds that there is no evidence that those operations are undertaken by the memory controller in response to the "ALERT_n signal." For example, the trial testimony of Respondents' expert (Wedig) relied upon by Complainant clearly indicates that the ten (10) operations undertaken by the memory controller when the accused initiation sequence (*i.e.*, the "Clock-to-CA" training mode) occurs. (Wedig, Tr. 721:12-17.) Respondents' expert does not indicate that those operations occur responsive to the "ALERT_n signal."

However, even assuming *arguendo* that those ten (10) operations are responsive to the "ALERT_n signal," there is no evidence that any, all or some subset thereof cause the memory controller to "execute an interrupt routine." Complainant does not appear to even make this argument, but rather simply argues that there no special meaning has been afforded to the term "interrupt routine." (CRB at 48.) That Complainant did not make this argument—or at least do so expressly—is consistent with the fact that even Complainant's own expert did not perform any analysis of memory controllers that operate in conjunction with the accused devices in order

¹⁶ As noted *supra* in section VII.C.1, Respondents' proposed construction using similarly broad language of the term "execute an interrupt routine" was rejected.

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to assess how the memory controllers actually respond to the “ALERT_n signal,” much less whether any such response(s) is an “interrupt routine.” (See Mangione-Smith, Tr. 408:1-19; 416:8-419:23; 421:13-24; 422:7-10.) Moreover, both Complainant’s expert and Respondents’ expert agreed that memory controllers can be designed to respond differently to an “ALERT_n signal. (See Mangione-Smith, Tr. 416:8-419:23; 421:13-24; 422:7-10; RX-1587C at Q/A 165, 181, 187, 191.) At most, therefore, there is evidence showing that as a general matter a memory controller *might* be capable of responding to “ALERT_n signal” in order to trigger an interruption routine if implemented by the manufacturer to do so. However, Complainant has made no specific evidentiary showing to that effect with respect to the accused products.

Thus, the undersigned finds that the accused products do not include this feature of independent claim 1.

f. Conclusion

For the reasons set forth above, the undersigned finds that the accused products do not infringe independent claim 1 of the ’837 patent.

2. Dependent Claims 2, 3, 5 and 6

“One who does not infringe an independent claim cannot infringe a claim dependent on (and thus containing all the limitations of) that claim.” *Wahpeton Canvas Co. v. Frontier, Inc.*, 870 F.2d 1546, 1552 n. 9 (Fed.Cir.1989). Given that the undersigned has found that independent claim 1 of the ’837 patent is not infringed, dependent claims 2, 3, 5 and 6 are also not infringed.

The undersigned notes that Respondents do not appear to dispute that the accused products include the additionally recited features of dependent claims 2, 3, 5, and 6 of the ’837 patent. (RIB at 120.) Thus, the determination of whether these dependent claims are infringed rises and falls solely with the determination of infringement as to independent claim 1.

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E. Domestic Industry – Technical Prong

Complainant asserts that its HybriDIMM products practice claims 1-3, 5 and 6 of the '837 patent.¹⁷ (CIB at 90-91.) Owing to their mutual compliance with the JEDEC specifications, the parties and Staff agree that there is no difference between the accused products and Complainant's HybriDIMM products for purposes of analyzing compliance with the technical prong of the domestic industry requirement. (*Id.*, CRB at 49, RIB at 125 and SIB at 121-122 and SRB at 40.) Therefore, the parties and Staff agree that the determination as to whether Complainant's HybriDIMM products establish the technical prong of the domestic industry requirement turns on the same analysis set forth above regarding whether the accused products infringe claims 1-3, 5 and 6 of the '837 patent. Given that the undersigned has determined that the accused products do not infringe claims 1-3, 5 and 6 of the '837 patent, the undersigned finds that Complainant's HybriDIMM products do not practice claims 1-3, 5 and 6 of the '837 patent for at least the same reasons for which the accused products do not infringe those claims.

Based on the foregoing, therefore, the undersigned finds that Complainant has failed to satisfy the technical prong of the domestic industry requirement for the '837 patent based on its HyperDIMM products.

F. Validity

1. Anticipation

a. Reference No. 1: SK Hynix DDR3 UDIMM

i. Waiver

Respondents contend that the SK Hynix DDR3 UDIMM ("DDR3") anticipates claims 1-3, 5 and 6 of the '837 patent under 35 U.S.C. §102. (RIB at 127.) In doing so, Respondents

¹⁷ Complainant does not assert that its HyperCloud products practice claims 1-3, 5 and 6 of the '837 patent. (*See also* SIB at 121, n. 16.)

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assert that Complainant has not disputed that the DDR3 qualifies as prior art under 35 U.S.C. §102. (*Id.* at 127-128.) Complainant, however, takes the opposite position and posits that the DDR3 is not prior art. (CIB at 92.) Respondents contend (i) that Complainant has waived this argument and (ii) that it has provided ample evidence that the DDR3 qualifies as prior art. (RRB at 69-71.) Staff has not taken a position on this issue.

Ground Rule 8.1(f) of this investigation provides, in relevant part, that the parties must submit a pre-hearing brief that includes “[a] statement of the issues to be considered at the hearing that *sets forth with particularity* a party's contentions on each of the proposed issues, including citations to legal authorities in support thereof.” (Order No. 2 (emphasis added).) Ground Rule 8.1(f) further provides that “[a]ny contentions not set forth in detail as required herein shall be deemed abandoned, or withdrawn, except for contentions of which a party is not aware and could not be aware in the exercise of reasonable diligence at the time of filing the pre-hearing statements.” (*Id.*) As argued by Respondents, Complainant’s pre-hearing brief does not set forth any argument with particularity that it planned to challenge whether the DDR3 qualifies as prior art to the ’837 patent. At most, Complainant’s pre-hearing brief states that “[t]he specific Hynix DDR3 UDIMM relied on by Respondents had model no. HMT125U7AFP8C and was *allegedly sold* in the United States to computer manufactures for slightly over 2 months in 2008.” (CPB at 400 (emphasis added).) Standing alone, that assertion fails “sets forth with particularity” Complainant’s positions as to whether the DDR3 qualifies as prior art. In addition, Complainant’s post-hearing brief does not allege that, at the time of filing the pre-hearing brief, it was unaware of or unable to ascertain facts during discovery to support this later-made argument with respect to the DDR3.

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Thus, the undersigned finds that Complainant has waived its arguments regarding whether the DDR3 qualifies as prior art with respect to the '837 patent.

ii. Analysis

Respondents contend that the DDR3 teaches all of the features of claims 1-3, 5 and 6 of the '837 patent. (RIB at 127.) The DDR3 is a memory device that utilizes “write-leveling” to temporally synchronize a memory controller’s clock signals and data strobe signals. (*Id.* at 126-127 and SIB at 123 (citing RX-0009C at Q/A 121).) Among other things, Respondents assert (i) that the DDR3 is a memory module, (ii) that the “MRS circuit” of the DDR3 corresponds to the claimed “controller circuit” and (iii) that the DDR3 “memory module creates the ‘notification signal’ by sampling the clock ‘CK’ at the rising edge of the data strobe signal” that is then “fed back to the memory controller using the data pin ‘DQ.’” (*Id.* at 129 and 133-134, RRB at 71-73 and RX-0009C at Q/A 174 (explaining that the “HMT125U7AFP8C discloses a “*memory module*,” under any construction....”).) Respondents also argue that if the accused products are found to infringe the '837 patent based upon the RCD/“Clock-to-CA” training mode, then the prior art “write-leveling” of the DDR3 should be found to anticipate the asserted claims of the '837 patent. (RIB at 125-126 and SIB at 123.) According to Respondents, this conclusion is necessary because the RCD of the accused products “is merely another version of the ‘analogous’ functionality in DDR3, known as write leveling.” (RIB at 125 (*citing* RX-1587C at Q/A 256; RX-0009C at Q/A 16 and RX-0320.066).)

Complainant and Staff argue that the DDR3 fails to teach the following features of independent claim 1: (i) “a controller circuit configured to cause the memory module to enter the initialization mode” and (ii) “a notification circuit configured to drive the at least one output while the memory module is in the initialization mode to provide at least one notification signal

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to the memory controller indicating at least one status of the at least one initialization sequence.”¹⁸ (CIB at 93-96, CRB at 50-53, SIB at 123-124 and SRB at 40-41.)

According to Complainant and Staff, the DDR3 includes multiple memory elements (*i.e.*, DRAMs) each of which includes an MRS circuit (*i.e.*, the “memory controller”) embedded therein that operates exclusively with the DRAM with which it associated. (CIB at 93, CRB at 50, SIB at 123 and SRB at 41.) As such, Complainant and Staff argue that no single MRS circuit can cause an unassociated DRAM, much less the memory module as a whole, to take any specific action (*e.g.*, to enter an initialization mode and/or “write-leveling”). (CIB at 93, CRB at 50, SIB at 123 and SRB at 41.) Complainant and Staff make a similar argument regarding the “notification circuit;” namely that the DRAMs each include an associated “notification circuit” that does not operate on an unassociated DRAM or the memory module as a whole, and therefore cannot provide a “notification signal” to the memory module. (CIB at 95-96, CRB at 53, SIB at 124 and SRB at 41.)

With respect to Complainant’s and Staff’s contentions, Respondents argue that these positions advance a new claim construction that requires “a single controller circuit” and that “[t]here is no requirement that a single controller circuit puts every DRAM into write leveling mode....” (RRB at 71-72.) Respondent makes a similar argument with respect to the “notification circuit.” (*Id.* at 73.)

The undersigned agrees with Complainant’s and Staff. Independent claim 1 recites, in relevant part, “[a] memory module comprising a controller circuit configured to cause the

¹⁸ Complainant’s Post-Hearing Reply Brief further claims that the DDR3 does not disclose a notification signal that “trigger[s]...an interrupt routine” because it does not teach a “notification signal.” (CRB at 52-53.) This particular argument is not set forth in Complainant’s initial Post-Hearing Brief.

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memory module to enter the initialization mode.” Respondents’ expert (Wedig) testified that no single MRS circuit can “write-level” the DDR3:

Q And you agree that the MRS circuit on one DRAM chip cannot perform write leveling on any other DRAM chip; correct?

A That's correct. While the -- while the write leveling is going on on one, all the others are disabled, so they're not -- they're not being used.

Q Thank you. And no MRS circuit on a DRAM chip can write level the full UDIMM device; correct?

A No, each -- each MRS circuit write levels its own DRAM chip, while the others are silent, while the others are disabled, and then you go through and you -- and then you do each one individually.

(Wedig, Tr. at 750:25-751:12.) Thus, no one of the MRS circuits can cause the DDR3 memory module to enter the alleged initialization mode. Rather, for the DDR3 to enter “write-leveling,” it is necessary for the plurality of MRS circuits to all communicate that instruction to their associated DRAMs. In order to arrive at the conclusion Respondents’ urge, therefore, it necessarily requires establishing that the plurality of MRS circuits of the DDR3 act as a single “controller circuit” for the DDR3 to arrive at the recited outcome (*i.e.*, to enter the initialization mode). (See CX-0931C at Q/A 1074-1075.)

In framing the issue in that manner, Respondents contend that Complainant is advocating a new claim construction, and the undersigned would agree that do so would be improper at this stage of the proceedings. However, Respondents’ argument inherently raises an issue pertaining to the *number* of controller circuits that independent claim 1 implicates, both in terms of scope (*i.e.*, the number allowed) and requirement (*i.e.*, the minimum number and type required). By virtue of using the “comprising” transition phrase, independent claim 1 does not on its face limit

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itself to a single controller circuit.¹⁹ (See RX-0009C at Q/A 197.) It does, however, require there to be at least one “controller circuit *configured to cause the memory module to enter the initialization mode.*” (Emphasis added).

As noted above, there is ample evidence—including from Respondents’ own expert (Wedig)—that individual MRS circuits in each of the DRAMs cannot make the DDR3 (*i.e.*, the “memory module”) enter “write-leveling.” (See CX-0931C at 1082 (discussing Wedig witness statement).) Therefore, the question Respondents failed to adequately address is whether the plurality of MRS circuits should be collectively treated as the required “controller circuit” that causes the DDR3 (*i.e.*, the memory module)²⁰ to enter “write-leveling” (*i.e.*, the initialization mode) given that none of the MRS circuits can do so individually. Indeed, the evidence is absent. Respondents instead offer case law arguments regarding the interpretation of the terms “a,” “an,” “one or more” and “comprising.” (RIB at 131-132 and RRB at 71-72.)

On the other hand, there is evidence that the individual MRS circuits in each of the DRAMs does not interact with other MRS circuits or other non-associated DRAMS. (Wedig, Tr. at 750:25-751:5.) Under such circumstances, the individual MRS circuits can hardly be considered as working collectively as a single “controller circuit” regardless of whether they are individually each doing the same thing. Moreover, the evidence shows that each MRS circuit only causes its associated DRAM to enter “write-leveling” and that the memory module is considered to enter “write-leveling” only after all of the individual DRAMs have done so. (Wedig, Tr. at 751:7-12.) Thus, even assuming *arguendo* that the operations of the “plurality

¹⁹ The undersigned takes no position on whether Complainant’s arguments regarding independent claim 1 will, in other contexts, serve to limit the scope of that claim and the claims depending therefrom.

²⁰ It should be noted that Respondents identified the DDR3—not the individual DRAMs disposed thereon—as corresponding to the “memory module.” (See RX-0009C at Q/A 174.)

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components” (e.g., the MRS circuits and the DRAMs) of the DDR3 were considered a single operation/component with respect to the memory module, it would be the collective action of the DRAMs that causes the DDR3 memory module to enter “write-leveling” not the collective action of the MRS circuits.

For the same reasons outlined above, the DDR3 also fails to teach a “notification circuit” and also cannot, therefore provide a “notification signal” to the memory module.

In view of the forgoing, the undersigned finds that the SK Hynix DDR3 UDIMM does not anticipate independent claim 1 or the claims depending therefrom, including asserted dependent claims 2, 3, 5 and 6, of the '837 patent under 35 U.S.C. §102.

b. Reference No. 2: JEDEC Standard (JESD79-3)

Respondents contend that the JESD79-3 teaches all of the features of claims 1-3, 5 and 6 of the '837 patent, and comingles that argument with the argument above for the DDR3 because “[t]he DDR3 UDIMM [] follows the JESD79-3 standard for write-leveling....” (RIB at 127.) In other words, Respondents appear to assert JESD79-3 is anticipatory for the same reasons asserted for the DDR3. (RX-0009C at Q/A 116-120 and 145-149; CX-0931C at Q/A 1148-1153; Wedig, Tr., 751:17-752:11.) Complainant and Staff each contend that the invalidity analysis for JESD79-3 is the same as DDR3. (CIB at 98-99, CRB at 54, SIB at 125 and SRB at 41.) Complainant further asserts that JESD79-3 fails to teach a “memory module.” (CIB at 98-99 and CRB at 54.) Respondents disagree with Complainant’s latter point regarding the “memory module.” (RRB at 75.)

Given that Respondents do not address JESD79-3 separately from DDR3, the undersigned agrees with Complainant and Staff that that the invalidity analysis for JESD79-3 is the same as DDR3. Accordingly, the undersigned finds that JESD79-3 does not anticipate

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independent claim 1 or the claims depending therefrom, including asserted dependent claims 2, 3, 5 and 6, of the '837 patent under 35 U.S.C. §102.²¹

c. Reference No. 3: U.S. Patent Application Publication No. 2005/0071580 to LeClerc *et al.* (“LeClerc”)

Respondents contend that the LeClerc teaches all of the features of claims 1-3, 5 and 6 of the '837 patent. (RIB at 137-138.) Among other things, Respondents assert that LeClerc teaches (i) a “memory initialization” corresponding to the claimed “initialization mode,” (ii) a “normal mode of operation” corresponding to the claimed “operational mode,” (iii) an “initialization/test controller 304” corresponding to the claimed “controller circuit,” (iv) a “bus interface 302” corresponding to the claimed “notification circuit” whose output constitutes a “notification signal,” and (v) that the “notification signal” is sent to the memory controller causing the processor to enter a testing protocol. (RIB at 138-142 and RRB at 75-77.) Respondents further support these contentions based upon the Patent Trial and Appeal Board’s decision to initiate review of the '837 patent based upon LeClerc. (RIB at 138-142 (*citing SK Hynix, Inc. v. Netlist, Inc.*, IPR2017-00548, Institution Decision, Paper No. 7 (May 15, 2017)).)

Complainant and Staff argue independent claim 1 of the '837 patent requires two separate operating modes: an initialization mode (during which an initialization sequence occurs) and an operational mode. (CIB at 100, CRB at 54, SIB at 126 and SRB at 42) Complainant and Staff then assert that the evidence of record illustrates that the memory module of LeClerc operates in only two modes: (i) a low powered sleep mode during which no operations occur and (ii) a normal power mode, during which the “memory initialization” occurs. (CIB at 99, CRB at 54-56, SIB at 126-127, SRB at 42 (each citing the witness statement of Complainant’s expert

²¹ The undersigned takes no position on whether JESD79-3 teaches a memory module given that there is no need to reach that issue.

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(Murphy) CX0931C at Q/A 1231-1236.) According to Complainant and Staff, therefore, LeClerc cannot anticipate because the cited “memory initialization” occurs during the “operational mode” contrary to independent claim 1. Complainant notes that LeClerc “does not disclose any operative mode that ‘is performed separate from the operational mode.’” (CRB at 55; *see also* CIB at 100-101 and CX0931C at Q/A 1236.)

In addition to citing Complainant’s expert (Murphy), Complainant and Staff further rely on the testimony of Respondents’ expert (Wedig) to support these positions. In particular, Respondents’ expert agreed (i) that independent claim 1 requires an initialization mode (during which an initialization sequence occurs) and a separately occurring operational mode²²:

Q You agree that the proper construction of the term “initialization mode” makes clear that the initialization mode is performed separate from the operational mode; correct?

A Correct.

Q And you agree that in the context of the '837 patent, and particularly claim 1, the initialization mode and operational mode cannot be performed simultaneously; correct?

A Yeah, that's correct. It makes no sense, because how can you operate until you're initialized?

(Wedig, Tr. 753:5-15), and (ii) that the initialization steps of LeClerc occur after it leaves the low-power sleep mode and enters the normal operations mode:

Q Okay. And you have not contended that LeClerc performs initialization in the low-power mode, have you?

A No, I have not said that. As I said, it does it after it comes out of low-power mode.

²² Respondents’ expert (Wedig) agreed that “the operational mode that's claimed in claim 1 of the '837 patent is basically a normal mode of operation.” (Wedig, Tr. 761:8-11; *see also* 761:12-14.)

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(*Id.* at 753:1-4.) Complainant and Staff thereafter posit that because LeClerg lacks an initialization mode separate from the operational mode, then it necessarily fails to teach (i) a “controller circuit” that causes the memory module to enter the initialization mode and (ii) a “notification circuit” producing a “notification signal” indicative of one status of the initialization sequence and (iii) that the “notification signal” trigger an interrupt routine. (CIB at 101-102, CRB at 57, SIB at 126-127, SRB at 42.)

Respondents disagree with Complainant and Staff, and argue that LeClerg is being “mischaracterized” because “[w]hile *LeClerg* does mention a “low power mode” or “sleep mode,” the term “normal mode” or “operation mode” does not exist in the reference.” (RRB at 76.) In doing so, Respondents also contend that “*LeClerg* discusses a ‘full initialization’ as a separate state of operation after the system is revived from sleep mode.” (CRB at 76.) Thus, Respondents intimate that LeClerg includes a mode other than the low-powered sleep mode and the operational mode.

The undersigned agrees with Complainant and Staff. Both private parties’ experts testified that the initialization steps of LeClerg occur outside of the low-powered sleep mode. (Wedig, Tr. at 753:1-4 and CX0931C at Q/A 1231-1236.) Thus, the issue is whether the initialization steps of LeClerg occur in an “initialization mode” separate from the normal operation mode which, again, both parties’ experts agree is a requirement. (Wedig, Tr. at 753:5-15 and CX0931C at Q/A 1236.) Respondents have failed to show that LeClerg provides such a teaching.

As noted above, Respondents argue that adopting this position is incorrect because (i) it “mischaracterizes” LeClerg because it does not mention a “normal mode” or an “operational mode” and (ii) the “full initialization” mode of LeClerg is “a separate state of operation after the system is revived from sleep mode.” CRB at 76. Both of these positions are unavailing.

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With respect to point (i), Respondents contradict themselves. The question is not whether LeClerg uses specific language; rather the question is what LeClerg does and does not teach. Lest there be any question as to the *teachings* of LeClerg, Respondents expressly state that LeClerg teaches a normal mode of operation despite the fact that it apparently does not “mention” the term “normal mode.” (RIB at 139.) Moreover, Respondents contend that this description of a “normal mode” corresponds to the recited “operational mode.” (*Id.*) Respondents also acknowledge that LeClerg teaches a low-powered sleep mode, and apparently do not contest that no operations occur during the low powered sleep mode. (RRB at 76.) Thus, there is no mischaracterization involved in concluding that the memory module of LeClerg operates in only two modes: (i) a low powered sleep mode during which no operations occur and (ii) a normal power mode, during which the “memory initialization” occurs.

Given that Respondents’ expert (Wedig) agreed that the “initialization mode” of independent claim 1 of the ’837 patent is separate from the “operational mode, (Wedig, Tr. 753:5-9), point (ii) is equally unavailing because it is therefore premised on the notion that LeClerg includes a mode during which initiation steps occur and which is separate from the low-powered sleep mode and the operational mode. In doing so, Respondents overlook that their own expert agreed with Complainant’s and Staff’s characterization of LeClerg as teaching only two modes, and Respondents conspicuously fail to cite to any evidence of record that clearly and convincingly establishes the presence of another mode. Rather, based on the evidence of record LeClerg appears to teach, as stated succinctly by Complainant’s expert (Murphy), “a single mode during which two different procedures or processes can occur.” (CX0931C at Q/A 1236.) That description of the LeClerg contrasts with the recitation of independent claim 1, and therefore cannot anticipate it.

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In view of the forgoing, the undersigned finds that LeClerg does not anticipate independent claim 1 or the claims depending therefrom, including asserted dependent claims 2, 3, 5 and 6, of the '837 patent under 35 U.S.C. § 102.

2. Obviousness

- a. **LeClerg in view of (i) U.S. Patent Application Publication No. 2005/0193161 to Lee *et al.* (“Lee”) and (ii) U.S. Patent No. 8,359,521 to Kim (“Kim”).**

Respondents contend that claims 1-3, 5 and 6 of the '837 patent are obvious under 35 U.S.C. § 103 based upon the combined teachings of LeClerg and Lee (claims 1-3 and 6) and LeClerg and Kim (claim 5). (RIB at 144-147, RRB at 77-79.) Respondents make these arguments in the alternative in the event, as is the case, the undersigned determines that LeClerg does not anticipate these claims under 35 U.S.C. § 102. (RIB at 142.)

Respondents rely on LeClerg as teaching all of the features of independent claim 1²³ as set forth in their anticipation contentions except that “the at least one notification signal triggers the memory controller to execute an interrupt routine.” (RIB at 144-145.) Respondents apparently rely on Lee as supplying this deficiency. (*Id.*) In doing so, however, Respondents never clearly set forth exactly what teaching from Lee they are relying on and instead focus exclusively on teachings from LeClerg. (*Id.*)

With respect to dependent claim 5, Respondents rely on Kim only as teaching a single pin to report initialization errors. (*Id.* at 146-147 and RRB at 78-79.) In doing so, Respondents are

²³ Respondents assert that LeClerg teaches the features of dependent claims 2, 3 and 6, and contends that because they are purportedly anticipated by LeClerg they must also be rendered obvious by the combination of LeClerg and Lee as applied to independent claim 1. (RIB at 146.)

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therefore relying on LeClerg as teaching all of the features of independent claim 1 from which claim 5 depends.²⁴

Even assuming *arguendo* that Lee and Kim supply the deficiencies for which Respondents rely upon them—and as noted above it is not exactly clear what teaching from Lee Respondents are relying upon—those teachings do not supply the deficiencies of LeClerg that prevent it from anticipating claims 1-3, 5 and 6 of the '837 patent. Put differently, Lee and Kim have not been asserted by Respondents as curing the deficiencies of LeClerg described above. Therefore, the combined teachings of LeClerg, Lee and/or Kim cannot establish a *prima facie* case of obviousness as to independent claim 1 or the claims depending therefrom, including dependent claims 2, 3, 5 and 6, under 35 U.S.C. §103.

In view of the above, the undersigned finds that LeClerg, Lee and/or Kim do not render obvious independent claim 1 or the claims depending therefrom, including instantly asserted dependent claims 2, 3, 5 and 6, of the '837 patent under 35 U.S.C. §103. In addition, because the undersigned finds that claims 1-3, 5 and 6 of the '837 patent are not obvious, it is unnecessary to address the sufficiency of Complainant's evidence of secondary considerations of non-obviousness. (CRB at 58.)

VIII. U.S. PATENT NO. 8,516,185

A. Overview

1. Asserted Claims

Complainant alleges infringement of claims 1-3, 7, 8 and 10-12 of the '185 patent. Claims 2, 3, 7, 8 and 10-12 depend from independent claim 1. The asserted claims provide as follows:

²⁴ It should be noted that Respondents did not argue that dependent claim 5 was obvious based upon the combination of LeClerg, Lee and Kim. (RIB at 146.)

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1. A memory module comprising:

a plurality of memory devices;

a controller configured to receive control information from a system memory controller and to produce module control signals; and

a plurality of circuits configured to receive the module control signals,

each circuit of the plurality of circuits having a first bit width and operatively coupled to at least two corresponding memory devices of the plurality of memory devices, the at least two corresponding memory devices each having a second bit width smaller than the first bit width,

each circuit of the plurality of circuits comprising

at least one write buffer and

at least one read buffer and

configured to selectively allow data transmission between the system memory controller and at least one selected memory device of the at least two corresponding memory devices in response to the module control signals, and

to selectively isolate at least one other memory device of the at least two corresponding memory devices from the system memory controller in response to the module control signals,

wherein each circuit of the plurality of circuits is operable, in response to the module control signals,

to actively drive write data from the system memory controller to the at least one selected memory device of the at least two corresponding memory devices through the at least one write buffer, and

to receive and drive read data from the at least one selected memory device of the at least two corresponding memory devices to the system memory controller through the at least one read buffer,

wherein the circuits of the plurality of circuits are distributed at corresponding positions separate from one another.

* * * * *

2. The memory module of claim 1, wherein the plurality of circuits is contained

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in a plurality of packages at locations spaced from one another.

* * * * *

3. The memory module of claim 2, wherein the plurality of memory devices, the controller, and the plurality of circuits are mechanically coupled to a printed circuit board having an edge, wherein the packages are positioned along the edge and between the edge and the plurality of memory devices.

* * * * *

7. The memory module of claim 1, wherein the memory module is a dual in-line memory module.

* * * * *

8. The memory module of claim 1, wherein the plurality of memory devices comprise one or more synchronous dynamic random access memory devices.

* * * * *

10. The memory module of claim 1, wherein the controller is configured to control the plurality of circuits using a Column Access Strobe (CAS) latency parameter.

* * * * *

11. The memory module of claim 1, wherein the module control signals include first indication of a direction of data flow and second indication of whether a first group of the plurality of memory devices or a second group of the plurality of memory devices are being accessed.

* * * * *

12. The memory module of claim 1, further comprising module control signal lines extending across a substantial portion of the memory module, wherein the controller transmits the module control signals over the module control signal lines, and wherein the plurality of circuits are distributed along the module control signal lines and receive the module control signals via the module control signal lines.

(JX-0002 at Cls. 1-3, 7, 8 and 10-12.)

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B. Level of Ordinary Skill in the Art

Complainant contends that a person of ordinary skill in the art with respect to the '185 patent “would have an electrical or computer engineering background, and specifically, a Bachelor’s degree in electrical engineering, computer engineering, or in a related field and at least one—and preferably two—years of work experience relating to memory systems.” (CIB at 107 (citing CX-0930C at Q/A 87; Baker, Tr. at 993:11-998:7).)

Respondents alternatively argue that a person with an appropriate level of skill in the art with respect to the '185 patent has “an advanced degree in electrical or computer engineering and *two years* working in the field, or a bachelor’s degree in such engineering disciplines and at least *five years* working the field.” (RIB at 11 (citing RX-0006C at Q/A 49) (emphasis in original).)

Staff asserts that Complainant’s proposed definition be adopted because “Respondents’ proposed definition of ordinary skill requires an amount of experience that appears to the Staff to be much greater than warranted.” (SIB at 132.) Staff further notes that “the differences in the proposed definitions do not appear to be significant enough to change or materially alter the parties’ positions.” (SIB at 133.) Staff also points out that “the parties generally agree that the differences in their proposed definitions of ordinary skill would not change their positions on the issues to be decided in this investigation.” (SRB at 44 (citing CIB at 107-108; RIB at 11; SIB at 131-133; CX-0004C at Q/A 66, 68; CX-0930C at Q/A 88-89; and RX-1584C at Q/A 19-21).)

Given (i) the evidence of record cited above by the parties and Staff and (ii) that the parties’ positions would not be changed or materially altered under either of the proposed definitions, the undersigned finds that the level of ordinary skill in the art for the '185 patent is consistent with the definition proposed by Complainant and Staff which is a person “hav[ing] an electrical or computer engineering background, and specifically, a Bachelor’s degree in electrical

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engineering, computer engineering, or in a related field and at least one—and preferably two—years of work experience relating to memory systems.”

C. Claim Construction

There is only one disputed claim term relevant to the asserted claims of the '185 patent: “selectively isolate.” (CIB at 108-109, CRB at 58-59, RIB at 12-14, RRB at 4-5, SIB at 133-136 and SRB at 44-45.) The term “selectively isolate” appears in independent claim 1 from which claims 2, 3, 5, 7, 8 and 10-12 depend. The parties propose the following respective constructions for this term:

<i>“selectively isolate”</i>		
Complainant’s Proposed Construction	Respondents’ Proposed Construction	Staff’s Proposed Construction
plain and ordinary meaning	“selectively electrically separating one component from another”	plain and ordinary meaning

(SIB at 133 and SRB at 44; *see also* CIB at 108; RIB at 12.)

The parties and Staff agree that the term “selectively isolate” should be interpreted consistent with its plain and ordinary meaning. (CIB at 108, CRB at 59, RIB at 12, RRB at 4, SIB at 133 and SRB at 44-45.) Neither the parties nor the Staff suggests that the '185 patent provides an express definition or ascribes a “special meaning” to the term “selectively isolate.” Complainant and Staff disagree, however, with Respondents as to what that plain and ordinary meaning is. Staff and (presumably) Complainant is of the opinion that the plain and ordinary meaning of “selectively isolate” is “selectively isolate.” Respondents, based upon the '185 patent specification, prosecution history, the trial testimony of Complainant’s expert (Baker), are of the view that the plain and ordinary meaning is “selectively electrically separating one component from another.” The parties’ and Staff’s positions are addressed below in more detail.

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Complainant asserts that the term “selectively isolate” should be given its plain and ordinary meaning based upon the testimony of its experts (Brogioli and Baker) which, in turn, is based upon their review of the specification and prosecution file history of the ’185 patent. (CIB at 108 (*citing* CX-0004C at Q/A 105-06; CX-0930C at Q/A 133).) Complainant offers no further support justifying its proposed construction (*e.g.*, direct citation to portions of the ’185 patent specification or its prosecution file history) or, for that matter, expressly states what it considers the plain and ordinary meaning to actually be. Rather, Complainant focuses on the purported deficiencies of Respondents’ proposed construction. (CIB at 108 and CRB at 59.)

Specifically, Complainant contends that Respondents’ construction is flawed because it adopts a construction from the PTAB to which redundant language (*i.e.*, “selectively”) is added to produce a phrase that when read in view of the remainder of the claim does not further clarify the term at issue but rather reiterates features already set forth in the claim. (CIB at 108.) Complainant further notes that Respondents’ proposed construction lacks credibility given that “Respondents failed to provide any invalidity analysis using their own construction for at least the following prior art references: Shau, Rajan, SK hynix DDR2 RDIMM, and Solomon.” (RIB at 108-109 (emphasis in original).) Complainant concedes, however, that there would be “no material impact on infringement, technical domestic industry, or validity” if Respondents’ construction were adopted. (CIB at 108-109.)

As noted above, Respondents posit that the plain and ordinary meaning of “selectively isolate” is “selectively electrically separating one component from another.” (RIB at 12.)²⁵ According to Respondents, “[t]he specification teaches that isolating means electrically

²⁵ Respondents note that neither Complainant nor Staff explains what the plain and ordinary meaning of “selectively isolate” actually is. (RIB at 12 and RRB at 4.)

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separating.” RIB at 12. Respondents cite to the following portion of the ’185 patent in support of this contention:

This advantageous result is desirably achieved in certain embodiments by using the data transmission circuits 416 to electrically couple only the enabled memory devices 412 to the memory controller 420 (e.g., the one, two, or more memory devices 412 to which data is to be written) and to electrically isolate the other memory devices 412 from the memory controller 420 (e.g., the one, two, or more memory devices 412 to which data is not to be written).

(JX-0002 at 14:34-42.) Respondents then assert that a specific amendment during prosecution of the ’185 patent supports its proposed claim construction. (RIB at 13.)

Staff contends the term “selectively isolate” should be given its plain and ordinary meaning of “selectively isolate.” (SIB at 133-136 and SRB at 44-45.) Staff argues that this construction is proper based upon the ’185 patent specification and despite the claim amendment and arguments made during prosecution cited by Respondents. (SIB at 134-136.) In particular, Staff contends that the prosecution amendment cited by Respondents did not directly or indirectly limit the scope of the term “isolate” such that it would be limited to “electrical separation.” (*Id.* at 135.) Staff also asserts that Respondents’ proposed construction is redundant and largely unnecessary because it adopts language and concepts expressly recited in independent claim 1 and also is overly restrictive. (*Id.* at 133-135.) However, in reply briefing, Staff has also asserted that, although it believes the term “selectively isolate” should be given its plain and ordinary meaning, it no longer objects to Respondents’ proposed construction because Complainant’s expert (Baker) testified that “isolation always requires electrical separation.” (SRB at 45.)

Based on the forgoing and the evidence of record there are deficiencies with the proposed constructions by the parties and Staff.

To begin with, the parties’ analysis of the intrinsic evidence in support of their proposed constructions is severely lacking despite the fact that “the specification ‘is always highly relevant

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to the claim construction analysis. Usually, it is dispositive; it is the single best guide to the meaning of a disputed term.” *Phillips*, 415 F.3d at 1315 (citing *Vitronics*, 90 F.3d at 1582). Indeed, by way of “analysis” the parties provide little more than citations to portions of the ’185 patent and its file history—without significant analysis—before segueing into their criticisms of the opposing side’s construction. For example, Complainant’s entire analysis of the evidence supporting its claim constructions is two sentences; the rest is a critique of Respondents’ proposed construction. (CIB at 108.) Respondents provide little more, but do include an illustration and three sentences discussing a purportedly significant claim amendment and supporting argument from the prosecution file history of the ’185 patent.

First, it seems to have been overlooked that (i) the parties and Staff all agree that any construction of the term “selectively isolate” includes the word “selectively” and (ii) there is no dispute as to what “selectively” means. As such, common sense dictates that any construction of the term “selectively isolate” should include the word “selectively.” Put differently, and based on the positions adopted by the parties and Staff, the term in dispute is “isolate,” not “selectively isolate.”

Second, the express language of independent claim 1 provides that “each circuit of the plurality of circuits...[is] operatively coupled to at least two corresponding memory devices” and that the “at least two corresponding memory devices” are “configured” (i) “*to selectively allow data transmission between the system memory controller and at least one selected memory device*” (which for convenience can be called a “first” memory device) and (ii) “*to selectively isolate at least one other memory device of the at least two corresponding memory devices* from the system memory controller” (which for convenience can be called an “other” memory device(s) different from the “first” memory device). As can be seen from this breakdown, the claim language already embraces the concept of “separating one component from another” as set forth in Respondents’ proposed

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construction. That is, the claim plainly distinguishes the “first” memory device from the “at least one *other* memory device.” Therefore, it is unnecessary to adopt this portion of Respondents’ proposed claim construction language (*i.e.*, “separating one component from another”) purporting to differentiate claim components given that the claim already distinguishes them.

Therefore, as noted above, claim construction for the ’185 patent distills down to determining the meaning of the term “isolate” and, in particular, whether the term “isolate” should be construed to mean “electrically separate.” (SIB at 134.) In this regard, the actual language of independent claim 1 and the ’185 patent specification provides guidance.

The above-discussed claim language makes clear that the “first” memory device is in communication with the system memory controller while the “other” memory device is “selectively isolated” from the system memory controller. According to the ’185 patent, the memory controller of conventional/prior art memory systems sees “all the memory devices” as its load during write operations and that such causes performance deficiencies. (JX-0002 at 4:47-52; 4:65-5:4; 5:41-46; 5:59-65.) In contrast, a purported beneficial aspect of the inventive subject matter of the ’185 patent is

[t]o reduce the memory device loads seen by the system memory controller 420 (e.g., during a write operation), the data transmission circuit 416 of certain embodiments is advantageously configured to be recognized by the system memory controller 420 as a single memory load. This advantageous result is desirably achieved in certain embodiments by using the data transmission circuits 416 to electrically couple only the enabled memory devices 412 to the memory controller 420 (e.g., the one, two, or more memory devices 412 to which data is to be written) and to electrically isolate the other memory devices 412 from the memory controller 420 (e.g., the one, two, or more memory devices 412 to which data is not to be written). Therefore, during a write operation in which data is to be written to a single memory device 412 in a rank of the memory module 400, each data bit from the system memory controller 420 sees a single load from the memory module 400, presented by one of the data transmission circuits 416, instead of concurrently seeing the loads of all of the four memory devices 412A, 412B, 412C, 412D to which the data transmission circuit 416 is operatively coupled. In the example of FIG. 3A, during a write operation in

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which data is to be written to two memory device 412 in two ranks (e.g., memory devices 412A and 412C or memory devices 412B and 412D), each data bit from the system memory controller 420 sees a single load from the memory module 402, which is presented by one of the data transmission circuits 416, instead of concurrently seeing the loads of all of the four memory devices 412A, 412B, 412C, 412D to which the data transmission circuits 416 is operatively coupled. In comparison to the standard JEDEC four-rank DIMM configuration (see FIG. 2A and FIG. 2B), the memory system 402 of certain embodiments may reduce the load on the system memory controller 420 by a factor of four.

(JX-0002 at 14:30-62.) As is plainly described in the '185 patent, at least one advantageous aspect of the disclosed subject matter is the ability to reduce the load on the memory controller by presenting only the load from specifically coupled and enabled memory devices while “electrically isolating” other non-enabled memory devices even though all of the memory modules remain “operatively coupled.” In other words, “selectively isolate” conveys that during a write operation a “selected” subset of the memory modules are electrically separated from the memory controller thereby reducing the load upon the memory controller even though the “electrically isolated” memory modules are still “operatively coupled” to the memory controller. Thus, the intrinsic evidence establishes that the term “isolate” refers to “electrically isolating” or “electrically separating.”

Extrinsic evidence also supports this conclusion. On the one hand, Complainant’s expert (Baker) testified that “isolation always requires electrical separation.” (Baker, Tr. 1015:21-23.) On the other, Respondents urge that “[t]he specification teaches that isolating means electrically separating.” (RIB at 12.) Staff appears to accede to this position as well. (SRB at 45.)

In view of the forgoing, therefore, the undersigned finds that the term “selectively isolate” should be construed as “*selectively electrically separate.*”

D. Infringement

1. Independent Claim 1

a. Undisputed Features

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Complainant contends that there is no disagreement that “all claim limitations except the ‘Selective Allowance’ and ‘Selective Isolation’” features can be found in the accused LRDIMM products (“LRDIMM”) because the LRDIMM “control[] the timing and directionality of data transmission to and from the DRAM memory devices....” (CIB at 110-111 and CRB at 60.) Complainant cites to the written testimony of its expert to fulfill its obligation in establishing that accused products include the various features of independent claim 1. (CIB at 110 (citing CX-0004C at Q/A 426-466, 483-502.) Respondents and Staff do not appear to dispute this evidence and Complainant’s contention, but instead focus only on whether the LRDIMM includes the “Selective Allowance” and “Selective Isolation” features. (RIB at 14-18, RRB at 5-11, SIB at 137-140 and SRB at 45-47.)

In view of the testimony of Complainant’s expert that the LRDIMM include all of the features of independent claim 1 except “Selective Allowance” and “Selective Isolation” features, and there being no clear disagreement by Respondents and Staff as to that fact, the undersigned finds that the LRDIMM includes these features (*i.e.*, all of the features except the “Selective Allowance” and “Selective Isolation” features) of independent claim 1. *See* CX-0004C at Q/A 426-466, 483-502.

b. Disputed Features

As noted above, Respondents and Staff disagree with Complainant that the LRDIMM includes the “Selective Allowance” and “Selective Isolation” features. As discussed below in more detail, the undersigned finds that the LRDIMM does not include either the “Selective Allowance” or the “Selective Isolation” feature.

iii. “Selective Allowance”

Independent claim 1 recites, in relevant part, that each of the plurality of circuits is configured “to selectively allow data transmission between the system memory controller and at least one

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selected memory device of the at least two corresponding memory devices in response to the module control signals.” Complainant argues that the term “selectively allow” includes “selecting” the timing and “direction” (*i.e.*, reading or writing data) based upon two excerpts of the ’185 patent:

- “As is known, Column Address Strobe (CAS) latency is a delay time which elapses between the moment the memory controller 420 informs the memory modules 402 to access a particular column in a selected rank or row and the moment the data for or from the particular column is on the output pins of the selected rank or row. The latency may be used by the memory module to control operation of the data transmission circuits 416.” (JX-0002 at 15:29-36); and
- “The control signals indicate, for example, the direction of data flow, that is, to or from the memory devices 412, 412’.” (JX-0002 at 10:23-24.)

(CRB at 60-61 and CIB at 112-113.) Thus, the ’185 patent specification does indicate that timing (*i.e.*, latency) and direction can be used to control data transmission.

According to Complainant, the accused LRDIMM includes data buffers (“DBs”), and that “the DB controls data transmission according to the direction of data (*e.g.*, read, write) and timing (*e.g.*, rank-specific timing, CAS latency, etc.) and therefore satisfies the ‘selectively’ requirement of claim 1 in multiple ways.” (CIB at 112.) For example, Complainant asserts that in the LRDIMM “the DB performs rank-specific timing adjustment based on which rank (*e.g.*, group) of memory devices is selected to ensure that data will be transmitted to or received from the selected memory devices correctly.” (*Id.* at 113 (citing CX-0004C at Q/A 272-85, 475; Subramanian, Tr. at 675:1-685:4).) Complainant similarly cites other operations of the DBs of the LRDIMM purporting to demonstrate that the DBs “selectively allow data transmission.” (*Id.* at 111-17.)

Respondents and Staff disagree that the DBs of the LRDIMM “selectively allow” there to be data transmission. In doing so, they focus on whether the control of the data transmission in the LRDIMM is “selective” as that term should be understood in the context of the ’185 patent

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and, in particular, what exactly is being selected. (RIB at 15-16, RRB at 5-7, SIB at 138-139 and SRB at 45-47.)

Respondents and Staff contend that during prosecution, independent claim 28 (which would eventually issue as independent claim 1) was amended to add the following underlined language in order to distinguish a reference (Rajan) cited during prosecution: “selectively allow data transmission between the system memory controller and at least one selected memory device of the at least two corresponding memory devices and to selectively isolate at least one other memory device of the at least two corresponding memory devices from the system memory controller....” (RIB at 16, 18 and SIB at 138 (each citing RX-1584C at Q/A 102, 106, 107, 113).) In view of this amendment, Respondents argue that

the accused DBs in the accused products do *not* selectively allow data transmission to one rank and not the other (instead data is transmitted to *all* ranks, and a prior-art chip select signal from the system memory controller to a given rank of memory tells that rank of memory to listen for the incoming data), and the accused DBs do *not* selectively isolate a given rank from the memory controller on the host computer (instead *all* ranks are isolated).

(RIB at 15 (citing RX-1584C at Q/A 81-92, 104-117; *see also* Brogioli, Tr. 468:15-22, 471:1-7, 472:23-473:7, 474:7-20 (admissions by Brogioli that the DBs send data to *all* ranks of memory, not just selected ranks of memory); *id.* at 485:19-486:2 (admission by Brogioli that “there’s no fork in the road” in the accused products); *id.* at 476:23-477:2, 478:17-479:6, 480:21-25, 481:15-20 (admissions by Brogioli that the DBs *always* isolate, they do not selectively isolate)); *see also* RIB at 16 and 18.) In sum, Respondents and Staff take the position that even if the DBs of the LRDIMM utilize directional and timing controls that are selective, the effect of those “selective” actions does not amount to discriminating between memory modules such that some participate in data transmission to the exclusion of others. (RIB at 18 (stating “[A]t most the BCOM signals (with RankID) affect the *timing* of any transmission through the DB, but they do not change the

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fact that the Data Buffer always transmits data to *all* ranks, contrary to the requirement of the claim language that the circuit (alleged to be the DB) must selectively transmit data to one rank and not the other.”.)²⁶

Based on Complainant’s evidence and arguments, it appears that the DBs of the LRDIMM utilize directional (*i.e.*, read/write) and timing controls to determine the *order* in which data is transmitted as opposed to controlling whether only a selected subset of memory devices participate in that communication to the exclusion of other memory devices. In fact, Complainant states as much: “[t]he evidence showed that the DB in DDR4-compliant LRDIMMs facilitates *when data is transmitted during a write or a read operation* based on various latency/delay values and rank-specific timing.” (CIB at 112 (emphasis added) (citing CX-0006C at Q/A 225-27; Subramanian, Tr. at 675:1-685:4; CX-0417 at 00025; CX-0505 at 00016; *see also* CRB at 60 (stating “the only dispute is whether ‘how and when’ the DB allows data transmission satisfies the ‘Selective Allowance’ claim limitation.”).) However, in utilizing those directional and timing controls, the DBs assert control over *all* of memory devices of the LRDIMM. This distinction is critical to determining whether the LRDIMM infringe.

The “selectively allow” feature of independent claim 1 recites that the circuits are configured to perform some selective actions—which Complainant contends covers the directional and timing controls of the LRDIMM’s DBs—that result in the circuits discriminating the “first” memory devices from the “other” memory devices with respect to data transmission.²⁷ On first blush, it could be argued with respect to data transmission that there is no requirement

²⁶ Respondents call the functional discrimination between subsets of memory modules “a telltale ‘fork in the road’ layout.” (RIB at 16.)

²⁷ *See* designation convention adopted *supra* in section VII.C.

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the circuit discriminate between the “first” and “other” memory devices by virtue of the “at least one” language (*i.e.*, allowing data transmission between the memory controller and at least one of the at least two memory devices could include allowing data transmission between *all* memory devices). Such a conclusion, however, is belied by the applicant’s amendments and arguments during prosecution.

As noted above, the applicant amended what would become independent claim 1 as follows during prosecution: “selectively allow data transmission between the system memory controller and at least one selected memory device of the at least two corresponding memory devices and to selectively isolate at least one other memory device of the at least two corresponding memory devices from the system memory controller....” (JX-0008 at 702.) The applicant argued that this amendment distinguished the cited art (Rajan) because

Rajan does not disclose “the plurality of circuits configured to selectively allow data transmission between the system memory controller and at least one selected memory device of the at least two corresponding memory devices and to selectively isolate at least one other memory device of the at least two corresponding memory devices from the system memory controller,” as recited by Claim 28 (emphasis added). *The Office Action at p. 5 states that “the presence of the ‘at least one buffer chip’ isolates the DRAMs from the memory controller because the DRAMs are no longer directly connected to the memory controller.”* However, even if, for the sake of argument, the buffer chips of Rajan are interpreted as isolating the DRAMs from the memory controller, *there is no support for Rajan being interpreted as disclosing a plurality of circuits that selectively allows data transmission between the system memory controller and at least one selected memory device of the at least two corresponding memory devices and that selectively isolates at least one other memory device of the at least two corresponding memory devices from the system memory controller*, as recited by Claim 28. At least on this basis, Applicants submit that Claim 28 is patentable over Rajan.

(JX-0008.00697-698 (emphasis added).) As can be seen, the applicant argued that the distinction with Rajan was not simply related to separating the memory controller and the memory devices by virtue of an intervening component (*i.e.*, a buffer chip). Rather, the applicant

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argued that the claimed subject matter was distinguishable because it involved allowing only a selected subset of the memory devices—to the exclusion of others—from communicating with the memory controller.²⁸ Indeed, Complainant’s expert (Baker) acknowledged that “[t]he big difference, in simple terms, between Rajan and the ’185 [patent] is Rajan is not using the buffers to *select the memory device*.” (Baker, Tr. 1004:17-22 (emphasis added).) Thus, the amendment and accompanying argument made clear that the “selectively allow” and the “selectively isolate” features are related in terms of their ability to choose and treat separately the “first” memory devices from the “other” memory devices with respect to the memory controller. Complainant’s evidence, however, fails to establish that the “selective” actions it cites divorce one subset of memory devices from another; rather the evidence of record shows that the cited actions are directed to selecting the order and direction in which *all* of the memory devices collectively operate. (See RX-1584C at Q/A 81-92, 104-117.)

Thus, the undersigned finds that the LRDIMM does not include this feature of independent claim 1.

iv. “Selective Isolation”

Independent claim 1 further recites that each of the plurality of circuits is configured “to selectively isolate at least one other memory device of the at least two corresponding memory devices from the system memory controller in response to the module control signals.” As discussed at length above, the undersigned has determined that the term “selectively isolate”

²⁸ Complainant argues that this rationale produces “a narrow interpretation [that] improperly excludes embodiments of the ’185 Patent that are expressly disclosed in the specification and expressly permitted by the language of claim 1.” (CRB at 63.) Even assuming *arguendo* that Complainant is correct about the scope of disclosure or what is ostensibly “permitted” by the words used in the claims, such does not address what the claims actually cover in view of the amendments and arguments made by the applicant to distinguish the cited art and secure allowance of the patent. See *Graham*, 383 U.S. at 33 (explaining that “claims that have been narrowed in order to obtain the issuance of a patent by distinguishing the prior art cannot be sustained to cover that which was previously by limitation eliminated from the patent.”).

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should be construed as “selectively electrically separate.” That conclusion derives from both the intrinsic and extrinsic evidence of record. Indeed, even Complainant’s expert (Baker) testified that “isolation always requires electrical separation.” (Baker, Tr. 1015:21-23.)

The parties and Staff set forth generally the same arguments and reasoning with respect to the “selective isolation” as they did regarding the “selective allowance” feature. (CIB at 118-120, CRB at 61-62, RIB at 15-16, RRB at 7-8 and SRB at 45-47.) Accordingly, a similar analysis—and outcome—is warranted. To be clear, the “selective allowance” and “selectively isolate” features are not the same even though both require discriminating between different subsets of memory modules and their relationship with the memory controller. The former requires selectively permitting only a subset of the memory modules to participate in data communications with the memory controller to the exclusion of the other memory modules whereas the latter requires selectively limiting or stopping the electrical relationship (*i.e.*, electrically separating) between a subset of the memory devices and the memory controller while maintaining that electrical relationship for other of the memory controllers.

As with “selective allowance” Complainant’s evidence is again directed to the “rank-specific timing” and how it is used to order the memory modules in electrical relationship to memory controller. (CIB at 118-120.) However, those actions are applied to all of the memory devices, not a selected subset. Indeed, Complainant expressly confirms that in the accused LRDIMM “*the DB electrically separates all the memory devices during the selected access*” by asserting appropriate buffer enable signals which enable the DB’s internal write or read buffers” and that “[w]hen enabled, the write or read buffers *electrically separate all the memory devices* through the use of high impedance.” (*Id.* at 120 (emphasis added).) Thus, by Complainant’s own admission the “selective” operational controls of the LRDIMM that it relies upon to establish infringement apply to all of the

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memory modules and do not selectively differentiate between different subsets thereof such that only certain memory devices are separated from the memory controller and others are not.

Accordingly, the undersigned finds that the LRDIMM does not include this feature of independent claim 1.

2. Dependent Claims 2, 3, 5 and 6

“One who does not infringe an independent claim cannot infringe a claim dependent on (and thus containing all the limitations of) that claim.” *Wahpeton*, 870 F.2d at 1552 n. 9. Given that the undersigned has found that independent claim 1 of the '185 patent is not infringed, dependent claims 2, 3, 7, 8 and 10-12 are also not infringed.

The undersigned notes that Respondents do not appear to dispute that the accused products include the additionally recited features of dependent claims 2, 3, 7, 8 and 10-12 of the '185 patent. (RIB at 18.) Thus, the determination of whether these dependent claims are infringed rises and falls solely with the determination of infringement of independent claim 1.

E. Domestic Industry – Technical Prong

Complainant asserts that its HyperCloud products and HybriDIMM products practice claims 1-3, 7, 8 and 10-12 of the '185 patent. (CIB at 130-132 and CRB at 66.) Among other things, Complainant acknowledges that “the HybriDIMM Products include a LRDIMM portion that functions exactly like a DDR4-compliant LRDIMM such as the Accused LRDIMM Products” and that “[t]here is no dispute among the parties that this is (*sic.*) case, namely that the LRDIMM block of the HybriDIMM Products is substantially similar to the Accused LRDIMM Products with respect to the claims at issue.” (CIB at 131-132.)

Respondents do not dispute (or even address) whether Complainant's HyperCloud products practice claims 1-3, 7, 8 and 10-12 of the '185 patent. (RIB at 18 and RRB at 11.) Respondents

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disagree, however, that Complainant's HybriDIMM products practice the asserted claims. (RIB at 18 and RRB at 11.) Consistent with Complainant's contention (discussed above), Respondents assert that the accused LRDIMM products and Complainant's HybriDIMM operate in the same manner. (RIB at 18.) According to Respondents, therefore, Complainant's "HybriDIMM do not practice the asserted claims for the same reasons that SK hynix's [LRDIMM] products do not" infringe. (*Id.* (citing RX-1584C at Q/A 178-80).)

Staff takes the position Complainant's HyperCloud products practice claims 1-3, 7, 8 and 10-12 of the '185 patent in view of the testimony of Complainant's expert and the lack of contradictory evidence and/or testimony from Respondents. (SIB at 142-144 and SRB at 47-48.) Staff agrees, however, with Respondents that Complainant's HybriDIMM products do not practice the asserted claims. (SIB at 145-146 and SRB at 47-48.)

In view of the uncontested evidence of record from Complainant's expert, (CX-0004C at Q/A 806-902), the undersigned finds that Complainant's HyperCloud products practice claims 1-3, 7, 8 and 10-12 of the '185 patent.

With respect to the Complainant's HybriDIMM, the parties and Staff agree that there is no difference between the accused products and Complainant's HybriDIMM with respect to whether they practice the asserted claims of the '185 patent. (CIB at 131-132, RIB at 18; SIB at 145-146.) Therefore, the parties and Staff essentially agree that the determination as to whether Complainant's HybriDIMM products establish the technical prong of the domestic industry requirement turns on the same analysis set forth above regarding whether the accused LRDIMM products infringe claims 1-3, 7, 8 and 10-12 of the '185 patent. Given that the undersigned has determined that the accused LRDIMM products do not infringe claims 1-3, 7, 8 and 10-12 of the '185 patent, the undersigned finds that Complainant's HybriDIMM products do not practice

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those claims for at least the same reasons for which the accused products do not infringe claim 1-3, 7, 8 and 10-12 of the '185 patent.

Based on the foregoing reasoning, the undersigned finds that Complainant has satisfied the technical prong of the domestic industry requirement for the '185 patent based on its HyperCloud products:

F. Validity

1. Anticipation

a. U.S. Patent No. 7,024,518 to Halbert *et al.* ("Halbert")

Respondents contend that Halbert teaches all of the features of claims 1-3, 7, 8 and 10-12 of the '185 patent. (RIB at 19-28 and RRB at 11-17.) Complainant and Staff disagree, and posit that Halbert does not anticipate for the same reasons that Complainant's HybriDIMM products and Respondents' LRDIMM products do not practice the asserted claims of the '185 patent. That is, Complainant and Staff assert that Halbert does not teach circuits including the "selectively allow" or "selective isolation" features because the operations of Halbert are applied to all of the memory devices, not a selected subset. (CIB at 134-136, CRB at 67, SIB at 147 and SRB at 48-49.)

Respondents dispute this conclusion because Halbert discloses that "[g]enerally, multiple ranks will receive the same address and commands, and will perform memory operations with the interface circuit concurrently." (RIB at 23 (citing RX-1429 at ¶ [0030] which corresponds to Halbert at 4:57-59²⁹)). According to Respondents, the fact that concurrent operations are described as occurring on the memory devices "generally" means that there must be occurrences where they occur "non-concurrently" which Respondents then equate with "selective allowance"

²⁹ RX-1429 is the U.S. Patent Application Publication of the application that matured into U.S. Patent No. 7,024,518 (*i.e.*, Halbert).

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of data transmission to a selected subset of memory modules as required by independent claim 1. (*Id.* at 25 and RRB at 15 (each citing Baker, Tr. at 1008:22-1009:4; *see also* RX-0006C at Q/A 595 (explaining that “generally” does not mean “always.”).) With respect to the “selective isolation” feature, Respondents point out that Halbert discloses an embodiment in which the “configuration can also allow the memory devices to operate at voltage levels independent of the voltage levels of the memory system that the module is attached to. The exemplary embodiments also allow the memory devices to be isolated from the full capacitive loading effects of the system memory data bus.” (*Id.* at 26 (citing RX-1429 at ¶ [0024] which corresponds to Halbert at 3:64-4:2.)

Based on the above, Respondents appear to be arguing that Halbert *suggests* non-concurrent memory module data transmission by virtue of the use of the word “generally” in the cited disclosure. Conspicuously, Respondents do not appear to cite to any other portion of Halbert explaining or providing an example of non-concurrent memory module operations. On this basis alone, therefore, Halbert cannot anticipate, much less do so by clear and convincing evidence, given that in order for a reference to anticipate it must teach each and every feature of the claimed subject matter. *See Verdegaal Bros. v. Union Oil Co. of California*, 814 F.2d 628, 631 (Fed. Cir. 1987) (“A claim is anticipated only if each and every element as set forth in the claim is found, either expressly or inherently described, in a single prior art reference.”).

Moreover, in order for Halbert “[t]o serve as an anticipating reference, [Halbert] must enable that which it is asserted to anticipate.” *Elan Pharm., Inc. v. Mayo Found. For Med. Educ. & Research*, 346 F.3d 1051, 1054 (Fed. Cir. 2003). For example, even assuming for the sake of argument that Halbert discloses non-concurrent memory module operations, Respondents do not adequately explain how the circuits make a selection between subsets of those memory devices

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to the exclusion of others as opposed to merely establishing a read/write order among all of the memory devices. On this point it is worth noting that Respondents' citation to the testimony of Complainant's expert (Baker) is incomplete. (RRB at 15.) Although Complainant's expert agreed that "[g]enerally does not mean always" he immediately thereafter explained that "the invention in Halbert doesn't work if you don't select the multiple ranks at the same time. You do that so you can transmit the information at a higher speed on the bus." (Baker, Tr. at 1009:3-7.) Thus, the evidence of record indicates that Halbert does not enable non-concurrent memory module data transmission, and therefore cannot anticipate it.

With respect to the "selective isolation," Halbert discloses that the "memory devices" can (i) "operate at voltage levels independent of the voltage levels of the memory system" and (ii) "be isolated from the full capacitive loading effects of the system memory data bus." (Halbert at 3:64-4:2.) Therefore, this portion of Halbert discusses the memory devices collectively and their collective electrical relationship with the memory controller. Even if suggestive to one of ordinary skill in the art, that disclosure is not the same as the requirement of independent claim 1 that the circuits be configured to selectively electrically separate a subset of the memory devices and the memory controller while maintaining that electrical relationship for other of the memory devices. As such Halbert's disclosure cannot anticipate the "selective isolation" feature of independent claim 1.

In view of the forgoing, the undersigned finds that Respondents have failed to prove by clear and convincing evidence that Halbert anticipates independent claim 1 or the claims depending therefrom, including instantly asserted dependent claims 2, 3, 7, 8 and 10-12, of the '185 patent under 35 U.S.C. §102.

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2. Obviousness

a. Halbert

Respondents contend that claims 1-3, 7, 8 and 10-12 of the '185 patent are obvious under 35 U.S.C. § 103 based upon Halbert. (RIB at 28 and RRB at 17.) Respondents make this argument in the alternative to their contention that Halbert anticipates claims 1-3, 7, 8 and 10-12 under 35 U.S.C. § 102.

As discussed above, Respondents argue that Halbert suggests the “selective allowance” feature because it purportedly describes non-concurrent memory module data transmission based upon the use of the word “generally” in the disclosure that “[g]enerally, multiple ranks will receive the same address and commands, and will perform memory operations with the interface circuit concurrently.” (RIB at 23 (citing RX-1429 at ¶ [0030] which corresponds to Halbert at 4:57-59).) With respect to the “selective isolation” feature, Respondents rely on the same disclosures from Halbert discussed above in conjunction with 35 U.S.C. §102. In short, therefore, the question is whether this evidence from Halbert sufficiently suggests the “selective allowance” and “selective isolation” features of independent claim 1. Based upon the evidence of record, the undersigned finds that it does not.

In *KSR*, 550 U.S. at 418-19, the Supreme Court shifted the obviousness analysis from a more objective test (*i.e.*, the Teaching, Suggestion Motivation Test; “TSM”) to a more subjective analysis that is required to include some “articulated reasoning” that amounts to more than mere conclusions. In this regard, an obviousness “analysis need not seek out precise teachings directed to the specific subject matter of the challenged claim, for a court can take account of the inferences and creative steps that a [POSITA] would employ” but rather adopts a flexible analysis reflecting, among other things, that “[t]he combination of familiar elements according to

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known methods is likely to be obvious when it does no more than yield predictable results.” *Id.* at 416-18. Even within the flexible framework mandated by *KSR*, however, Respondents contentions are insufficient.

With respect to the “selective allowance” feature, the semantics of the word “generally” do not, standing alone, suffice as an “articulated reasoning.” To be sure, there is no disagreement amongst the experts that the term “generally” does not mean “always.” (RX-0006C at Q/A 595 and Baker, Tr. at 1009:3-4.) Nevertheless, that alone hardly leads to the conclusion that the circuits of the Halbert device are configured to selectively allow data transmission to a selected subset of memory modules to the exclusion of others in response to signals from the memory controller rather than, for example, sending a signal to all of the memory modules that sets an order for the read/write operations.

The undersigned acknowledges that the Halbert disclosure cited by Respondents uses very broad terminology, and as such could arguably be read such that the “selective allowance” feature falls within that language. However, merely because a claim feature can fall under the umbrella of the language used in a particular disclosure does not mean the disclosure renders obvious the claim feature. Given the nuanced nature of the “selective allowance” feature, the undersigned finds that to divine it from the use of the word “generally” in the cited portion of Halbert, coupled with the lack of evidence in the record as to why one of ordinary skill in the art would come to that particular conclusion from that disclosure, is not possible without the benefit of utilizing improper hindsight analysis. *See Insite Vision Inc. v. Sandoz, Inc.*, 783 F.3d 853, 859 (Fed. Cir. 2015). As such, the undersigned finds that Halbert’s disclosure does not render obvious the “selective allowance” feature of independent claim 1.

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With respect to the “selective isolation,” Halbert discloses that in at least one configuration “the memory devices to operate at voltage levels independent of the voltage levels of the memory system that the module is attached to” and that “the memory devices to be isolated from the full capacitive loading effects of the system memory data bus.” (Halbert at 3:64-4:2.) While this disclosure certainly seems to suggest that the memory controller and the memory devices as a group can operate at different voltage levels or perhaps that different voltages can be selected for the memory controller and memory devices, respectively, it does not indicate one way or the other that the circuits are configured to selectively electrically separate a subset of the memory devices and the memory controller while maintaining that electrical relationship for other of the memory devices. Therefore, the undersigned finds that Halbert’s disclosure does not make obvious the “selective isolation” feature of independent claim 1.

Given that Halbert fails to suggest at least the above two discussed features of independent claim 1, the undersigned finds that Respondents have failed to prove by clear and convincing evidence that Halbert establishes a *prima facie* case of obviousness as to independent claim 1 or the claims depending therefrom, including dependent claims 2, 3, 7, 8 and 10-12 under 35 U.S.C. §103.

b. Halbert in view of U.S. Patent No. 8,250,295 to Amidi *et al.* (“Amidi”), U.S. Patent Application Publication No. 2009/0103387 to Shau (“Shau”) or U.S. Patent Application Publication No. 2006/0262586 to Solomon *et al.* (“Solomon”)

Respondents alternatively contend that claims 1-3, 7, 8 and 10-12 of the ’185 patent are obvious under 35 U.S.C. §103 based upon the combined teachings of Halbert in view of Amidi, Shau or Solomon. (RIB at 20, 25-26, RRB at 15-16.)

Although Respondents maintain that Halbert teaches or suggests all of the features of independent claim 1, they rely on Amidi as disclosing “where chip select signals are used so that not all ranks are accessed concurrently.” (RIB at 25 (citing RX-0006C at Q/A 554).) Respondents

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then contend such a combination has been endorsed by the PTAB. (RIB at 25-26.) Respondents also urge that Shau discloses adding ranks to Halbert. (*Id.* at 25.) Respondents assert, with respect to dependent claim 10, that Solomon “discloses snooping the CAS latency parameter setting command of JESD79, and controlling the interface circuit accordingly.” (*Id.* at 27 (emphasis in original).) These contentions, however, amount to nothing more than an assertion that various claim features are generally known in the art. Respondents’ briefing fails to set forth any basis why one of ordinary skill in the art would select those particular teachings from Amidi, Shau and Solomon in the first place, much less establish by clear and convincing evidence why and how one of ordinary skill in the art would combine those teachings with Halbert with an expectation to arrive at the claimed subject matter. Thus, even if Respondents have shown that all of the features of the claims were known in the art it does not alone establish obviousness. *KSR*, 550 U.S. at 418 (“[A] patent composed of several elements is not proved obvious merely by demonstrating that each of its elements was, independently, known in the prior art.”).

Even assuming *arguendo* that Amidi, Shau and Solomon supply the deficiencies for which they are relied upon, they nevertheless fails to supply the deficiencies of Halbert discussed above. Among other things, Amidi, Shau and Solomon are not relied upon as teaching or suggesting the “selective allowance” and “selective isolation” features of independent claim 1. For example, Respondents contend that Amidi discloses “where chip select signals are used so that not all ranks are accessed concurrently.” (RIB at 25.) Such a teaching, however, does not suggest a memory circuit device configured to selectively allow data transmission to a selected subset of memory modules to the exclusion of others in response to signals from the memory controller.” Moreover, none of Amidi, Shau and Solomon is asserted as teaching or suggesting the “selective isolation” feature.

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In view of the forgoing, therefore, the undersigned finds that Respondents have failed to prove by clear and convincing evidence that the combined teachings of Halbert, Amidi, Shau or Solomon establish a *prima facie* case of obviousness as to independent claim 1 or the claims depending therefrom, including dependent claims 2, 3, 7, 8 and 10-12, under 35 U.S.C. §103.

c. SK Hynix DDR2 RDIMM

Respondents contend that claims 1-3, 7, 8 and 10-12 of the '185 patent are obvious under 35 U.S.C. §103 based upon the SK Hynix DDR2 RDIMM ("DDR2").³⁰ (RIB at 28-34 and RRB at 17-19.) Complainant and Staff disagree, and in particular dispute whether the DDR2 teaches or suggests "a plurality of memory devices" and/or "a plurality of circuits" as recited in independent claim 1. (CIB at 141-144, CRB at 70, SIB at 151 and SRB at 49.)

i. "Plurality of Memory Devices"

With respect to the "plurality of memory devices" feature of independent claim 1, Respondents contend that the individual "banks" within each DRAM constitutes a "memory device" and that multiple of the banks constitute a "plurality of memory devices." (RIB at 29-30 and RRB at 17-18.) Respondents cite two equally unavailing grounds in support of this contention.

First, Respondents allege the '185 patent specification supports their position because it "does not limit '*memory device*' in any specific way. JX-0002 at 9:8-20 ('Memory devices . . . compatible with embodiments described herein include, but are not limited to, . . . have packaging which include, but *are not limited to*, . . .')." (RRB at 17-18 (emphasis in original).) Respondents contend that interpreting the '185 patent any other way would improperly limit the

³⁰ Respondents also casually assert that other references can be combined with the DDR2 to render obvious dependent claims 2, 3, 7, 8 and 10-12. (RIB at 33.) Respondents, however, fail to adequately explain how or why these additional references would be combined with the DDR2. (RIB at 33.) As such, the undersigned finds that Respondents have failed to prove by clear and convincing evidence that the proposed combinations of DDR2 with the additionally cited references establishes a *prima facie* case of obvious as to the asserted claims.

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claims to preferred embodiments. (RRB at 18.) However, in making this argument, Respondents fail to fully cite the '185 patent which provides, in relevant part, that:

Memory devices 412, 412' compatible with embodiments described herein include, but are not limited to, random-access memory (RAM), dynamic random-access memory (DRAM), synchronous DRAM (SDRAM), and double-data-rate DRAM (e.g., DDR, DDR2, DDR3, etc.). In addition, memory devices 412, 412' having bit widths of 4, 8, 16, 32, as well as other bit widths, are compatible with embodiments described herein. Memory devices 412, 412' compatible with embodiments described herein have packaging which include, but are not limited to, thin small-outline package (TSOP), ball-grid-array (BGA), fine-pitch BGA (FBGA), micro-BGA (μ BGA), mini-BGA (mBGA), and chip-scale packaging (CSP).

(JX-0002 at 9:8-20.) As can be clearly seen, the '185 patent exemplifies the types of components that could be considered "memory devices." Even though the '185 patent expressly sets forth that the listed specific embodiments are non-limiting examples, Respondents are incorrect to disregard the framework the list of examples provides for identifying what constitutes a "memory device." Conspicuously, Respondents do not argue that the components they rely on from the DDR2 fall within that framework or are otherwise considered to be art-equivalent to the exemplary "memory devices" given that the components Respondents rely on are merely subcomponents of the exemplified "memory devices" (e.g., are subcomponents of the listed DDR2).

Instead, Respondents essentially advocate disregarding the express examples of "memory devices" provided by the '185 patent and turn to their expert to assert that a "memory device" should be considered to be any device "to perform memory functions" or "that performs memory functions." (RRB at 32 and RIB at 18.) This definition is overly broad and untethered to the '185 patent disclosure discussed above. Indeed, utilizing that definition would lead to the absurd conclusion, for example, that a computer keyboard qualifies as a "memory device" since it is used to perform memory functions (e.g., enabling users to input data for storage).

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While not necessarily agreeing with Complainant's arguments regarding the meaning of the term "memory device," and in view of the above, the undersigned finds that Respondents are incorrect in contending that a bank inside a DRAM die of the DDR2 is a separate and independent "memory device" or that multiple of such banks constitutes a "plurality of memory devices." (CIB at 143-144 and CRB at 70.)³¹ Based on the arguments presented, the undersigned finds that Respondents have not established by clear and convincing evidence that the DDR2 includes a "plurality of memory devices" as recited in independent claim 1.

ii. "Plurality of Circuits"

Respondents also argue that combined circuitry components from two different dies (*i.e.*, chips) of the DDR2 constitute the "plurality of circuits" of independent claim 1. (RIB at 30-33 and RRB at 18-19.) Complainant asserts that Respondents' approach is "arbitrary" and inappropriate because "two dies within the same DRAM package stack on top of each other, reside on two different ranks, and operate independently" and therefore Respondents' contention incorrectly relies on combining "independent internal circuitries residing in independently compartmentalized DRAM dies." (CIB at 144 and CRB at 70.) Respondents counter that Complainant is relying on a claim construction for the term "circuit" that Complainant was obligated, but failed, to construe and that the '185 patent specification supports its position. (RRB at 17-19.) Respondents are incorrect on both of these points.

First, Respondents misapprehend that Complainant was obligated to offer a claim construction on an issue related to invalidity where *Respondents* carry the burden of proof. (RRB at 17-19.) If Respondents' invalidity positions are premised on specific claim constructions—such as

³¹ Staff agrees with Complainant that Respondents' arguments regarding the DDR2 and "memory modules" is incorrect, but does not expressly set forth its basis for arriving at the conclusion. (SIB at 151.)

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the purportedly plain and ordinary meaning of the term “memory device” (*see* RRB at 18)—then it was Respondents’ obligation to offer and establish that claim construction as part of establishing that the cited art clearly and convincingly invalidates the asserted claims of the ’185 patent.

Second, Respondents’ arguments are largely based on how the ’185 patent specification purportedly limits the meaning of certain claim terms. (RIB at 32 and RRB at 17-18.) As noted above, for example, Respondents assert that the ’185 patent does not limit the meaning of the term “memory device” and thus its plain and ordinary meaning should be utilized in assessing whether the DDR2 renders obvious the asserted claims. (RRB at 32 and RIB at 17-18.)

With respect to the term “circuit,” Respondents rely on a selective invocation of the ’185 patent specification. In particular, in support of their position that components of the circuitry of different dies constitute a single circuit, Respondents argue that the ’185 patent “does not limit the claimed ‘*circuit*’ to a single die and expressly discloses that a ‘*circuit*’ can include ‘one or more functional devices’ and ‘may comprise one or more integrated circuits.’” (RRB at 18 (citing JX-0002 at 9:65-10:9) (emphasis in original).) However, that is not all the ’185 patent provides:

In certain embodiments, the control circuit 430, 430’ may include one or more functional devices, such as a programmable-logic device (PLD), an application-specific integrated circuit (ASIC), a field-programmable gate array (FPGA), a custom-designed semiconductor device, or a complex programmable-logic device (CPLD). In certain embodiments, the control circuit 430, 430’ may comprise one or more custom devices. In certain embodiments, the control circuit 430, 430’ may comprise various discrete electrical elements; while in other embodiments, the control circuit 430, 430’ may comprise one or more integrated circuits.

(JX-0002 at 9:65-10:9.) As can be seen, the ’185 patent describes a number of different embodiments for the control circuit. Thus, the question is twofold: (i) does independent claim 1 cover all of those embodiments—including the subset selectively cited by Respondents—and (ii) if not, which embodiments are covered. By citing only those embodiments convenient to their argument, Respondents fail to address or establish what is actually covered by the claim.

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Even assuming *arguendo* that all of the embodiments fall within the scope of independent claim 1, and in particular the embodiments selected by Respondents, there is no indication that the cited portions of the '185 patent embrace the concept of combining circuitry parts that are independent from one another by virtue of residing and operating in compartmentalized dies. Regardless of whether the '185 patent describes that the control circuit can comprise one or more integrated circuits, Respondents have not carried their burden of showing by clear and convincing evidence that such disclosure refers to anything other than multiple circuits within the same die. Simply asserting that the '185 patent is not expressly limited in that manner does not carry that burden.

Given the arguments and deficiencies discussed above, the undersigned finds that Respondents have not established by clear and convincing evidence that the DDR2 includes a "plurality of circuits" as recited in independent claim 1.

In view of the above, the undersigned finds that Respondents have failed to prove by clear and convincing evidence that the DDR2 renders obvious independent claim 1 or the claims depending therefrom, including instantly asserted dependent claims 2, 3, 7, 8 and 10-12, of the '185 patent under 35 U.S.C. §103.

d. U.S. Patent No. 8,130,560 to Rajan *et al.* ("Rajan")

Respondents contend that Rajan alone or in combination with a number of different references (*i.e.*, Halbert, Shau, Stone and T174LS245) render obvious claims 1-3, 7, 8 and 10-12 of the '185 patent under 35 U.S.C. §103. (RIB at 34-38 (citing RX-0006C at Q/A 658-692) and RRB at 19-21.) The parties dispute whether Rajan alone or in combination suggest (i) a "controller" configured to "produce module control signals," (ii) "a plurality of circuits"

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configured to “receive the module control signals” and (iii) “a first bit width” and “a second bit width smaller than the first bit width.” (CIB at 139-141 and RRB 20-21.)³²

i. “Controller”

With respect to the “controller,” Respondents rely on their expert’s witness statement which cites to the registers of Rajan as corresponding to the claimed controller because “skilled artisans understood at the time that these buffer chips need to be controlled by the register circuit to perform functions, such as emulating a higher capacity virtual DRAM....” (RIB at 35 (citing RX-0006C at Q/A 663).) Alternatively, Respondents state that this feature is taught by Halbert. (*Id.* at 36.) Citing the witness statement of its own expert, Complainant disagrees and contends, on the one hand, that Rajan does not teach this feature because the buffer chips do not necessarily need to be controller by the register circuit and, on the other hand, that there is no basis set forth by Respondents to combine Rajan and Halbert and such a combination is impermissible because it changes the principle of operation of Rajan. (CIB at 140-141 (citing CX-0930C at Q/A at 699-701 and 751-752).)

ii. “Plurality of Circuits”

Regarding the “plurality of circuits” configured to “receive the module control signals,” Respondents cite to the buffer circuits 612 of Rajan and contend that those of ordinary skill in the art could “implement” Rajan’s register “to produce module control signals” and also “have its buffer circuits ‘configured to receive the module control signals.’” (RIB at 35-36.) Complainant’s respond that Rajan’s buffer circuits do not “receive any control signal at all from the registers.”

³² Staff states only that “the evidence does not show that a person of ordinary skill in the art would be motivated to combine Rajan, which uses simple buffers for selecting among multiple ranks of memory devices, and Halbert, which makes concurrent access to all memory devices.” (SIB at 150.)

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(CIB at 141.) As such, according to Complainant, the Rajan buffer circuits also cannot meet the “selective allowance” and “selective isolation” features of independent claim 1. (*Id.* at 141.)

iii. “First Bit Width” and “Second Bit Width”

As to the “first bit width” and “second bit width smaller than the first bit width” features of independent claim 1, Respondents simply state that Rajan teaches these features and refer to their expert’s witness statement. (RIB at 35 (citing RX-0006C at Q/A 664-665³³)) and RRB at 20. Respondents’ argument appears to be that if the embodiment shown in Figure 2 of Rajan is modified to include buffers, then it will have the claimed bit width relationship. (RRB at 20.) Complainant counters that the witness statement of Respondents’ expert acknowledges that Rajan does not disclose this feature and in fact that “Rajan teaches the opposite—the memory devices have a larger bit width than the buffer chip” and as such, the proposed modification of Rajan in view of Halbert would be require improperly modifying Rajan manner opposite to its disclosed configuration. (CIB at 141 and CX-0930C at Q/A 751-752.)

iv. Analysis

The undersigned finds it has not been shown by clear and convincing evidence that Rajan either alone or in combination renders obvious claims 1-3, 7, 8 and 10-12 of the ’185 patent under 35 U.S.C. §103.

As discussed above, a patent claim is not rendered obvious merely by showing that the claimed elements are known. *KSR*, 550 U.S. at 418. Rather, there must be some basis established (*e.g.*, motivation) for modifying and/or combining the art. (*Id.* at 416-418.) The Federal Circuit has explained that (i) “[i]n considering motivation in the obviousness analysis,

³³ Respondents’ Brief cites to RX-0006C at Q/A 676-677, however, these questions and answers do not address this feature. It appears Respondents intended to cite RX-0006C at Q/A 664-665.

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the problem examined is not the specific problem solved by the invention” and (ii) that “[d]efining the problem in terms of its solution reveals improper hindsight in the selection of the prior art relevant to obviousness.” *Insite Vision*, 783 F.3d at 859 (citing *In re Kahn*, 441 F.3d 977, 988 (Fed.Cir. 2006) and *Monarch Knitting Mach. Corp. v. Sulzer Morat GmbH*, 139 F.3d 877, 881 (Fed.Cir. 1998)). Here, Respondents fail to articulate any basis for modifying the embodiments Rajan alone³⁴ or in combination with other references other than using the claimed subject matter to guide the proposed modifications.

As to whether Rajan can stand alone, Respondents make far too many assumptions with respect to modifications that *could* be made to Rajan to arrive at the subject matter of independent claim 1 without sufficiently explaining the basis for why one of ordinary skill in the art would make those modifications. For example, in making their argument that Rajan suggests the “first bit width” and “second bit width smaller than the first bit width” features, Respondents pile proposed modification upon proposed modification. The witness statement of Respondents’ expert argues that Figures 4 and 6 of Rajan each teach embodiments that include buffers, and that Rajan further suggests that those embodiments “may be implemented in the context of the details” of other embodiments, including the embodiment of Figure 2 which does not include buffers. (See RX-0006C at Q/A 659 (citing Rajan at 5:39-41 and 6:27-29).) Respondents also point to Rajan’s disclosure that “as an option, the system 170 may include at least one buffer chip (not shown) that is in communication with the memory circuits 178 and the memory bus 174” as suggesting to

³⁴ Rajan was cited during prosecution of the ’185 patent. (See JX-0002 at 2.) As such, Respondents have an elevated burden for establishing that Rajan invalidates the ’185 patent. See *In the Matter of Certain Electronic Devices, Including Mobile Phones and Tablet Computers, and Components Thereof*, Inv. No. 337-TA-847, Initial Determination, at 15 (Sept. 23, 2013) (explaining that “When no prior art other than that which was considered by the PTO examiner is relied on by the attacker, he has the added burden of overcoming the deference that is due to a qualified government agency presumed to have properly done its job[.]” and “Therefore, the challenger’s ‘burden is especially difficult when the prior art was before the PTO examiner during prosecution of the application.’”) (internal citations omitted).

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include a buffer in the embodiment of Figure 2. (*See* RX-0006C at Q/A 659 (citing Rajan at 3:10-14) and 664-665.) On that basis, Respondents' expert concludes that such a modification would result in teaching the claimed first and second bit widths.

Although Rajan discloses that Figures 4 and 6 "may be implemented in the context of the details" of other embodiments, such as that shown in Figure 2, that statement is at best ambiguous with respect to what modifications could or should be made. As much as Respondents contend it "suggests" adding buffers to the embodiment of Figure 2 it could, for example, mean removing the buffers from the embodiments in Figures 4 and 6 or utilizing a mixture of component configurations. The same is true for the various combinations of bit widths and the relationships thereof that can be derived from the figures. In this regard, Rajan does not simply suggest implementing the embodiments of Figures 4 and 5 only with that of Figure 2, but rather in all of the preceding embodiments (including implementing the embodiment of Figure 6 "in the context" of Figure 4). In view of the different potential design options and in the absence of any clear indication to make the above-proposed modifications, Respondents appear to be improperly relying the '185 patent claims to guide the proposed modifications of Rajan. This point is especially true, where, as here, Rajan was considered during prosecution of the '185 patent. (*See supra* at note 34.)

Respondent's further contention regarding Rajan's disclosure that "as an option, the system 170 may include at least one buffer chip (not shown) that is in communication with the memory circuits 178 and the memory bus 174" is similarly unavailing since it relates to a discussion of Figure 1A, and there is no indication that it in any way is suggestion about a modification to the embodiment of Figure 2. While the undersigned understands that the various embodiments illustrated in the figures should not necessarily be considered in isolation, there is a conspicuous

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lack of discussion in Rajan of a buffer in conjunction with the embodiment of Figure 2 compared to the discussions of using buffers in the embodiments of Figures 1A, 4 and 6 cited by Respondents.

Given the multitude of design choices and configurations possible potentially suggested in Rajan, the undersigned finds that Respondents have failed to clearly and convincingly establish a basis for one of ordinary skill in the art to modify Rajan in the particular manner necessary to render obvious the above-discussed features of independent claim 1 other than through the use of impermissible hindsight analysis.³⁵

Respondents also intermittently cite to a number of different additional references in their Brief and/or their expert's witness statement, including Halbert, Shau, Stone and T174LS245, that they propose can be combined with Rajan. Respondents fail, however, to explain why those of ordinary skill in the art would combine the teachings of Rajan with the other cited references. Indeed, Respondents only generally assert that certain deficiencies of Rajan are disclosed in these other references without actually detailing which specific features from those other references they are specifically relying on. Merely stating that other references supply the deficiencies of the primary reference does not suffice as establishing by clear and convincing evidence that the proposed combination renders the claimed subject obvious.

As discussed above, *KSR* requires that there be some "articulated reasoning" for combining the cited art. *KSR*, 550 U.S. at 416-18. Here, Respondents' Brief includes only a single sentence addressing why those of ordinary skill in the art would understand that the buffer chips of Rajan would be controlled by the register circuits *of Rajan* which is not the same as clearly

³⁵ Tellingly, a review of RX-0006C at Q/A 664-665 reveals that Respondents' expert primarily relies on Halbert to modify Rajan with respect to this feature further calling into question the basis for modifying Rajan on its own.

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and convincingly establishing the basis for why one of ordinary skill in the art would combine Rajan with the variously cited other features from the *other references*. (RIB at 35.)

Highlighting this critical deficiency is Respondents' citation to approximately thirty (30) pages from their expert's (Subramanian) witness statement purporting to show that Rajan renders obvious independent claim 1 (along with ten (10) additional pages addressing dependent claims 2, 3, 7, 8 and 10-12). (RIB at 35-38.) It is not the obligation of the undersigned to sift through the witness statement of Respondents' expert in order to discern whether sufficient evidence exists establishing a *prima facie* case of obviousness. Rather, that job rests exclusively with Respondents. *See PharmaStem Therapeutics, Inc. v. ViaCell, Inc.*, 491 F.3d 1342, 1360 (Fed. Cir. 2007). Nevertheless, the undersigned's review of the expert's witness statement reveals it to include little, if anything, explaining why those of ordinary skill in the art would combine the cited references with Rajan in order to arrive at the claimed subject matter. As discussed at length above, that approach to establishing obviousness is improper.

For the forgoing reasons, the undersigned finds that Respondents have failed to prove by clear and convincing evidence that Rajan alone or in combination with the other cited references render obvious independent claim 1 or the claims depending therefrom, including instantly asserted dependent claims 2, 3, 7, 8 and 10-12, of the '185 patent under 35 U.S.C. §103.

e. Secondary Considerations

Given that the undersigned finds that claims 1-3, 7, 8 and 10-12 of the '185 patent are not invalid as obvious, it is unnecessary to address the sufficiency of Complainant's evidence of secondary considerations of non-obviousness. (CIB at 147-149.)

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3. Written Description and Enablement

a. “Chip-Select Signals”

Respondents contend that Complainant’s infringement theory relies on the use of “chip-select signals” to establish that the accused products infringe, but that the ’185 patent fails to disclose using “‘chip-select signals’ to practice the claimed invention....” (RIB at 41-42 and RRB at 23.) Respondents make this argument despite acknowledging that the ’185 patent discloses “chip-select signals” and that such were known prior art. (RIB at 41-42 and RRB at 23.) Respondents take the position that “chip-select signals” are discussed only in the context of “prior art” and not with respect to practicing the claimed invention. (RIB at 41-42 and RRB at 23.)

Complainant counters that not only do Respondents concede that the “chip-select signals” are disclosed in the ’185 patent, but that the ’185 patent does in fact disclose the “chip-select signals” are disclosed in the context of the claimed subject matter. (CIB at 132-133(citing RX-0006C at Q/A 218; JX-0002 at 1:47-54, 10:10-30 and 16:46-49).)

Staff does not address this particular invalidity argument.

The written description requirement does not mandate that a feature or component of an invention that is already within the knowledge of a person of ordinary skill in the art be described in detail. Rather, a sufficient description exists where a patent specification “reasonably conveys to those skilled in the art that the inventor had possession of the claimed subject matter as of the filing date.” *Ariad Pharm., Inc. v. Eli Lilly & Co.*, 598 F.3d 1336, 1351 (Fed. Cir. 2010). For example, there is no “word for word” requirement, *see, e.g., Eiselstein v. Frank*, 52 F.3d 1035, 1038 (Fed. Cir. 1995) and *Martin v. Johnson*, 454 F.2d 746, 751, 172 USPQ 391, 395 (CCPA 1972) (stating “the description need not be in *ipsis verbis* [i.e., “in the same words”] to be

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sufficient”),” and the requirement can be satisfied by “words, structures, figures, diagrams, formulas, etc.,” *Lockwood v. Am. Airlines, Inc.*, 107 F.3d 1565, 1572 (Fed. Cir. 1997).

Here, Respondents acknowledge that the “chip-select signals” were known in the art and, within that context, Respondents fails to explain what additional detail would have been required for compliance with the written description requirement.

Moreover, Respondents’ repeated contention that the “chip-select signals” were not described in the context of the claimed subject matter does not appear to be correct. At a minimum, the ’185 patent states—outside of merely describing the prior or known art—that “[t]he control circuit 430, 430’ of certain embodiments is configurable to be operatively coupled to control lines 440, 440’ to receive control signals (e.g., bank address signals, row address signals, column address signals, address strobe signals, and rank-address or chip-select signals) from the system memory controller 420, 420” and that “[t]he control circuit 430, 430’ may produce additional chip-select signals or output enable signals based on address decoding.” (JX-0002 at 10:10-14 and 24-26.)

Despite the above and other portions of the ’185 patent being identified to Respondents by Complainant, Respondents did not explain how the above disclosures fail to apprise one of ordinary skill in the art that “chip-select signals” are not disclosed in the context of the claimed subject matter or, for that matter, that those disclosures fail to adequately convey “to those skilled in the art that the inventor had possession of the claimed subject matter as of the filing date” as is required. This deficiency is fatal to Respondents’ contention that the ’185 patent lacks written description for the “chip-select signals.”

b. “Exactly Two Memory Devices”

Respondents further contend that the ’185 patent lacks written description and does not enable that “*each circuit of the plurality of circuits having a first bit width and operatively coupled*

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to *at least two* corresponding memory devices ... each having a second bit width smaller than the first bit width' in the case where there are *exactly* two corresponding memory devices operatively coupled to each circuit.” (RIB at 42 (citing RX-0006C at Q/A 223-234) (emphasis in original).) Respondents argue that while the '185 patent and figures may disclose and support certain embodiments, they do not support a configuration having exactly two memory devices. (*Id.* at 42-43.) Respondents then argue, therefore, that the addition of the above claim language during prosecution must have come about due to “some careless amendments to the claims.” (*Id.* at 43.)

Complainant contends that such a configuration was not disclaimed and those of ordinary skill in the art reading the '185 patent and reviewing the figures (especially Figures 4A and 4B) “would know that it disclosed a configuration using exactly two memory devices.” (CIB at 133 (citing CX-0930C at Q/A 976-80).)

Staff agrees that the evidence of record establishes that “a person of ordinary skill in the art would review the patent specification including, in particular, Figure 4A and 4B at issue, and realize that the '185 patent provides for various configurations, including a configuration with *exactly* two corresponding memory devices operatively coupled to each circuit.” (SIB at 152 (citing CX-093C at Q/A 976-980) and SRB at 50.)

As discussed above, the test for written description is whether the patent specification reasonably conveys “to those skilled in the art that the inventor had possession of the claimed subject matter as of the filing date.” *Ariad*, 598 F.3d at 1351. In assessing compliance with the written description requirement, it is necessary to consider “the existing knowledge in the particular field, the extent and content of the prior art, the maturity of the science or technology, and the predictability of the aspect at issue.” *Id.* However, there is no requirement to describe every feature where such feature or component is already within the knowledge of a person of

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ordinary skill in the art. *LizardTech, Inc. v. Earth Resource Mapping, Inc.*, 424 F.3d 1336, 1345 (Fed. Cir. 2005) (“[T]he patent specification is written for a person of skill in the art, and such a person comes to the patent with the knowledge of what has come before. Placed in that context, it is unnecessary to spell out every detail . . . only enough must be included to convince a person of skill in the art that the inventor possessed the invention”).

At its core, Respondents are arguing that a specific configuration having “exactly two” memory devices is not disclosed or enabled because such a configuration is not *specifically* disclosed or illustrated. On its face, this argument fails since compliance with the written description and enablement requirement does not turn on whether there is an explicit or specific disclosure. Respondents do not dispute that a configuration having “exactly” two memory devices” was within the knowledge of a person of ordinary skill in the art and given that knowledge that a person of skill would not understand what the inventor possessed. As such, Respondents’ have not shown by clear and convincing evidence that the ’185 patent lacks written description for a configuration with *exactly* two corresponding memory devices operatively coupled to each circuit.

Respondents’ enablement argument is similarly deficient. To satisfy the enablement requirement a patent specification must “contain a written description of the invention . . . to enable any person skilled in the art . . . to make and use the same.” 35 U.S.C. §112, ¶1. In this regard, the specification must enable a person of ordinary skill in the art to practice the claimed invention without undue experimentation. *See Transocean*, 617 F.3d 1296 at 1305. Respondents’ argument is again rooted in its contention that the ’185 patent does not explicitly or specifically disclose a configuration with *exactly* two memory devices. As noted above, however, Respondents do not dispute that a configuration having “exactly” two memory devices” was within the knowledge of a person of ordinary skill in the art. Moreover, given that knowledge, Respondents do not even

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address why one of ordinary skill in the art would be unable to practice the claimed subject absent undue experimentation. Indeed, Respondents' briefing does not even address the various factors considered when assessing undue experimentation (*i.e.*, the *Wands* factors). *See In re Wands*, 858 F.2d 731, 737 (Fed. Cir. 1988). As such, Respondents' have failed to show by clear and convincing evidence that the '185 patent does not enable a configuration with *exactly* two corresponding memory devices operatively coupled to each circuit.

In view of the forgoing, therefore, the undersigned finds that Respondents have failed to prove by clear and convincing evidence that the '185 patent does not comply with the written description and enablement requirements of 35 U.S.C. §112.

IX. DOMESTIC INDUSTRY - ECONOMIC PRONG

A. Netlist HyperCloud Products

Complainant submits that it has "an existing domestic industry with investments of [REDACTED] in plant and equipment in HyperCloud [REDACTED], from at least [REDACTED]," as well as "ongoing domestic activities in incorporating HyperCloud into Netlist's next-generation memory module, HybriDIMM." (CIB at 154 (emphasis in original).)

1. 337(a)(3)(A) - Significant Investment in Plant and Equipment

Netlists submits that it has established significant investment in plant and equipment for an existing domestic industry in its HyperCloud products. (*See Id.*) Specifically, Netlist submits that, between [REDACTED], it incurred facilities costs of [REDACTED] and equipment costs of [REDACTED], for a total of [REDACTED] related to its HyperCloud product. These totals represent allocated amounts. The equipment allocations are based on a ratio of Netlist's investments in HyperCloud over its total R&D investments for a given year. (*See id.* at 152-53.) Thus, for the

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HyperCloud years— [REDACTED]. (See *id.* at 153.) The facilities allocations “are based on Netlist’s annual headcount percentage of [HyperCloud] engineers in Irvine compared to total U.S. headcount.” (*Id.*) [REDACTED]. (*Id.*)

Netlist submits that these investments are both quantitatively significant and qualitatively significant. (See *id.* at 154-55.) Netlist submits that “this investment of close to [REDACTED] is a significantly high level of investment, especially for a ‘small company’ like Netlist. (*Id.* at 154.) “In terms of qualitative significance,” Netlist argues that “the R&D efforts by Netlist’s engineers in Irvine’s facilities in HyperCloud and HybriDIMM were essential to completing the key features of the domestic industry products, and have been extraordinarily important to Netlist’s business as a whole.” (*Id.* at 155.)

Staff adopts a position in line with Complainant’s. Specifically, Staff submits that “[t]he evidence shows that Complainant made investments of [REDACTED], and that these investments are significant quantitatively (compared to other product investments and overall investments), and qualitatively (compared to other products and for a small company like Complainant). (SIB at 155 (citing CX-0002C at Q/A 24, 41-42, 82-83; CX-805C [REDACTED]; CX-0001C at Q/A 88-95).)

Respondents do not address plant and equipment investments for HyperCloud specifically, but instead argue that Complainant cannot satisfy the economic prong of the domestic industry requirement based on any investments in the HyperCloud product. The basis of Respondents’ opposition is that sales for the HyperCloud products [REDACTED]. (See RIB at 148-149.) Respondents note that, for the HyperCloud products, [REDACTED]

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existence. First, *Motiva, LLC v. ITC*, 716 F.3d 596, 601 n.6 (Fed. Cir. 2013), which is the only case relied on by Respondents, does not, as Respondents suggest, stand for the proposition that a product discontinued three years prior to the filing of a complaint cannot form the basis for a domestic industry. To the contrary, *Motiva* states that “[a]lthough Motiva may have been fully engaged in developing a domestic industry for its patented technology until early 2007, there is no evidence in the record *relating that development activity* to Motiva’s efforts to establish a domestic industry at the time Motiva chose to file its complaint three years later.” *Motiva*, 716 F.3d at 601 n.6 (emphasis added). The salient failing was the lack of a relation between Motiva’s 2007 investments and its later attempt to establish a domestic industry based on licensing. *See id.* Here, by contrast, the evidence of record shows that, during the year [REDACTED], Netlist transitioned its investments from the HyperCloud product to the HybriDIMM product, but also shows that HybriDIMM draws heavily on the patented technology originally developed via the investments in the HyperCloud products. (See CX-0001C at Q/A 117-21; CX-0002C at Q/A 23, 34, 38-40, 44-54, 80-86; CX-0003C at Q/A 12-14.) Accordingly, unlike *Motiva*, here there is a relationship between Complainant’s [REDACTED] investments in HyperCloud and its ongoing investments in HybriDIMM, and that relationship is rooted in the technology described in the asserted patents. (CX-0002C at Q/A 41-42, 82-83; CX-805C.)

Further, Complainant correctly notes that the Commission has previously rejected the argument that investments in a discontinued product cannot form the basis of an existing domestic industry. (See CRB at 71 (citing *Certain Electronic Digital Media Devices and Components Thereof*, Inv. No. 337-TA-796, Comm’n Op. at 99-102 (Sept. 6, 2013); *Certain Variable Speed Wind Turbines and Components Thereof*, Inv. No. 337-TA-376, Comm’n Op. at 25 (Sept. 23, 1996)).)

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With respect to Respondents' argument that there has been no showing of a nexus between the HyperCloud expenditures and the asserted patent, the undersigned first notes that it is unclear whether Respondents' argument applies to investments shown under sections 337(a)(3)(A)-(B). The case upon which Respondents' rely for an explanation of the nexus requirement clearly ties that requirement to the phrase "in its exploitation" that appears in section 337(a)(3)(C). *See Certain Integrated Circuit Chips and Products Containing the Same*, Inv. No. 337-TA-859, Comm'n Op. at 38 (August 22, 2014) ("To meet this requirement of 'its exploitation,' the Commission requires that the complainant establish a nexus between the asserted patent and the U.S. investment in its exploitation."). The "its exploitation" language does not appear in subsection 337(a)(3)(A), upon which Complainant's investments in plant and equipment are based. *See* 19 U.S.C. § 1337(a)(3). Therefore, it is unclear from what statutory language a similar nexus requirement would arise in the context of plant and equipment investments.³⁶

For the purposes of Netlist's investments in plant and equipment for the HyperCloud products, it is sufficient to note that the evidence shows that the HyperCloud products incorporate the patented technology of the '185, '434, '501, and '064 patents. (CIB at 151 (citing CX-0001C at Q/A 80-84, 87-106, 172-73; Hong, Tr. at 181:24-183:1; CX-0002C, at Q/A 27; CX-0004C at Q/A 758, 806; CX-0005C at Q/A 978-83, 1157, 1166).) Accordingly, the undersigned finds that Complainant has made significant investments in plant and equipment

³⁶ As noted, Respondents did not address the various subsections of section 337(a)(3) individually, and so it is possible the nexus argument was only ever intended to be confined to Complainant's domestic industry investments under section 337(a)(3)(C). The briefing is simply unclear on this point.

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with respect to the HyperCloud product, and thus has satisfied the economic prong of the domestic industry requirement for the '185, '434, '501, and '064 patents.³⁷

2. 337(a)(3)(B) – Significant Investment in Labor and Capital

Netlist submits that it has an existing domestic industry in the HyperCloud product based on significant employment of labor and capital. (*See* CIB at 156.) Specifically, Netlists points to employment of ██████████ in engineering labor, and ██████████ in operations and management labor—for a total of ██████████—from ██████████ with respect to the HyperCloud product. (*Id.*) These figures represent allocated amounts. The allocations are based on the same ratios of Netlist's investment in HyperCloud versus investment in R&D overall, which, ██████████ ██████████. (*Id.* at 152-53.) Netlist further submits that these expenditures “are significant for similar reasons as stated above under 337(a)(3)(A).” (*Id.* at 156.)

As noted above, Respondents do not break their opposition into different grounds for each subsection of § 337(a)(3). Accordingly, Respondents argue that there is no existing domestic industry for the HyperCloud products based on Netlist's employment of labor and capital for the same reasons summarized in the previous section. (RIB at 148-149.)

Staff submits that, with respect to § 337(a)(3)(B), “[t]he evidence shows that Complainant made investments of ██████████, and that these investments are significant quantitatively (compared to other product investments and overall investments), and qualitatively (compared to other products and for a small company like Complainant).” (SIB at 156.)

Based on the evidence presented, the undersigned finds that Complainant has shown that it satisfies the economic prong of the domestic industry requirement based on significant

³⁷ By Complainant's own admission, the HyperCloud product does not incorporate the technology claimed in the '837 patent. (*See* CIB at 151.)

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employment of labor and capital. Specifically, the evidence shows that between [REDACTED] Complainant spent [REDACTED] on engineering labor, and [REDACTED] on operations and management labor for a combined total of [REDACTED] expended on labor related to the HyperCloud product. (See CIB at 154 (citing CX-0002C, at Q/A 13, 39-41, 50-52, 76, 79, 82-84; CX-0805C, at CX-0805C.00006 [REDACTED])

[REDACTED] Neither Staff nor Respondents challenge the significance of these expenditures, and the undersigned finds that they are indeed significant, based both on the relatively modest size of Netlist as a company, and based on the importance of the HyperCloud product to Netlist's business. Neither Respondents nor Staff challenge the allocation methodology employed by Complainant either, and the undersigned finds that Netlist's use of a ratio derived from its investment in the HyperCloud product versus Netlist's overall expenses to be a reasonable approach to allocation given the facts of this investigation.

For the reasons detailed in the previous section, the undersigned is not persuaded by Respondents' argument that expenditures for HyperCloud cannot form the basis of a domestic industry because sales of the HyperCloud product have dwindled in recent years as Netlist has transitioned its efforts to the HybriDIMM product. And, as previously noted, the nexus requirement raised by Respondents is based on statutory language that does not appear in section 337(a)(3)(B). Accordingly, the undersigned finds that Complainant has shown significant employment of labor and capital with respect to the HyperCloud product, and thus has satisfied the economic prong of the domestic industry requirement for the '185, '434, '501, and '064 patents.³⁸

³⁸ See supra at note 37.

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3. 337(a)(3)(C) – Substantial Investment in its Exploitation

Complainant submits that “under 19 U.S.C. § 1337(C), Netlist has an existing domestic industry with substantial investments of [REDACTED] invested in R&D in the United States in the exploitation of the patented technology in the developments of HyperCloud and HybriDIMM from [REDACTED]

[REDACTED] (CIB at 156 (emphasis in original).) Staff echoes Complainant’s position. (See SIB at 156.) As previously noted, Respondents did not address each category of investment under section 337(a)(3) separately.

As an initial matter, unlike the investments in plant and equipment and employment of labor and capital, here, Complainant relies on research and development covering both the HyperCloud and HybriDIMM and products, and spanning a time period from [REDACTED]. (CIB at 156; *see also id.* at 154.) Given that the evidence in this investigation demonstrates that Netlist’s HyperCloud and HybriDIMM products are closely related, and that around [REDACTED] Netlist transitioned many of its research and design efforts from HyperCloud to HybriDIMM, including incorporating technology first implemented in HyperCloud into the HybriDIMM product, the undersigned finds Complainant’s treatment of the research and development expenses as one continuous investment in the patented technology is reasonable. Indeed, while HyperCloud and HybriDIMM do invoke different names, they are not wholly dissimilar products.

As Respondents note, however, in order to establish a domestic industry under section 337(a)(3)(C), it is not sufficient to merely establish investments in research and development for the domestic industry products. (See RIB at 154 (citing *Certain Integrated Circuit Chips and Products Containing the Same*, Inv. No. 337-TA-859, Comm’n Op. at 38 (August 22, 2014).) Complainant must also show a nexus between the asserted patents and the U.S. investment in their

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exploitation. *Certain Integrated Circuit Chips and Products Containing the Same*, Inv. No. 337-TA-859, Comm'n Op. at 38 (August 22, 2014). The Commission has explained that "this nexus may readily be inferred based on evidence that the claimed investment is in the domestic industry article, which itself is the physical embodiment of the asserted patent." *Id.* at 40. Further, the Commission has explained that "no patent-by-patent allocation is required for research and development investment under subparagraph (C)." *Id.* at 41. The Commission reasoned that such an approach would risk "freezing cognizable investment at the point at which the patented technology is reduced to practice," and would run contrary to the reality that "most firms have little reason to keep research and development records on a patent-by-patent basis, as opposed to a project-by-project basis (to the extent that project-by-project records are kept)." *Id.* at 41-42. In the context of this guidance from the Commission, Respondents' nexus argument is unpersuasive.

With respect to drawing a nexus between the HyperCloud and HybriDIMM products and the asserted patents, Complainant submits that "[b]oth HyperCloud and HybriDIMM are the results of Netlist's domestic investments in exploiting the patented technology of all five Asserted Patents." (CIB at 156 (citing CX-0001C at Q/A 75.)) Further, Complainant submits that "[s]ubstantially all of the effort to exploit the patented technology in Netlist's HyperCloud and HybriDIMM products has occurred, and still occurs, in the United States, at Netlist's facilities in Irvine," (*id.* (citing CX-0001C at Q/A 25-48, 77, 82-83, 86, 88-96, 117-121, 129-133, 161; CX-0002C at Q/A 13, 16-19, 24-27, 56-76; CX-0003C at Q/A 12-39, 49, 54)), and "[b]oth HyperCloud and HybriDIMM incorporate Netlist's patented distributed buffer architecture, as claimed in the '185 Patent, and Netlist's self-test technologies, as claimed in the '434, '501, and '064 Patents, each of which were developed by Netlist's engineers in Irvine." (*Id.* at 156-57 (citing CX-0001C

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at Q/A 81-84, 87-96, 117-24, 167; Hong, Tr. at 181:24-183:1; CX-0004C at Q/A 576-79, 593, 758, 806; CX-0005C at Q/A 632, 978-83, 1157, 1166; CX-0060C.)

Consistent with the findings *supra* that the HyperCloud products satisfy the technical prong of the domestic industry requirement for the '434, '501, '064, and '185 patents, *see supra* §§ IV.E, V.E, VI.E, VIII.E, and the evidence of record showing that the research and development related to the HyperCloud products was conducted within the United States, (*see* CX-0001C at Q/A 25-48, 77, 82-83, 86, 88-96; CX-0002C at Q/A 13, 16-19, 24-27), the undersigned finds that Complainant has established a nexus between its research and development activities and those four asserted patents based on the patented articles themselves, *i.e.*, the HyperCloud products. Respondents have not provided an adequate basis to contest the evidence offered by Complainant with respect to these four patents. *See Certain Integrated Circuit Chips and Products Containing the Same*, Inv. No. 337-TA-859, Comm'n Op. at 38 (August 22, 2014) ("Requiring an extensive inquiry as to the adequacy of the nexus when it is not challenged on the merits by respondents would unduly consume the time and resources of the parties and the Commission given the Commission's experience that in most factual situations a patent is exploited in research and development efforts concerning products that practice the patent."). Rather, Respondents have simply alleged that Complainant completely ignored the nexus requirement, which is not accurate. (*Compare* RRB at 81 ("Netlist says not a word about the portion of its expenditures associated with HyperCloud and HybridDIMM that actually relate to the patents at issue") *with* CIB at 156-57.)

However, Complainant concedes that the HyperCloud products do not practice the '837 patent. (*See* CIB at 157.) Rather, Complainant submits that "Netlist's patented initialization technology, as claimed in the '837 patent, innovated during the course of the HyperCloud design

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effort, is incorporated into HybriDIMM.” (*Id.*) Accordingly, Complainant cannot rely on the HyperCloud products to make an articles-based nexus showing between its research and development activities and the ’837 patent. Moreover, because the undersigned has determined that the HybriDIMM products do not practice the ’837 patent, *see supra* at § VII.E, Complainant also cannot make an articles-based nexus showing between its research and development activities and the ’837 patent based on its HybriDIMM products.

Complainant’s assertion that the technology of the ’837 patent was nonetheless “innovated during the course of the HyperCloud design effort” is not sufficient to establish a nexus between its research and development expenditures and the technology of the ’837 patent. (CIB at 157.) The evidence Complainant cites in support of that assertion is simply too conclusory, or irrelevant, to determine that a substantial portion of its research and development activities were directed to exploitation of the ’837 patent. (*See* CX-0001C at Q/A 75; CX-0005C at Q/A 1496.) This is particularly true given that Complainant has opted to allocate its research and development costs based solely on ratios between spending on the HyperCloud and HybriDIMM products versus its overall research and development spending. Given that neither product practices the ’837 patent, the undersigned cannot discern a reliable basis in the evidence to find a nexus between Netlist’s research and development spending and the ’837 patent.

Accordingly, the undersigned finds that Netlist has shown that it satisfies the economic prong of the domestic industry requirement based on a substantial investment in the exploitation through research and development of the ’434, ’501, ’064, and ’185 patents. The undersigned further finds that Netlist has not shown a substantial investment in the exploitation of the ’837 patent, however, and therefore does not satisfy the economic prong with respect to that patent.

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B. Netlist HybriDIMM Products

Complainant also submits that it “has a domestic industry in the process of being established under subsection (A) with [REDACTED] invested in domestic plant and equipment in HybriDIMM [REDACTED] under subsection (B) with [REDACTED] invested in domestic labor in HybriDIMM [REDACTED], and under subsection (C) with [REDACTED] invested in the domestic research and development of the patented technology incorporated into HybriDIMM [REDACTED], which are all investments from [REDACTED].” (CIB at 158 (emphasis in original).) Respondents disagree, arguing [REDACTED] preclude Complainant from establishing a domestic industry in the process of being established. (See RIB at 149-154.) Staff argues that Complainant has established a domestic industry in the process of being established for the HybriDIMM product based on 337(a)(3)(A), (B), and (C), and dismisses Respondents concerns about the likelihood that the domestic industry will actually be established as either misplaced or overstated. (SIB at 156-158.)

Because the undersigned has already found that Complainant has satisfied the economic prong of the domestic industry requirement with respect to the '434, '501, '064, and '185 patents through the existence of a domestic industry with respect to the HyperCloud products, the domestic industry for those patents need not be addressed a second time here. With respect to the '837 patent, the undersigned has found that the HybriDIMM products do not satisfy the technical prong of the domestic industry requirement for that patent. Thus, whether Netlist can satisfy the economic prong of the domestic industry requirement for the '837 patent through an

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industry in the process of being established for the HybriDIMM products will not change the ultimate conclusion that Netlist has not established a domestic industry for the '837 patent. *See In the Matter of Certain Computers & Computer Peripheral Devices, & Components Thereof, & Prod. Containing Same*, Comm'n Opinion, USITC Inv. No. 337-TA-841 (Jan. 9, 2014) ("Based on the *InterDigital* and *Microsoft* decisions, a complainant alleging the existence of a domestic industry under 19 U.S.C. § 1337(a)(3)(C) must show the existence of articles.").

The undersigned notes that, should the Commission determine that the HybriDIMM products do practice the '837 patent, then Complainant would be able to show a domestic industry in existence for the '837 patent based on investments in the exploitation of the '837 patent through research and development of the HyperCloud and HybriDIMM products. (*See* CIB at 156-57.)

X. CONCLUSIONS OF LAW

1. The Commission has personal jurisdiction over the parties, and subject-matter jurisdiction over the accused products.
2. The importation or sale requirement of section 337 is satisfied as to all Respondents.
3. Respondents do not infringe any asserted claim of U.S. Patents No. 8,001,434; 8,359,501; 8,689,064; 8,489,837; or 8,516,185.
4. The asserted claims of U.S. Patent No. 8,001,434 are not invalid under 35 U.S.C. §102 as anticipated.
5. The asserted claims of U.S. Patent No. 8,001,434 are not invalid under 35 U.S.C. §112 as indefinite.
6. The asserted claims of U.S. Patent No. 8,359,501 are not invalid under 35 U.S.C. §102 as anticipated.
7. The asserted claims of U.S. Patent No. 8,359,501 are not invalid under 35 U.S.C. §112 as indefinite.
8. The asserted claim of U.S. Patent No. 8,689,064 is not invalid under 35 U.S.C. §102 as anticipated.
9. The asserted claim of U.S. Patent No. 8,689,064 is not invalid under 35 U.S.C. §112 as indefinite.

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10. The asserted claims of U.S. Patent No. 8,489,837 are not invalid under 35 U.S.C. §102 as anticipated.
11. The asserted claims of U.S. Patent No. 8,489,837 are not invalid under 35 U.S.C. §103 as obvious.
13. The asserted claims of U.S. Patent No. 8,516,185 are not invalid under 35 U.S.C. §102 as anticipated.
14. The asserted claims of U.S. Patent No. 8,516,185 are not invalid under 35 U.S.C. §103 as obvious.
15. The asserted claims of U.S. Patent No. 8,516,185 are not invalid under 35 U.S.C. §112 as failing to comply with the written description and/or enablement requirements.
16. The technical prong of the domestic industry requirement for U.S. Patent No. 8,001,434 has been satisfied.
17. The technical prong of the domestic industry requirement for U.S. Patent No. 8,359,501 has been satisfied.
18. The technical prong of the domestic industry requirement for U.S. Patent No. 8,689,064 has been satisfied.
19. The technical prong of the domestic industry requirement for U.S. Patent No. 8,489,837 has not been satisfied.
20. The technical prong of the domestic industry requirement for U.S. Patent No. 8,516,185 has been satisfied.
21. The economic prong of the domestic industry requirement has been satisfied for U.S. Patents No. 8,001,434; 8,359,501; 8,689,064; and 8,516,185.
22. The economic prong of the domestic industry requirement has not been satisfied for U.S. Patent No. 8,489,837.

XI. RECOMMENDED DETERMINATION ON REMEDY & BOND

The Commission's Rules provide that the administrative law judge shall issue a recommended determination concerning the appropriate remedy in the event that the Commission finds a violation of section 337, and the amount of bond to be posted by respondents during Presidential review of the Commission action under section 337(j). *See* 19 C.F.R. § 210.42(a)(l)(ii).

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A. Limited Exclusion Order

Under section 337(d), the Commission may issue a limited exclusion order (“LEO”) directed to a respondent's infringing products. 19 U.S.C. §1337(d). A limited exclusion order instructs the U.S. Customs Service to exclude from entry all articles that are covered by the patent at issue that originate from a named respondent in the investigation. *See Fuji Photo Film Co. Ltd. v. Int'l Trade Comm'n*, 474 F.3d 1281, 1286 (2007).

Complainant argues that, “[i]n the event a violation of Section 337 is found based upon the infringement of one or more asserted claims of the Asserted Patents, the ALJ should recommend that the Commission issue a Limited Exclusion Order directed to the products of the named Respondents, pursuant to 19 U.S.C. § 1337(d), excluding any articles that infringe one or more claims of the Asserted Patents.” (CIB at 195.) Complainant does not seek a general exclusion order.

Respondents do not dispute that, in the event a violation of section 337 is found, a LEO should issue. However, Respondents argue that enforcement of any LEO should be delayed by at least 12 to 18 months in order to mitigate adverse effects to the public interest. (RIB at 198.) Additionally, Respondents suggest a litany of exceptions and modifications to any exclusion “to mitigate harm to the public.” (*Id.*) These include:

1. an exception to accommodate service, repair, replacement, and “update” obligations with respect to SK hynix’s products already sold to customers;
2. an exception for future products that will be imported for sale for the first time after the close of the record;
3. an exception for products imported solely for research and testing purposes;
4. an exception for devices within the scope of this Investigation that are sold to or used by the U.S. Government; and
5. a certification provision.

(RIB at 198-199.)

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Staff submits that, “[s]hould a Section 337 violation be found, the Staff recommends the issuance of a limited exclusion order directed to infringing articles that are manufactured abroad by or on behalf of, or imported by or on behalf of, any of the Respondents or any of their affiliated companies, parents, subsidiaries, or other related business entities, or their successors or assigns.” (SIB at 163.) Staff also supports delaying enforcement of any exclusion order by 3 to 6 months. With respect to the exceptions proposed by Respondents, Staff “does not object to Respondents’ proposed certification provision and government exemption, which appear to the Staff to be similar to provisions normally included in limited exclusion orders issued by the Commission,” but “does object, however, to Respondents’ proposed carve out for ‘products imported solely for research and testing’ and exemption for ‘service, repair, replacement, and ‘update’” of SK hynix’s products, because the record does not include evidence establishing that these provisions are necessary or appropriate.” (SRB at 55.)

In the event the Commission finds a violation, the undersigned recommends that a limited exclusion order issue prohibiting the importation of Respondents’ LRDIMMs and RDIMMs found to infringe the asserted patents. The undersigned also recommends the inclusion of a provision whereby Respondents can certify that certain products are not subject to exclusion, as memory modules may be imported as subcomponents of larger devices, and ascertaining whether the modules are subject to the exclusion order would be difficult. The undersigned further notes that Respondents’ request for an exception for products sold to or used by the U.S. Government appears to be substantively identical to the requirement of 19 U.S.C. § 1337(l), which provides that:

Any exclusion from entry or order under subsection (d), (e), (f), (g), or (i), in cases based on a proceeding involving a patent, copyright, mask work, or design under subsection (a)(1), shall not apply to any articles imported by and for the use of the United States, or imported for, and to be used for, the United States with the authorization or consent of the Government.

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19 U.S.C. § 1337(l). As noted by Staff, a provision recognizing this requirement is typically present in the Commission's exclusion orders. The undersigned does not recommend incorporating the other exceptions requested by Respondents, as the record does not support them.

B. Cease and Desist Order

Under section 337(f)(1), the Commission may issue a cease and desist order ("CDO") in addition to, or instead of, an exclusion order. 19 U.S.C. § 1337(f)(1). The Commission generally issues a cease and desist order directed to a domestic respondent when there is a "commercially significant" amount of infringing, imported product in the United States that could be sold, thereby undercutting the remedy provided by an exclusion order. *See Certain Crystalline Cefadroxil Monohydrate*, Inv. No. 337-TA-293 USITC Pub. 2391, Comm'n Op. on Remedy, the Public Interest and Bonding at 37-42 (June 1991); *Certain Condensers, Parts Thereof and Prods. Containing Same, Including Air Conditioners for Automobiles*, Inv. No. 337-TA-334 (Remand), Comm'n Op. at 26-28, 1997 WL 817767, at *11-12 (U.S.I.T.C. Sept. 10, 1997).

In the event a violation of Section 337 is found, Complainant argues that a CDO should issue prohibiting SK Hynix America, Inc. from engaging in the unlawful importation and/or sale within the United States of infringing articles. (CIB at 195.) Complainant submits that "the evidence shows that Respondent entity SK Hynix America, Inc. maintains a commercially significant inventory of Accused Products." (*Id.* (citing CX-0277C at 89:22-91:21; CX-0993C; RX-0001C at Q/A 40-43).)

Respondents contend that Complainant has not shown the need for a CDO, nor has it shown that SK hynix maintains commercially significant inventories of the accused products in the United States. (*See* RIB at 199.) In the event a CDO does issue, Respondents contend that the order should be delayed for the same reasons it submitted with respect to the LEO. (*Id.*)

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Staff submits that “[t]he evidence shows that SK hynix America maintains a commercially significant inventory of accused products,” because, [REDACTED] [REDACTED] (SIB at 164 (citing CX-0993C (Inventory Listing); RX-0001C (Kim WS), at Q/A 40-43).) Accordingly, Staff takes the position that if the Commission finds a violation of section 337, “issuance of a cease and desist order to SK hynix America is appropriate.” (SIB at 164.) Staff further notes that “[t]he other Respondents are affiliated with SK hynix America and would thus be bound by a cease and desist order containing the Commission’s standard language.” (*Id.*)

Should the Commission find a violation of section 337, the undersigned does not recommend that a cease and desist order issue to SK hynix America. Both Complainant and Staff rely on exhibits that were withdrawn and thus are not in evidence. These exhibits are CX-0277C and CX-0993C. The only other exhibit cited by Complainant and Staff, RX-0001C at Q/A 40-43, does not address the volume of any domestic inventory held by SK hynix America. Accordingly, the record does not support a finding that SK hynix America maintains a commercially significant inventory, and thus the undersigned does not recommend issuance of a cease and desist order.

C. Bond During Presidential Review

Pursuant to section 337(j)(3), the Administrative Law Judge and the Commission must determine the amount of bond to be required of a respondent during the 60-day Presidential review period following the issuance of permanent relief, in the event that the Commission determines to issue a remedy. *See* 19 U.S.C. §1337(j)(3). The purpose of the bond is to protect the complainant from any injury. *See* 19 C.F.R. § 210.42(a)(1)(ii), § 210.50(a)(3).

When reliable price information is available, the Commission has often set the bond by eliminating the differential between the domestic product and the imported, infringing product.

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See Microsphere Adhesives, Processes for Making Same, and Prods. Containing Same, Including Self-Stick Repositionable Notes, Inv. No. 337-TA-366, USITC Pub. 2949, Comm'n. Op. at 24 (Dec. 8, 1995). In other cases, the Commission has turned to alternative approaches, especially when the level of a reasonable royalty rate could be ascertained. *See, e.g., Certain Integrated Circuit Telecomm. Chips and Prods. Containing Same, Including Dialing Apparatus*, Inv. No. 337-TA-337, Comm'n. Op. at 41, 1993 WL 13033517, at *24 (U.S.I.T.C. June 22, 1993). A 100 percent bond has been required when no effective alternative existed. *See, e.g., Certain Flash Memory Circuits and Prods. Containing Same*, Inv. No. 337-TA-382, USITC Pub. No. 3046, Comm'n. Op. at 26-27 (July 1997) (imposing a 100% bond when price comparison was not practical because the parties sold products at different levels of commerce, and the proposed royalty rate appeared to be *de minimus* and without adequate support in the record).

Complainant argues that a 100 percent bond is appropriate because “[t]he sheer number of Accused Products, with different features and configurations, make it difficult to compute the price differential between the Accused Products and those of Netlist.” (CIB at 196.)

Respondents submit that Netlist has not shown the need for a bond, or that the 100 percent proposed bond is necessary to protect itself from injury. (RIB at 200.) Particularly, Respondents argue that “Netlist has not alleged its products actually compete with SK hynix’s accused products,” and that “Netlist has provided no evidence demonstrating any injury would occur during the Presidential review period or the extent of any such injury.” (*Id.*) Finally, Respondents argue that, “[t]o the extent the Commission nonetheless decides to impose a bond, it should be no more than a reasonable royalty consistent with Netlist’s RAND licensing commitments, and certainly less than Netlist’s demand of ■ per LRDIMM and ■ per RDIMM.” (*Id.*)

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Staff argues in favor of a 100 percent bond rate because “there is insufficient information to set a bond based on price differentials or royalty rates.” (SIB at 165.)

Should the Commission find a violation of section 337 by Respondents, the undersigned does not recommend entry of any bond. Neither Complainant nor Staff identifies a connection between their proposed 100 percent bond rate and an injury that would be suffered by Complainant. Nonetheless, “Complainant bears the burden of establishing the need for a bond amount in the first place.” *Certain Cast Steel Railways Wheels, Processes for Manufacturing or Relating to Same and Certain Prods. Containing Same*, Inv. No. 337-TA-655, Comm’n Op. at 12 (Mar. 19, 2010). Whether Complainant can meet that burden here is not clear, [REDACTED]

[REDACTED]. In the absence of a competing product, it is not clear what injury Complainant will suffer from Respondents’ products being imported during the 60-day Presidential review period. The burden rests with Complainant to articulate the justification for a bond, but here, Complainant appears to assume that if there is a violation of section 337, it is entitled to a bond. (See CIB at 196.) Having provided no legal support for that position, and Commission precedent strongly suggesting there is none, see *Certain Cast Steel Railways Wheels.*, Inv. No. 337-TA-655, Comm’n, Op. at 12 (Mar. 19, 2010), the undersigned does not recommend imposition of any bond during the Presidential review period.

XII. PUBLIC INTEREST

In connection with this Recommended Determination, and pursuant to Commission Rule 210.50(b)(1), 19 C.F.R. § 210.50(b)(1), the Commission ordered that the presiding administrative law judge:

[S]hall take evidence or other information and hear arguments from the parties or other interested persons with respect to the public interest in this investigation, as

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appropriate, and provide the Commission with findings of fact and a recommended determination on this issue, which shall be limited to the statutory public interest factors set forth in 19 U.S.C. §§ 1337(d)(1), (f)(1), (g)(1).

(81 Fed. Reg. 69,854 (Oct. 7, 2016).)

Before issuing a remedy for a violation of section 337, the Commission must consider the effect of the remedy on the following public interest factors: (1) the public health and welfare; (2) competitive conditions in the U.S. economy; (3) the U.S. production of articles that are like or directly competitive with those that are the subject of the investigation; and (4) U.S. consumers. *See* 19 U.S.C. §§ 1337(d)(1), (f)(1). The Commission begins this analysis with the understanding that the public interest favors the protection of intellectual property rights by excluding infringing products. *See, e.g., Certain Two-Handle Centerset Faucets & Escutcheons & Components Thereof, Inc. No. 337-TA-422, Comm'n Op. at 9 (July 21, 2000).* It is rare for the Commission to determine that the public interest considerations outweigh the patent holder's rights. *See Spansion Inc. v. Int'l Trade Comm'n, 629 F.3d 1331, 1360 (Fed. Cir. 2010).* The Commission can, however, tailor the remedy to minimize the impact on the public interest. *See e.g., Certain Personal Data and Mobile Commc'ns Devices & Related Software, Inv. No. 337-TA-710, Comm'n Op. at 83 (delaying the effective date of an exclusion order based on competitive conditions in the U.S. economy).*

A. Public Health and Welfare

Complainant submits that “[a]n LEO as to the Accused Products will not have any material negative impact on U.S. public health or welfare within the context of Section 337,” because “[t]he Accused Products are not necessary for any health or welfare need, such as basic scientific research, or hospital equipment.” (CIB at 184.) Nonetheless, Complainant argues that “[t]o the extent DDR4 RDIMMs and LRDIMMs have applications relevant to public health, safety, or welfare, sufficient suitable substitutes are available.” (*Id.*) To the extent Respondents

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argue that an exclusion order would affect the public health and welfare, Complainant counters that Respondents have failed to “provide any information on how the Accused Products were used, what proportion was used in the U.S., or how many Accused Products were purchased by specific customers.” (*Id.*) Complainant is particularly critical of Respondents’ expert, Mr. Davies, whose opinions it asserts are “untethered to any real facts.” (*Id.*)

Staff also argues that an exclusion order will not adversely affect the public health and welfare. (*See* SIB at 160.) Particularly, Staff notes that “[t]he products at issue in this investigation are memory modules (for servers primarily), not the types of products necessary for health and welfare.” (*Id.*)

Respondents nominally argue that “[t]he exclusion of the accused products from the domestic memory module market would cause severe supply disruptions that would adversely impact public health and welfare, and harm competitive conditions in the U.S. economy.” (RIB at 187-188.) However, Respondents offer little in the way of explanation or evidence to support that assertion with respect to the public health and welfare. In Respondents’ public interest briefing, the only passage even tangentially addressing the public health and welfare is the following:

Representative examples of sectors of the U.S. economy that are dependent on modern computing include: healthcare, consumers, education, government, high performance computing applications, and innovation, but this list is by no means exhaustive. For example, the healthcare sector is heavily reliant on modern computing, for electronic health record, patient diagnosis, and research.

(*Id.* at 194 (citing RX-0004C at Q/A 90-98).)³⁹

The undersigned agrees with Complainant and Staff that there is no evidence indicating that an exclusion order would adversely affect the public health and welfare. Respondents’

³⁹ Respondents’ briefing is not organized by public interest factor, which has further contributed to the difficulty in identifying Respondents’ position on this particular factor.

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assertion to the contrary is unacceptably broad, and among other things, is predicated on a lack of access to “modern computing,” not the specific memory modules at issue in this investigation. (*See Id.*) The testimony from Mr. Davies, upon which Respondents rely, is similarly misdirected to the impact of “modern computing” on the health industry. (*See* RX-0004C at Q/A 90-98.) The evidence does not show that all modern computing technology will suddenly become unavailable for healthcare uses if an exclusion order for certain memory modules issues in this case. Accordingly, the undersigned finds that there is no evidence that the public health and welfare will be adversely affected by an exclusion order in this investigation.

B. Competitive Conditions in the U.S. Economy

Complainant submits that an exclusion order in this case will have no effect on competitive conditions in the United States. (CIB at 192.) First, Complainant argues that the global nature of the market for memory modules will reduce any impact on competitive conditions within the U.S. (*Id.*) Complainant reasons that there may be a geographical shift in supply of DDR4 products as Respondents divert their supply of accused products to foreign markets, and other manufacturers step in to supply the residual demand in the U.S. market (*Id.*) Second, Complainant argues that because an exclusion order would not cover Respondents’ DRAM chips, but instead only whole memory modules, the market would achieve equilibrium as Respondents re-direct their DRAM chips to other products. Complainant explains that it is the number of DRAM chips, not modules, that constrains the number of memory modules supplied to the market. (*Id.* at 193.) Accordingly, Complainant posits that Respondents could partner with other module manufacturers by supplying its DRAM chips, thus increasing the number of memory modules available to fill the gap left by Respondents’ memory modules. (*Id.* (citing CX-0006C at Q/A 308).) Alternatively, Respondents could make its DRAM chips available for other applications, thereby increasing supply of memory

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in other markets, which would in turn incentivize producers in those markets to re-allocate their production capabilities to the memory module market. (*Id.*)

Finally, Complainant submits that, “even when prices for memory modules have increased due to a DRAM-supply shortage, that increase in price has been only temporary.” (*Id.* at 194 (citing CX-0006C at Q/A 314; *see* also CX-0757C).) Complainant submits that “[p]rices for RDIMM products have flattened out typically within six to seven months due to either DRAM-supply improvement or demand adjustment.” (*Id.* (citing CX-0757C))

Respondents counter that “[t]he exclusion order sought by Netlist would eliminate from the U.S. market the second biggest supplier of server DRAM RDIMMs and LRDIMMs worldwide, in what is essentially a three supplier market.” (RIB at 189 (citing RDX-1582C.18-19; RX-1582C at Q/A 153-154).) Respondents reject Complainant’s contention that Respondents’ market share for RDIMMs and LRDIMMs could be readily replaced. (*Id.* at 189). Respondents argue that this is due to supply chain constraints, and the fact that the DRAM industry does not currently have excess capacity. (*Id.* at 189-190.) Respondents further counter that “there are no measures that could eliminate the supply constraints caused by an exclusion order within a commercially reasonable time frame.” (*Id.* at 190.) Finally, Respondents note that, while the supply of RDIMMs and LRDIMMs from other the other manufacturers could increase to meet the demand created by the exclusion of Respondents’ products, such rebalancing would not happen quickly. (*Id.* at 191-192.) Respondents estimate that it would take 24 months for RDIMM and LRDIMM manufacturers to renegotiate contracts and modify their supply chains to address the shortfall caused by Respondents’ exclusion from the domestic market for memory modules. (*Id.* at 192-93.)

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Staff takes the position that “the evidence does not support denying, but instead supports tailoring, the requested remedial orders” with respect to competitive conditions in the U.S. economy. (SIB at 160.) Staff reasons that due to the fact that there are only three primary suppliers of RDIMMs and LRDIMMs in the U.S., and the fact that only Samsung of those three is licensed under the asserted patents, “the exclusion of SK hynix from the memory market may adversely affect competitive conditions in the U.S. economy due to there being only two competitors remaining in the memory market in the U.S.” (*Id.*) Accordingly, Staff recommends “delaying entry of an exclusion order by three months to six months may be appropriate.”

The undersigned finds that the evidence presented does not support denying any otherwise appropriate remedial orders, but does support delaying their enforcement. Particularly, the evidence shows that there effectively only three suppliers of RDIMMs and LRDIMMs for the U.S. market: Respondents, Samsung, and Micron. (RX-1582C at Q/A 154.) The evidence further shows that Respondents provide around one third of that supply. (*Id.* at Q/A 250-251.) While the parties appear to be in agreement that the supply and demand for LRDIMMs and RDIMMs in the U.S. market would eventually reach equilibrium in the event of an exclusion of Respondents’ products, they differ in how long that exclusion would take. The evidence presented on this point is primarily in the form of expert testimony from Mr. Davies and Mr. Sidak. (*See* RX-0004C at Q/A 343; Sidak, Tr. at 565:11-566:18, 570:5-571:6.) While Mr. Sidak submits that the market would reach equilibrium in as little as three months and at most twelve months, Mr. Davies submits that it would take from twelve months to 18 months for the market to reach equilibrium. (*See* RX-0004C at Q/A 343; Sidak, Tr. at 565:11-566:18, 570:5-571:6.) Staff, for its part, submits that a three to six month delay would be appropriate. (SRB at 54.)

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The undersigned finds that a delay of six to twelve months for any exclusion order would be appropriate. Particularly, Respondents identify a number of assumptions relied on by Mr. Sidak in forming his opinions that are questionable. (*See* RIB at 195-197.) For instance, in considering substitutes for the Respondents' LRDIMMS and RDIMMs, Mr. Sidak appears to have considered non-JEDEC compliant memory modules, as well as memory modules practicing older generations of the RDIMM and LRDIMM standards to be suitable substitutes for Respondents' DDR4 products. (*See* CX-0006C at Q/A 199.) Respondents' expert, Mr. Davies, persuasively rebuts that assumption. (*See* RX-1582C at Q/A 64-65.) Further, during the hearing, Mr. Sidak testified that: "I certainly think that a year after the exclusion order, the market would have re-equilibrated. I think it's likely it would happen within six months, maybe it would happen within three months." (Sidak, Tr. at 565:11-18; *see also id.* at 559:10-25.) Contrary to Complainant's position, Mr. Sidak displayed little confidence that the market RDIMMs and LRDIMMs would return to equilibrium earlier than six months after entry of an exclusion order. (*Id.* at 565:11-18, 565:23-24.) Accordingly, the undersigned cannot find evidence to support a delay as short as three months, as suggested by Staff. There is, however, substantial support in the record that a delay of six to 12 months would allow the market to return to substantial equilibrium. (*See* RX-0004C at Q/A 343; Sidak, Tr. at 565:11-566:18, 570:5-571:6.) Accordingly, the undersigned recommends that any exclusion order for the accused products be delayed by six to twelve months on the basis of this public interest factor.

C. Production of Like or Directly Competitive Products in U.S.

Complainant argues that an exclusion order would have no effect on the production of like or directly competitive articles in the United States. (CIB at 185-192.) Staff agrees. (SIB at 161.) Respondents do not address this statutory public interest factor with particularity in its

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briefing, and the undersigned cannot ascertain a portion of that briefing that is clearly on point. Accordingly, the undersigned finds no evidence that an exclusion order would have an adverse effect on the production of likely or directly competitive products in the U.S.

D. U.S. Consumers

Complainant submits that a limited exclusion order will have no meaningful adverse effect on U.S. Consumers. (CIB at 194.) Complainant argues that “[i]ndividual consumers – aside from sophisticated business entities – typically do not buy servers that use DDR4 RDIMMs and LRDIMMs,” and thus consumers are “unlikely to experience any price effect from an LEO.” (*Id.*) Complainant further asserts that “[a]n LEO would not likely raise quality-adjusted prices significantly for servers” because DDR4 RDIMMs and LRDIMMs [REDACTED]

[REDACTED] (*Id.* (citing CX-0006C at Q/A 319).)

Staff argues that “the evidence does not support denying, but does support tailoring, the requested remedial orders,” on the basis of this public interest factor. (SIB at 161.) Staff reasons that “[t]he exclusion of SK hynix’s products could adversely affect the available supply of RDIMMs and LRDIMMs for manufacturers who purchase them to manufacture servers,” and that because “[s]uch servers have a multitude of computing uses, and an exclusion may ultimately affect consumers of downstream products or services.” (*Id.*) Ultimately, Staff recommends the same modification as it did based on competitive conditions: delaying the entry of an exclusion order by three to six months. (*Id.*)

Respondents do not address the effects of an exclusion order on U.S. consumers with particularity, but do make reference to consumers in the context of its other public interest arguments. For instance, in the context of supply chain constraints, Respondents submit that, “even if Samsung and Micron did pursue the unlikely course of shifting manufacturing

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production away from other types of memory to server memory, the public interest would be harmed by a lack of memory in other segments such as mobile, PC, and other consumer areas.” (RIB at 191.) Further, in arguing that the effects of an exclusion order would be widespread, Respondents note that “[c]onsumers rely on computing devices, especially smartphones, that are enabled by servers containing RDIMMs and LRDIMMs. (RIB at 194.) And, in the context of discussing a potential single-supplier market, *i.e.*, Samsung as sole supplier, “Respondents assert that “[a] one-supplier RDIMM and LRDIMM market is more susceptible to market disruption, is less competitive in terms of both price and innovation, and will harm downstream consumers, as well as the broader U.S. computing industry and economy.” (*Id.*)

The undersigned finds that the evidence and arguments relied on by Respondents with respect to this factor have significant overlap with the competitive conditions in the U.S. factor. Particularly, to the extent U.S. consumers would be harmed by an exclusion order, the harm Respondents point to derives from downstream activities that might be affected by a disruption to the current supply and demand for servers using DDR4 RDIMMs and LRDIMMs. (*See Id.* at 193-94.) The evidence does not show, by contrast, that there is a significant market among individual consumers as end users for RDIMMs and LRDIMMs. (CX-0006C at Q/A 318.)

Further, like their arguments about the public health and welfare, many of Respondents’ arguments about harm to U.S. consumers are based not on an absence of RDIMMs or LRDIMMs in the market, but on assumption that modern computing would become less accessible to consumers due to an exclusion order. (*See RIB* at 193-94.) While there is certainly a link between the accused memory modules, servers, and a wide variety of computing technology that affects consumers daily in the U.S., the undersigned is not persuaded that the evidence supports the conclusion that an exclusion order for Respondents’ RDIMMs and LRDIMMs will necessarily

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have the significant detrimental effect on all of modern computing that Respondents suggests. Accordingly, the undersigned recommends that this factor be viewed at most as an additional reason to delay the entry of an exclusion order for between six and twelve months, as described *supra* in the discussion of competitive conditions in the U.S. economy.

E. RAND Obligations

In addition to the four statutory factors discussed above, the parties also submitted substantial briefing on whether a RAND (“reasonable and non-discriminatory”) licensing obligation on the part of Netlist weighed against issuance of an exclusion order. (See CIB at 162-182; CRB at 74-83; RIB at 155-187; RRB at 81-94; SIB at 161-163.) As an initial matter, the undersigned notes that the Notice of Institution for this investigation gave clear instructions that the presiding administrative law judge:

[s]hall take evidence or other information and hear arguments from the parties or other interested persons with respect to the public interest in this investigation, as appropriate, and provide the Commission with findings of fact and a recommended determination on this issue, ***which shall be limited to the statutory public interest factors set forth in 19 U.S.C. 1337(d)(1), (f)(1), (g)(1).***

81 Fed. Reg. 69,854 (Oct. 7, 2016) (emphasis added). None of the parties explicitly connect their RAND arguments to the statutory public interest factors, *i.e.*, the public health and welfare, competitive conditions in the United States economy, the production of like or directly competitive articles in the United States, and United States consumers. See 19 U.S.C. § 1337(d)(1), (f)(1), (g)(1). Nonetheless, all parties treat the RAND issue in the context of public interest, as opposed to, for example, a defense to patent infringement. Accordingly, the undersigned addresses the issue here.

The alleged RAND obligation in this investigation stems from the standard setting organization JEDEC (“Joint Electron Device Engineering Council”). Specifically, JEDEC Manual Section 8.2.4 provides:

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Subject to the terms and conditions of section 8.2.4, each Committee Member, as a condition of Participation, agrees to offer to license on RAND terms, to all Potential Licensees, such Committee Member's Essential Patent Claims for the use, sale, offer for sale or other disposition of a portion of a product in order to be compliant with the required portions of a final approved JEDEC Standard issued during the period of membership in that committee. The licensing commitment does not apply to Essential Patents of a Committee Member where notice of a Refusal to License has been given by the Committee Member in accordance with 8.2.3.1.

(CX-0325 at 34.) Thus, absent certain exceptions not applicable here, the JEDEC manual places a RAND licensing obligation on JEDEC Committee Members with respect to the member's "Essential Patent Claims." Relatedly, section 8.2.3 provides in part that:

All Committee Members must Disclose Potentially Essential Patents, known to their Representative(s) to be Potentially Essential Patents that are owned or controlled by that Committee Member to the personal knowledge of the Representatives.

(CX-0325 at 33.) Thus, the JEDEC Manual articulates a system where committee members are required to disclose "potentially essential patents" to the other JEDEC committee members, but attaches a RAND licensing obligation only to those patent claims that are actually essential to a final approved JEDEC standard. (*See id.* at 33-34.) Thus, a necessary pre-requisite to any determination that Complainant has violated a RAND licensing obligation is a showing that the asserted patents in this investigation are actually standard essential. If the asserted patents are not essential to a JEDEC standard, Netlist does not have a RAND licensing obligation for those patent claims according to the terms of the JEDEC Manual. (*See id.* at 34.)

On this first point, Staff argues that, because the asserted patent claims are not infringed, they "cannot be 'essential' to the practice of the JEDEC standards." (SIB at 162 n.17.) The reasoning behind that statement relies on the fact that the accused products are in fact JEDEC compliant. (*See CX-0005C at Q/A 222, 310.*) If the accused products comply with JEDEC standards, then a standard essential patent would necessarily be infringed by those products. The converse is not necessarily true; a patent infringed by a JEDEC compliant product may not be

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essential to the standard, for example. Hence, Staff submits that, any finding that Netlist violated its RAND obligation “would require, *inter alia*, (i) a finding of infringement of patents that have been declared to be standard essential patents (“SEPs”) to JEDEC” (SIB at 161.)

In the absence of an infringement finding, as here, any RAND obligation on Netlist’s part is purely hypothetical, and cannot form a factual basis for foregoing or delaying an exclusion order on the basis of the public interest. Indeed, the Commission came to a similar conclusion in *Certain 3G Mobile Handsets and Components Thereof*. In that investigation, the Commission received numerous comments and briefs addressing the effect of SEPs and FRAND obligations in the public interest context. These briefs came from the parties to that investigation, Staff, and Commissioners of the Federal Trade Commission, among others. Ultimately, however, the Commission declined to reach the SEP issue based on the fact that it had found no infringement, stating:

Our findings of noninfringement render any consideration of public interest issues moot. We appreciate the extensive submissions provided on these issues. These submissions, available to the public, may be beneficial to those interested in these issues.

Certain 3G Mobile Handsets and Components Thereof, Inv. No. 336-TA-613 (Remand), Comm’n Op. at 50 n.27 (Sep. 21, 2015).

However, if the Commission finds infringement in this investigation, and then reaches the RAND issue as related to one or more of the statutory public interest factors, it would still be necessary to determine whether the asserted patents are essential to a JEDEC standard. In addressing this point, Respondents rely on contentions from Netlist representatives, as well as interrogatory responses, indicating that Netlist believed the asserted patent claims were essential to JEDEC standards. (RIB at 157 (citing RX-0018C.010; RX-0007C at Q/A 74-75; JX-0032C at 24:5-14; Whitley, Tr. at 313:2-4).) For example, Netlist’s expert, Dr. Fiona Scott Morton testified that:

based on my review of Netlist’s contention interrogatory responses in this Investigation, I understand that Netlist believes all six of the Asserted Patents are essential to JEDEC standards for DDR4 LRDIMM and that the ’837 patent is also

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essential to the JEDEC standards for DDR4 RDIMM. Netlist's corporate representative, Noel Whitley, also confirmed that at his deposition

(RX-0007C at Q/A 74.) Similarly, Netlist's representative, Mr. Noel Whitley testified during his deposition that, "[i]t's Netlist's position that each of the asserted claims is essential to, yeah, a JEDEC standard." (JX-0032C at 24:10-12.) And, in an interrogatory response, Netlist stated:

Netlist contends that each asserted claim is essential to a JEDEC standard and that, consistent with Section 8.2.4 of the JEDEC Manual of Organization and Procedure, JM21R (Revision of JM21Q, November 2011), dated July 2015 ("JEDEC Manual"), Netlist was obligated "to offer to license on RAND terms, to all Potential Licensees, [Netlist]'s Essential Patent Claims for the use, sale, offer for sale or other disposition of a portion of a product in order to be compliant with the required portions of a final approved JEDEC Standard issued during the period of membership in that committee."

(RX-0018C at 10.) Complainant does not appear to dispute the essentiality of its asserted patents. Accordingly, if the Commission determines that one or more of the asserted patents is infringed in this investigation, the undersigned finds that the evidence of record would support the conclusion that the infringed patents are essential to a JEDEC standard.

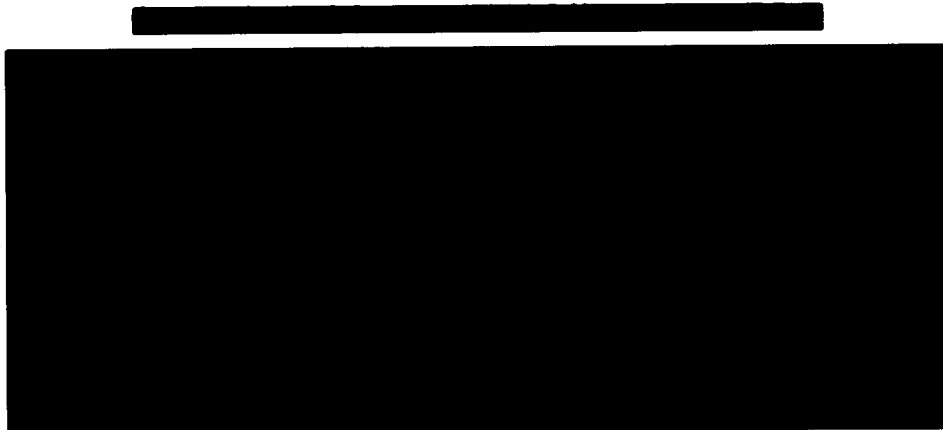
There is no dispute among the parties that, if Complainant's patents are essential to a JEDEC standard, then Complainant has an obligation to license those patents on RAND terms. (See RIB at 157 (citing JX-0032C at 26:6-11).) Rather the parties dispute whether Complainant has complied with its RAND obligation.

Respondents argue that Complainant has not complied with its RAND obligation. Respondents' base their argument on a [REDACTED] offer, among others, from Complainant that "asked SK hynix to pay [REDACTED] per LRDIMM and [REDACTED] per RDIMM on [REDACTED] [REDACTED] (RIB at 164 (citing RX-0411C).) Respondents argue that, under those terms, it "would have paid (on a present value basis) approximately [REDACTED] in royalties." (*Id.* (citing RX-0005C at Q/A 31).) Respondents further argue that "[t]he [REDACTED] LRDIMM royalty would equate to an effective rate

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of approximately [REDACTED], and approximately [REDACTED]
[REDACTED], as prices are projected to decline.” (*Id.* (citing RX-0005C at Q/A 34).)

Respondents compare the offer they received from Complainant to a Joint Development and Licensing Agreement (“JDLA”) between Complainant and Samsung. (*See Id.* at 165.) Respondents insist that “Netlist’s offers to SK hynix must be measured against what Samsung paid under the JDLA because that agreement is the *only* license that Netlist has entered covering the Asserted Patents and Samsung and SK hynix are similarly situated competitors in the sale of the accused LRDIMM and RDIMM products.” (*Id.* (citing RX-0005C at Q/A 179-180; RX-0007C at Q/A 199-209; RX-1585C at Q/A 82-105).) Following this line of reasoning, Respondents, through their expert, Mr. Lasinski, “unpack” the JDLA into constituent elements and assign a value gained by Netlist for each component of the agreement. (*See id.* at 166-169.) From those values, Respondents calculate per unit royalty rates for both the LRDIMMs and RDIMMs under the JDLA. (*Id.* at 170.) To show unfair discrimination, Respondents compare the royalty rates it calculated from unpacking the JDLA to the royalty rates in a [REDACTED] licensing offer from Netlist to SK Hynix. (*See id.*) That comparison is summarized in the following chart created by Respondents:



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(*Id.*) As shown in this chart, Respondents submit that the discrepancy between the terms offered to Samsung in the JDLA and the terms offered to SK hynix establish that Complainant's licensing offers are unfairly discriminatory. (*See Id.*)

Respondents also argue that Complainant's licensing offers have been unreasonable because the inventions claimed in the asserted patents are of minimal value, at least in part because of alternatives in the prior art. (*See Id.* at 172-74.) Respondents also appear to suggest that the asserted patents do not "cover the key enabling technologies in the LRDIMM and RDIMM standards." (*Id.* at 173-74.) Respondents also support their unreasonableness argument by pointing to internal Netlist documents that attempted to forecast [REDACTED]. (*Id.* at 174 (citing JX-0032C at 175:9-25; RX-0197C.060; RX-0005C at Q/A 258; RX-0007C at Q/A 210-11).) From that estimate, Respondents submit that Netlist's offers to SK hynix in [REDACTED] and [REDACTED] have [REDACTED]. (*Id.* at 174 (citing RX-0005C at Q/A 263-67).) Respondents additionally argue that because the amount of consideration Netlist would have received from SK hynix under the [REDACTED] offer was [REDACTED]. (*Id.* at 175 (citing RX-0005C at Q/A 258).) Further, Respondents argue that [REDACTED]. (*Id.* at 174-75 (citing RX-0005C at Q/A 264-267; RX-0499C; RX-0500C; RX-0502C; RX-0498C).) And, Respondents argue that Netlist's offers are unreasonable because they are not in line with the JDLA, or with [REDACTED].

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(*Id.* at 175 (citing RX-0002C at Q/A 163-212; RDX-0002).) Finally, Respondents criticize at length the hedonic regression analysis performed by Complainant's expert, Mr. Sidak, which Netlist offers as evidence that its offers to SK hynix are reasonable. (*Id.* at 175-182.)

By contrast, Complainant argues that Respondents have "refus[ed] to engage meaningfully with Netlist on a license to Netlist's standard essential patents," and are thus guilty of patent holdout. (CIB at 164.) Complainant submits that, "[a]n infringer of an SEP holds out when it uses SEPs without authorization under the guise that the patent owner's offers to license were not fair or reasonable." (*Id.* (citing *Certain Electronic Devices, Including Wireless Communication Devices, Portable Music & Data Processing Devices, & Tablet Computers* at 63, Inv. No. 337-TA-794, Doc. No. 512742 (USITC July 5, 2013) (Final)).) In support of this argument, Complainants submit that Respondents are not willing licensees because [REDACTED]

[REDACTED]. (*Id.* (citing Min, Tr. at 601:7-20, 602:14-604:6, 604:22-605:6; CX-0932C, at Q/A 428-430).) Complainant also points to Respondents' failure to make any revised licensing offer following Netlist's [REDACTED] offer, which Complainants characterize as [REDACTED] (*Id.* (citing CX-0315C at 75:3-8; CX-0006C, at Q/A 514, 642-644, 658-665; CX-0533C at 1).)

Complainant argues that "Respondents' bear the burden of proof on RAND-related defenses." (*Id.* at 165 (citing *Certain 3G Mobile Handsets Investigation and Components Thereof*, No. 337-TA-613, Initial Determination on Remand at 43 (April 27, 2015)).) Complainant asserts that a "departure from the principle that Respondents bear the burden of proving RAND-related defenses would disincentivize participation in SSOs and, for at least that reason, have significant, negative ramifications for the public health and welfare." (*Id.* (citing *Certain 3G Mobile Handsets and Components Thereof*, No. 337-TA-613, Reply of J. Gregory

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Sidak to the Written Submission of Chairwoman Edith Ramirez of the Federal Trade Commission on the Public Interest, at 6 (July 20, 2015)).) Here, Complainant submits that Respondents have not met their burden.

Complainant disputes that it has engaged in patent hold-up, or would engage in hold-up if an exclusion order enters, and argues that Respondents' "position on holdup consists of speculative policy arguments, divorced from the facts of this Investigation, many simply rehashing Dr. Scott Morton's 2016 Congressional testimony that the ITC abets patent holdup, without any effort to confront the scholarship and empirical evidence at odds with that position." (*Id.* at 166 (citing CX-0006C, at Q/A 370-412, 414; CX-0932C, at Q/A 59, 359-365).) With respect to Respondents' prospective hold-up accusations, Complainant quotes *Certain Electronic Devices, Including Wireless Communication Devices, Portable Music & Data Processing Devices, & Tablet Computers* at 63, Inv. No. 337-TA-794, Comm'n Op. at 113-114 fn. 23 (USITC July 5, 2013) (Final), which noted:

Absent empirical evidence of actual harm of consumers or innovation, what remains are policy arguments that the risk of hold-up occurring is sufficiently great to warrant denying an exclusion order to [the complainant] in this investigation. The Commission is not a policy making body and is not empowered to make that decision.

(*Id.*)

Complainant argues that Respondents have failed to meet their burden to establish that the JDLA is comparable to the type of one-way license contemplated under the JEDEC manual.

(*Id.*) Complainant submits that Respondents must show that the JDLA is sufficiently comparable, that licenses that bundle other rights along with patents rights require extra scrutiny, and that even if Respondents make a threshold showing of comparability, the ultimate weight given to the JDLA will still depend on its degree of comparability. (*Id.* at 167 (citing *LaserDynamics, Inc. v. Quanta Comput., Inc.*, 694 F.3d 51, 79 (Fed. Cir. 2012); *Lucent*

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Technologies, Inc. v. Gateway, Inc., 580 F.3d 1301, 1329 (Fed. Cir. 2009); *ResQNet.com v. Lansa, Inc.*, 594 F.3d 860, 871-872 (Fed. Cir. 2010).)

Separate from whether Respondents' have met their burden to establish that the JDLA is a comparable license, Complainant offers its own explanation of why the JDLA is not probative of a RAND rate. First, Complainant argues that the [REDACTED]

[REDACTED] (*Id.* at 168.) [REDACTED]
[REDACTED]

[REDACTED] (CIB at 168 (citing Whitley, Tr. at 350:23-351:23 and 356:8-357:1).)
In support of this argument, Complainant notes [REDACTED]

[REDACTED]
[REDACTED]
[REDACTED]

Complainant submits that its [REDACTED]
[REDACTED]

[REDACTED] (*Id.* at 169 (citing CX-0006C, at Q/A 521-527, 545-553).) In short, Complainant presents the JDLA as a wide-reaching agreement wherein [REDACTED]

[REDACTED]. (*See Id.*) Additionally, even assuming the JDLA was a comparable license, Complainant argues that the agreement would only represent [REDACTED] because [REDACTED]

[REDACTED]
[REDACTED] (*Id.* at 170 (citing CX-0006C, at Q/A 576, 578).)

Complainant also criticizes Respondents' reliance on their expert's attempt to "unpack" the JDLA into constituent elements. (*See Id.*) First, Complainant argues that the analysis

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improperly relied on accounting, as opposed to economic principles. (*See Id.* at 171.)

Complainant identifies several errors that stem from applying accounting principles to the JDLA, including improperly [REDACTED]

[REDACTED] (*See Id.* (citing RX-0005C, at Q/A 40).) Complainant also criticizes Respondents' unpacking analysis for failing to assign value to [REDACTED]

[REDACTED] that Complainant could obtain under the JDLA, (*see Id.*), and failing to assign value to Complainant from [REDACTED]

[REDACTED] (*see Id.* at 172-73.)

Complainant faults Mr. Lasinski's unpacking analysis for suggesting that [REDACTED]

[REDACTED] (*Id.* at 173.)

Complainant also discounts Mr. Lasinski's analysis of the JDLA as improperly retrospective. (*See Id.*) Complainant argues that [REDACTED]

[REDACTED]

[REDACTED] (*Id.*) Complainant goes on to levy several other critiques of Mr. Lasinski's analysis, all of which share a common theme: that Mr. Lasinski ignored, or undervalued, benefits received by Complainant under the JDLA. (*See Id.* at 173-175.)

As an alternative to Mr. Lasinski's analysis of the JDLA as a means for determining a RAND rate, Complainant advocates a "top-down" approach, "which extrapolates the incremental value of the patented technology from the profits made by the infringing article." (*Id.* at 176 (citing *Certain 3G Mobile Handsets Investigation and Components Thereof*, No. 337-TA-613, Initial Determination on Remand at 73-74 (April 27, 2015)).) Under this approach, which includes the hedonic regression analysis of its expert, Mr. Sidak, Complaint concludes that a proper RAND range for the asserted patents could be as high as [REDACTED] and as low as [REDACTED] per

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LRDIMM module, and as high as [REDACTED] and as low as [REDACTED] per DDR4 RDIMM. (*See Id.* at 179 (citing CX-0006C, at Q/A 473, 477, 484, 492).) Based on these estimates, Complainant argues that its [REDACTED] licensing offer to SK hynix is actually well within the RAND range for the asserted patents. (*Id.*) As an additional point, Complainant notes that its [REDACTED] offer calls for a royalty rate that is roughly [REDACTED] what Mr. Lasinski derived from the JDLA, and that at least one court found a RAND range that covered a similar scope from the upper to lower bound. (*See Id.* at 180 (citing *Microsoft Corp. v. Motorola, Inc.*, 864 F. Supp. 2d 1023, *8 (W.D. Wash. June 6, 2012)⁴⁰.)

Finally, Complainant argues that Respondents' understanding of "nondiscriminatory" has no basis in law, and is overly restrictive. (*See Id.* at 180-82.) Complainant likens Respondents' understanding of "nondiscriminatory" terms to that of a "most-favored nation clause," meaning that a licensor would be required to offer the same effective rate to all licensees, regardless of whether market assumptions that led to one offer were no longer accurate at the time of a later offer. (*See Id.* at 182.)

Staff "submits that the evidence shows that Complainant has discharged [its RAND] duty and that there is therefore no patent hold-up by Complainant that would support denying the requested remedial orders." (SIB at 162.) Staff elaborates that "the evidence shows that the JDLA is not a proper benchmark for determining terms and conditions for a license with a RAND rate" because [REDACTED] and the JDLA "includes additional [REDACTED]

[REDACTED]

(*Id.* at 162-63.) Like Complainant, Staff discredits Mr. Lasinski's "unpacking" analysis because

⁴⁰ This citation appears to be in error. The *Microsoft* opinion includes no "*8" pagination, and the opinion does not appear to reference "upper" or "lower" bounds.

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“it fails to assign a monetary value to each component of the JDLA and, moreover, ignores the overall value of the JDLA to Complainant, who initially searched for and subsequently found a strategic partner in Samsung.” (*Id.* at 163 (citing RX-0005C at Q/A 188-241; CX-0932C at Q/A 89-101, 109-113, 122-151).)

“Staff further submits that the evidence shows that Complainant have engaged in a series of negotiations with Respondents that clearly have not resulted in any agreement (including any license to the Asserted Patents), but that apparently have been in good faith.” (*Id.* (citing CX-0006C at Q/A 415-502; RX-0005C at Q/A 116-141).) Thus, Staff concludes that “[s]uch good-faith negotiations support finding that Complainant has discharged its duty, assuming that one arises with a finding that its Asserted Patents are SEPs.” (*Id.* (citing *Certain Electronic Devices, Including Wireless Communication Devices, Portable Music and Data Processing Devices, and Tablet Computers*, Inv. No. 337-TA-793, Comm’n Op., p. 44-45 (July 5, 2013)).)

As an initial matter, the undersigned notes that the burden to prove an affirmative defense based on a breach of Complainant’s RAND obligations lies with Respondents. This follows from prior Commission determinations, as well as the Commission’s Rules. *See Certain Electronic Devices, Including Wireless Communication Devices, Portable Music & Data Processing Devices, & Tablet Computers* at 63, Inv. No. 337-TA-794, Comm’n Op. at 63-64 (USITC July 5, 2013) (finding respondent “has not met its burden to prove that [the complainant’s] FRAND undertakings prevent the Commission from finding a violation of section 337”); 19 C.F.R. § 210.37(a) (“The proponent of any factual proposition shall be required to sustain the burden of proof with respect thereto.”). To the extent Respondents attempt to shift that burden based on the phrase “demonstrably free of any unfair discrimination,” the undersigned is not persuaded. That phrase appears in only one place in the JEDEC Manual, at

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section A.3 to the Annex, which is the form for making the potentially essential patent disclosure and RAND licensing assurance introduced in section 8.2.3 and 8.2.5 of the manual. (*See* CX-0325 at 45.) However, section 8.2.5, by its own terms, only refers to “terms and conditions that are free of any unfair discrimination.” (*See Id.* at 34-35.) Respondents do not acknowledge this discrepancy, and in fact, their expert relies only on the language in the Annex to support her conclusion that “the JEDEC policy appropriately places the responsibility on the SEP owner to demonstrate that its terms are non-discriminatory.” (RX-0007C at Q/A 114.) Respondents’ expert fails to even acknowledge that the JEDEC Manual provides inconsistent terms in discussing unfair discrimination in the RAND context.

Notwithstanding the internal inconsistency of the JEDEC manual on whether RAND terms must be “demonstrably” free of any unfair discrimination, the undersigned is not persuaded that the JEDEC Manual, which does not even purport to address which party bears the burden of proof in a RAND dispute, can serve as a basis to set aside the Commission’s practice of placing the burden of proof on the party advancing a RAND defense. To find otherwise would effectively add a new element of proof to section 337 investigations for RAND encumbered patents, *i.e.*, complainants seeking to establish a violation based on their RAND encumbered patents would necessarily have to show that they made licensing offers that were free from unfair discrimination. Such a requirement is untethered from the statutory language of section 337. *See* 19 U.S.C. § 1337. Of course, in the face of a *prima facie* showing of unfair discrimination by a respondent, a complainant would need to rebut that showing, but Respondents have failed to articulate a legal basis to place the initial evidentiary burden on Complainant for what is essentially their own affirmative defense.

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Second, the undersigned notes that the JEDEC Manual indicates that “[t]he Patent Policy will be interpreted and governed under the laws of the State of New York.” Except for a passing reference by Complainant, the parties make no attempt to analyze Complainant’s RAND obligations according to the New York state law. (See CIB at 162 (citing *W.W.W. Associates, Inc. v. Giancontieri*, 77 N.Y.2d 157, 162 (1990)).) Rather, the parties have relied on the testimony of their economic experts to lay out what is essentially a legal framework for interpreting the JEDEC Manual. (See, e.g., *Id.* at 163 (citing CX-0006C at Q/A 686); RIB at 165 (citing RX-0007C at 114-117).) That approach is largely unhelpful, as both experts’ opinions appear to be based primarily on policy concerns as opposed to controlling principles of law.

Respondents’ failure to address the JEDEC Manual RAND obligation in the context of New York law is particularly troubling here because, under New York law, “[a] court cannot enforce a contract unless it is able to determine what in fact the parties have agreed to,” *Carione v. Hickey*, 133 A.D.3d 811, 811 (N.Y. App. Div. 2015), and “[i]f an agreement is not reasonably certain in its material terms, there can be no legally enforceable contract.” *Id.* Based on an extensive review of the parties’ briefing, there seems to be, among other issues, a fundamental disagreement about what is required by the “reasonable” and “unfair discrimination” terms of the JEDEC patent policy. This is unsurprising given that section 8.2.1 of the JEDEC Manual, which provides “Terms and definitions” for the JEDEC Patent Policy, does not even attempt to define what is meant by “reasonable” or “non-discriminatory” licensing terms and conditions. (See CX-0325 at 30-31.) To the contrary, section 8.2.8 of the JEDEC Manual actually states that:

JEDEC makes no representation as to the reasonableness of any terms or conditions of the license agreements offered by such patent rights holders, and all negotiations regarding such terms and conditions must take place between the individual parties outside the context of JEDEC.

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(*Id.* at 36.) Thus, it appears that the JEDEC Patent Policy is, by design, ambiguous about the meaning of reasonable license terms and conditions. As such, the obligation to license on RAND terms, which appears to be a material term of the JEDEC Patent Policy, is anything but “reasonably certain.” *See Carione*, 133 A.D.3d at 811 (holding that reasonably certain material terms are a prerequisite to an enforceable contract). The parties have cited no legal authority for the proposition that the undersigned is empowered to inject clarity into the RAND obligation when there is none in the JEDEC manual. Rather, given that the undersigned cannot determine what exactly the RAND commitment entails in terms of acceptable licensing terms, New York law appears to require that the agreement be considered unenforceable. *See id.*

Nonetheless, the undersigned notes that none of the parties, including Complainant, assert that the JEDEC agreement is unenforceable. Accordingly, assuming that the JEDEC agreement is enforceable, and Complainant owes a RAND obligation, the undersigned finds that Respondents’ have not established a violation of that agreement by Complainant. As noted by Staff, the root of Respondents’ defense is that Complainant must offer them the same “effective rate” its expert derived from the JDLA between Samsung and Complainant. (*See* SIB at 162.) The JDLA, however, is not the same type of agreement that is required under the JEDEC Patent Policy. (*See generally* RX-0187C.) While the JDLA does include terms directed to a license to Samsung for Complainant’s asserted patents, (*see id.* at 8), it also includes a number of other terms that are directed to establishing a strategic partnership between Samsung and Complainant, (*see id.* at 4, 6). Respondents are overly-dismissive of these terms, and their expert, Mr. Lasinski, was only able to determine his low effective rate by concluding that those terms had no value to Complainant. (*See* RX-0005C at 46 (summarizing Mr. Lasinski’s valuation of each component to the JDLA).) Those conclusions are at odds with the testimony of record.

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The undersigned is not persuaded by Respondents' argument that the joint development aspect of the JDLA is a sham, meant only to cloak a license agreement between Complainant and Samsung. [REDACTED]

[REDACTED]

[REDACTED]

at the time the JDLA was executed, Complainant apparently believed it was receiving valuable consideration from having Samsung sign on as a strategic partner. (See CX-0001C at Q/A 139-141; CX-0007C at Q/A 35, 38, 43.) Whatever the RAND obligation means, it surely cannot mean that Complainant is required to offer a license to every JEDEC implementer on the same terms as the JDLA with Samsung, but without even the prospect of obtaining the strategic partnership benefits contemplated by the JDLA. Accordingly, the undersigned finds that Respondents have not made out a showing of unfair discrimination based on the JDLA.

In sum, Respondents have failed to tie their RAND arguments to a recognizable affirmative defense, a scenario that the Commission has previously noted with disapproval. See *Certain Electronic Devices, Including Wireless Communication Devices, Portable Music & Data Processing Devices, & Tablet Computers* at 63, Inv. No. 337-TA-794, Comm'n Op. at 63-64 (USITC July 5, 2013). Assuming the RAND arguments are breach of contract arguments, the undersigned finds that the underlying contract—the JEDEC Manual—lacks sufficient clarity to enforce its terms against Complainant, which the Commission has also noted as a reason a RAND argument may fail. (*Id.* (noting failure to identify basic elements of a contract claim, such as definite terms).) And finally, even assuming that the RAND agreement is related to a cognizable affirmative defense, and that the terms of the JEDEC Manual are sufficiently definite

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to be enforceable, the undersigned finds that Respondents have failed to establish unfair discrimination based on the evidence of record.

Accordingly, the undersigned finds that the evidence does not support foregoing or delaying any exclusion order on the basis of a RAND obligation by Complainant.⁴¹

XIII. INITIAL DETERMINATION

Based on the foregoing, it is the Initial Determination of the undersigned that Respondents do not infringe any asserted claim of U.S. Patents No. 8,001,434; 8,359,501; 8,689,064; 8,489,837; or 8,516,185. The undersigned further determines that asserted claims are not invalid and that the domestic industry requirement has been satisfied for the '434, '501, '064, and '185 patents, but has not been satisfied for the '837 patent.

The undersigned hereby CERTIFIES to the Commission this Initial Determination and the Recommended Determination. The parties' briefs, which include the final exhibits lists, are not certified as they are already in the Commission's possession in accordance with Commission rules. *See* 19 C.F.R. § 210.38(a).

The Secretary shall serve the confidential version of this Initial Determination upon counsel who are signatories to the Protective Order (Order No. 1) issued in this Investigation. A public version will be served at a later date upon all parties of record.

Within seven days of the date of this document, each party shall submit to the office of the Administrative Law Judge a statement as to whether or not it seeks to have any portion of

⁴¹ Respondents also include a section in their initial brief asserting equitable estoppel, waiver, and implied license. (*See* RIB at 185-87.) These arguments, which are treated summarily in less than three pages of briefing, appear to be afterthoughts. Regardless, each presupposes a finding that Complainant breached a RAND obligation. Because the undersigned has determined that the evidence does not show that Complainant breached a RAND obligation, each of these affirmative defenses also fails.

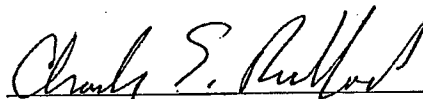
~~_____~~

this document deleted from the public version. The parties' submissions must be made by hard copy by the aforementioned date.

Pursuant to 19 C.F.R. § 210.42(h), this Initial Determination shall become the determination of the Commission unless a party files a petition for review pursuant to 19 C.F.R. §210.43(a) or the Commission, pursuant to 19 C.F.R. § 210.44, orders on its own motion a review of the Initial Determination or certain issues therein.

Within ten days of the date of this document, the parties shall submit to the Office of Administrative Law Judges a joint statement regarding whether or not they seek to have any portion of this document deleted from the public version. The parties' submission shall be made by hard copy and must include a copy of this Initial Determination with red brackets indicating any portion asserted to contain confidential business information to be deleted from the public version.⁴² The parties' submission shall include an index identifying the pages of this document where proposed redactions are located. The parties' submission concerning the public version of this document need not be filed with the Commission Secretary.

SO ORDERED.


Charles E. Bullock
Chief Administrative Law Judge

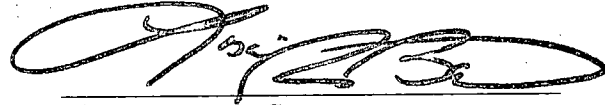
⁴² If the parties submit excessive redactions, they may be required to provide an additional written statement, supported by declarations from individuals with personal knowledge, justifying each proposed redaction and specifically explaining why the information sought to be redacted meets the definition for confidential business information set forth in Commission Rule 201.6(a). 19 C.F.R. § 201.6(a).

**CERTAIN MEMORY MODULES AND
COMPONENTS THEREOF, AND PRODUCTS
CONTAINING SAME**

Inv. No. 337-TA-1023

PUBLIC CERTIFICATE OF SERVICE

I, Lisa R. Barton, hereby certify that the attached **Initial Determination on Violation of Section 337 and Recommended Determination on Remedy and Bond** has been served by hand upon the Commission Investigative Attorney, Vu Bui, Esq., and the following parties as indicated, on **December 4, 2017**.



Lisa R. Barton, Secretary
U.S. International Trade Commission
500 E Street, SW, Room 112
Washington, DC 20436

On Behalf of Netlist Inc.:

James M. Wodarski, Esq.
**MINTZ, LEVIN, COHN, FERRIS, GLOVSKY
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One Financial Center
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- Via Hand Delivery
- Via Express Delivery
- Via First Class Mail
- Other: _____

On Behalf of Respondents SK hynix Inc., SK hynix America Inc., and SK hynix memory solutions Inc.

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- Via Hand Delivery
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