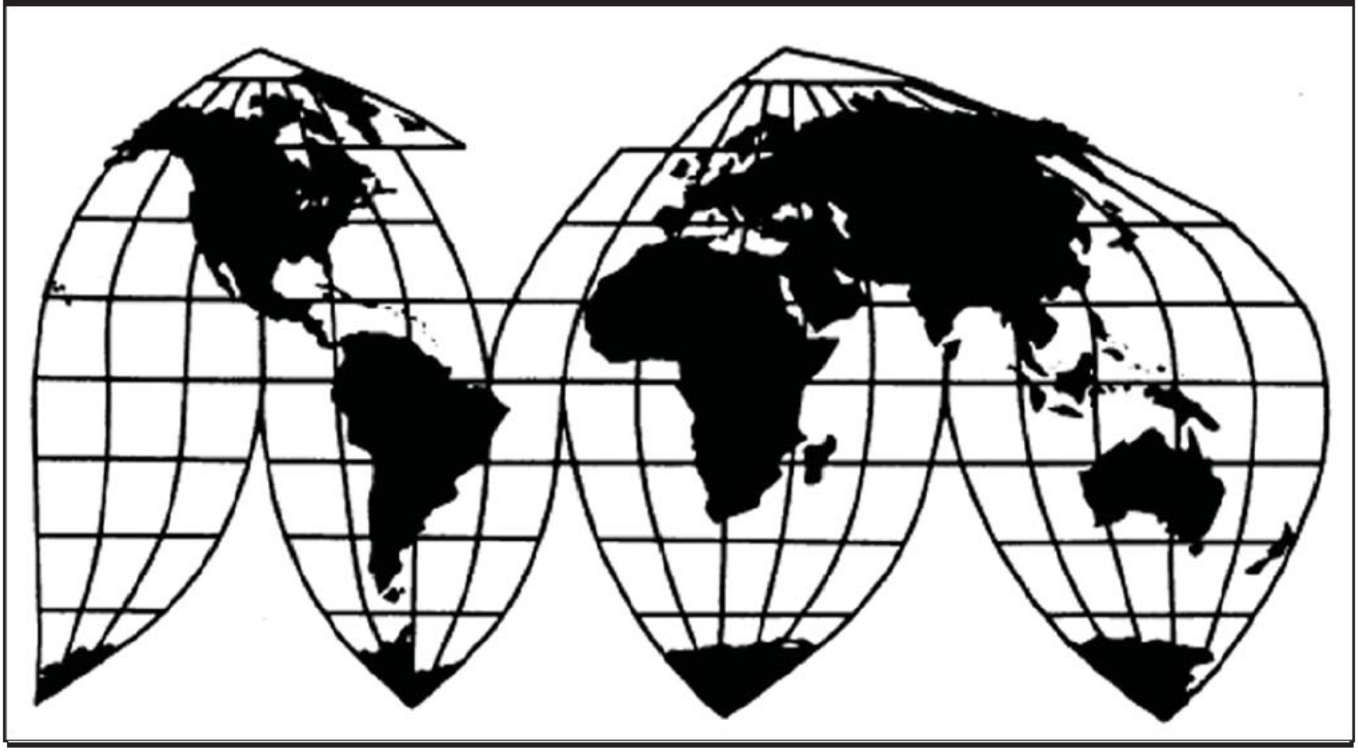
In the Matter of

Certain Semiconductor Chips and Products Containing Same

Investigation Nos. 337-TA-753

Publication 4386 **March 2013**

U.S. International Trade Commission



Washington, DC 20436

U.S. International Trade Commission

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U.S. International Trade Commission

Washington, DC 20436
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In the Matter of

Certain Semiconductor Chips and Products Containing Same

Investigation Nos. 337-TA-753

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UNITED STATES INTERNATIONAL TRADE COMMISSION
Washington, D.C.

In the Matter of **CERTAIN SEMICONDUCTOR CHIPS AND PRODUCTS CONTAINING SAME**	**Investigation No. 337-TA-753**

NOTICE OF COMMISSION DETERMINATION TERMINATING THE INVESTIGATION WITH A FINDING OF NO VIOLATION OF SECTION 337

AGENCY: U.S. International Trade Commission.

ACTION: Notice.

SUMMARY: Notice is hereby given that the U.S. International Trade Commission has determined to terminate the above-captioned investigation with a finding of no violation of section 337 of the Tariff Act of 1930, 19 U.S.C. § 1337.

FOR FURTHER INFORMATION CONTACT: Sidney A. Rosenzweig, Office of the General Counsel, U.S. International Trade Commission, 500 E Street, S.W., Washington, D.C. 20436, telephone (202) 708-2532. Copies of non-confidential documents filed in connection with this investigation are or will be available for inspection during official business hours (8:45 a.m. to 5:15 p.m.) in the Office of the Secretary, U.S. International Trade Commission, 500 E Street, S.W., Washington, D.C. 20436, telephone (202) 205-2000. General information concerning the Commission may also be obtained by accessing its Internet server at *http://www.usitc.gov*. The public record for this investigation may be viewed on the Commission's electronic docket (EDIS) at *http://edis.usitc.gov*. Hearing-impaired persons are advised that information on this matter can be obtained by contacting the Commission's TDD terminal on (202) 205-1810.

SUPPLEMENTARY INFORMATION: The Commission instituted this investigation on January 4, 2011, based on a complaint filed by Rambus Inc. of Sunnyvale, California ("Rambus"), alleging a violation of section 337 in the importation, sale for importation, and sale within the United States after importation of certain semiconductor chips and products containing the same. 76 *Fed. Reg.* 384 (Jan. 4, 2011). The complaint alleged the infringement of various claims of patents including U.S. Patent Nos. 6,470,405; 6,591,353; 7,287,109 (collectively, "the Barth patents"); and Nos. 7,602,857; and 7,715,494 (collectively, "the Dally patents"). The Barth patents share a common specification, as do the Dally patents. The notice of investigation named as respondents Freescale Semiconductor of Austin, Texas ("Freescale"); Broadcom Corp. of

Irvine, California ("Broadcom"); LSI Corporation of Milpitas, California ("LSI"); Mediatek Inc. of Hsin-Chu, Taiwan ("Mediatek"); NVIDIA Corp. of Santa Clara, California ("NVIDIA"); STMicroelectronics N.V. of Geneva, Switzerland; and STMicroelectronics Inc. of Carrollton, Texas (collectively, "STMicro"), as well as approximately twenty customers of one or more of these respondents.

The investigation has since been terminated against many of the respondents on the basis of Rambus's settlements with Broadcom, Freescale, MediaTek, and NVIDIA.

LSI and STMicro are the only two manufacturer respondents remaining. With them as respondents are their customers Asustek Computer, Inc. and Asus Computer International, Inc.; Cisco Systems, Inc.; Garmin International Inc.; Hewlett-Packard Company; Hitachi Global Storage Technologies; and Seagate Technology.

On March 2, 2012, the ALJ issued the final ID. The ID found no violation of section 337 for several reasons. All of the asserted claims were found to be invalid or obvious in view of the prior art under 35 U.S.C. § 102 or 103. The Barth patents were found to be unenforceable under the doctrine of unclean hands by virtue of Rambus's destruction of documents. The ID also found that Rambus had exhausted its rights under the Barth patents as to certain products of one respondent. The ID found that all of the asserted patent claims were infringed, and rejected numerous affirmative defenses raised by the respondents.

On March 19, 2012, Rambus, the respondents and the Commission investigative attorney ("IA") each filed a petition for review of the ID. On March 27, 2012, these parties each filed a response to the others' petitions.

On May 3, 2012, the Commission determined to review the ID in its entirety. 77 *Fed. Reg.* 27,249 (May 9, 2012). The notice of review asked the parties to brief certain questions.

Having examined the record of this investigation, including the ALJ's final ID, the petitions for review and the responses thereto, and the briefing in response to the notice of review, the Commission has determined to terminate the investigation with a finding of no violation of section 337.

The Commission has determined to find no violation of section 337 for the following reasons: We affirm the ALJ's conclusion that all of the asserted patent claims are invalid under 35 U.S.C. § 102 or 103, except for the asserted Dally multiple-transmitter claims ('857 claims 11-13, 32-34, 50-52), for which we find that Rambus has not demonstrated infringement. We reverse the ALJ's determination that Rambus has demonstrated the existence of a domestic industry under 19 U.S.C. § 1337(a) for both the Barth patents and Dally patents. We affirm the ALJ's determination that the Barth patents are unenforceable under the doctrine of unclean hands. We affirm the ALJ's finding of exhaustion of the Barth patents as to one respondent. The Commission's determinations, including non-dispositive findings not recited above, will be set forth more fully in the Commission's opinion.

The authority for the Commission's determination is contained in section 337 of the Tariff Act of 1930, as amended (19 U.S.C. § 1337), and in sections 210.21, 210.42-46 and 210.50 of the Commission's Rules of Practice and Procedure (19 C.F.R. §§ 210.21, 210.42-46 and 210.50).

By order of the Commission.

Lisa R. Barton
Acting Secretary to the Commission

Issued: July 25, 2012

CERTAIN SEMICONDUCTOR CHIPS AND PRODUCTS CONTAINING SAME **Inv. No. 337-TA-753**

PUBLIC CERTIFICATE OF SERVICE

I, Lisa R. Barton, hereby certify that the attached **NOTICE** has been served by hand upon, the Commission Investigative Attorney, Daniel L. Girdwood, Esq., and the following parties as indicated on **July 25, 2012.**

Lisa R. Barton, Acting Secretary
U.S. International Trade Commission
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PUBLIC VERSION

UNITED STATES INTERNATIONAL TRADE COMMISSION
Washington, D.C.

In the Matter of **CERTAIN SEMICONDUCTOR CHIPS AND PRODUCTS CONTAINING SAME**	**Investigation No. 337-TA-753**

COMMISSION OPINION

TABLE OF CONTENTS

I. INTRODUCTION

The Commission instituted this investigation on January 4, 2011, based on a complaint filed by Rambus Inc. of Sunnyvale, California ("Rambus"), alleging a violation of section 337 in the importation, sale for importation, and sale within the United States after importation of certain semiconductor chips and products containing the same. 76 *Fed. Reg.* 384 (Jan. 4, 2011). The complaint alleged the infringement of various claims of U.S. Patent Nos. 6,470,405; 6,591,353; 7,287,109 (collectively, "the Barth patents"); and Nos. 7,602,857; 7,602,858; and 7,715,494 (collectively, "the Dally patents"). The Barth patents share a common specification, as do the Dally patents. The notice of investigation named as respondents Freescale Semiconductor of Austin, Texas ("Freescale"); Broadcom Corp. of Irvine, California ("Broadcom"); LSI Corporation of Milpitas, California ("LSI"); Mediatek Inc. of Hsin-Chu, Taiwan ("Mediatek"); NVIDIA Corp. of Santa Clara, California ("NVIDIA"); STMicroelectronics N.V. of Geneva, Switzerland; and STMicroelectronics Inc. of Carrollton, Texas (collectively, "STMicro"), as well as approximately twenty customers of all these respondents. The asserted claims vary on a respondent-by-respondent basis.

This investigation is related to an earlier Commission investigation, *Certain Chips Having Synchronous Dynamic Random Access Memory Controllers and Products Containing Same*, Inv. No. 337-TA-661 ("*Synchronous DRAM Memory Controllers*"). Rambus is the complainant in both, and previously asserted the Barth patents in the *Synchronous DRAM Memory Controllers* investigation. In that investigation, the Commission found a violation of section 337 as to the Barth patents, and issued exclusion orders against NVIDIA and its customer-respondents. Several appeals of the Commission determination were taken, and the Court of Appeals for the Federal Circuit heard argument in

October 2011. Following the argument, Rambus and NVIDIA settled their dispute and the court of appeals dismissed the appeals prior to issuing an opinion.

In this investigation, Rambus asserted the Dally patents against NVIDIA, and against most of the other respondents, the Barth patents and the Dally patents together. The investigation has since been terminated against many respondents on the basis of Rambus's settlements with Broadcom, Freescale, Mediatek, and NVIDIA. LSI and STMicro remain as respondents, along with their customers Asustek Computer, Inc. and Asus Computer International, Inc.; Cisco Systems, Inc. ("Cisco"); Garmin International Inc. ("Garmin"); Hewlett-Packard Company; Hitachi Global Storage Technologies; and Seagate Technology.

On March 2, 2012, the ALJ issued the final Initial Determination ("ID"). It found no violation of section 337 because all of the asserted claims (of both patent families) were anticipated by, or obvious in view of, numerous pieces of prior art or combinations of prior art. In addition, the ID found the Barth patents unenforceable under the doctrine of unclean hands because of Rambus's spoliation of documents in the late 1990s. The ALJ found some of Rambus's patent rights exhausted as to respondent Garmin. Rambus filed a petition for review, and the respondents and the Commission investigative attorney ("IA") contingent petitions for review. The parties opposed each other's petitions. On May 3, 2012, the Commission determined to review the ID in its entirety. 77 *Fed. Reg.* 27,249 (May 9, 2012). The Commission's notice requested that the parties provide further briefing on specific issues. *See id.*

II. BACKGROUND

A. The Barth Patents

The asserted Barth patents disclose improvements to the signaling between a controller and a dynamic-random-access-memory device ("DRAM"). In particular, the patents disclose an improved signal protocol (*i.e.*, the signal traffic between the controller and the DRAM) that results in more efficient DRAM operation. Rambus has asserted claims 11-13, 15, and 18 of the '405 patent; claims 11-13 of the '353 patent; and claims 1, 2, 4, 5, 12, 13, 20, 21, and 24 of the '109 patent.

The accused products are memory controllers designed to interface with memory devices that comply with the DDR, DDR2, DDR3, LPDDR or LPDDR2 standards. *See* ID at 7. All of the accused Barth products are alleged to infringe a subset of claims, while the Accused Auto Precharge Products are alleged to infringe additional claims:

Asserted Barth Claims	Accused Products
'353 patent claims 11-13 '109 patent claims 1, 2, 4, 12, 20, 21, 24	All Accused Barth Products
'405 patent claims 11-13, 15, 18 '109 patent claims 5, 13	The Accused Auto Precharge Products (a subset of the Accused Barth Products)

See ID at 47-48.

B. The Dally Patents

The asserted Dally patents disclose improvements to the signaling between two components – a transmitter and a receiver – in a digital system. In particular, as will be discussed more fully below, data is converted from parallel transmission at one speed to serial transmission at a higher speed. With the use of certain equalization, the data can be

transmitted in such serial form faster and with fewer errors than had the transmission been made in parallel. Rambus has asserted the following claims against the following accused products:

Asserted Dally Claims	Accused Products
'857 patent claims 1, 4-6, 9, 10, 24-28, 35, 36, 39-44, 47, 53 '494 patent claims 1, 2, 6, 8, 25, 30, 39, 42	All Accused Dally Products
'857 patent claims 11-13, 32-34, 50-52 '494 patent claims 26, 40	Accused Dally Products with multiple transmitters
'857 patent claims 2, 31, 49 '494 patent claim 3	Accused Dally Products able to output data at 2 Gb/s or greater

ID at 68.

The two Dally patents asserted in this investigation are part of a family of patents whose parent application was filed on June 23, 1997. William Dally is the sole inventor. He was on the faculty of the Massachusetts Institute of Technology ("MIT") at the time, and MIT is the assignee of the Dally patents. Rambus acquired an exclusive license to the Dally patents in 2003, and in 2010, acquired all substantial rights in the Dally patents. ID at 327. As will be discussed, *infra*, the respondents contend in their petition for review that prior to Rambus's acquisition of rights, MIT and the University of North Carolina ("UNC") entered into an agreement that vested UNC with ownership of the Dally patents, and that the ALJ improperly found that Rambus has standing to assert the Dally patents. *Id.*

C. The Final ID

In the ID, the ALJ found that all of the asserted patent claims are directly and indirectly infringed by the respondents. He also found, however, that all of the asserted

claims are invalid under 35 U.S.C. §§ 102 or 103, and that the Barth patents are unenforceable because Rambus purposefully destroyed documents that could have helped the respondents' defense.

The ALJ made the following determinations under 35 U.S.C. §§ 102 and 103 for the Barth patents:

The ALJ's Barth §§ 102 and 103 Findings

Anticipation / obviousness	**Primary reference**	**Secondary reference**	**Patent claims**
Anticipated	Japanese patent publication no. 3-276344 (Yano)		'353 patent claim 11
Anticipated	European patent application no. 94304672.2 (Dan)		'353 patent claim 11
Anticipated	NeXTBus specification ("NeXTBus)		'353 patent claims 11-13 '109 patent claims 1, 20, 24
Anticipated	U.S. Patent No. 5,313,624 (Harriman)		'353 patent claims 11-13 '109 patent claims 1, 20, 24
Anticipated	U.S. Patent No. 5,218,684 (Hayes)		'353 patent claim 11
Obvious	Yano or Dan	Farmwald	All asserted claims
Obvious	Farmwald	Yano or Dan	All asserted claims
Obvious	Yano or Dan	Scalable Coherent Interface paper ("SCI") and JEDEC Standard 21-C Release 4 ("Release 4")	All asserted claims
Obvious	NeXTBus	Farmwald or Release 4	All asserted claims of the '405 and '109 patents
Obvious	Harriman	Farmwald or Release 4	All asserted claims of the '405 and '109 patents
Obvious	Farmwald	NeXTBus or Harriman	All asserted claims of the '405 and '109 patents

For the Dally patents, the ALJ made the following determinations under sections 102 and 103:

The ALJ's Dally §§ 102 and 103 Findings

Anticipation / obviousness	**Primary reference**	**Secondary reference**	**Patent claims**
Anticipated	Widmer Article		'857 patent claims 1, 4-6, 9-10, 24-28, 35-36, 39-44, 47, 53 '494 patent claim 1, 2, 6, 8
Anticipated	LSI SL500		'857 patent claims 1-2, 4-6, 9-10, 24-28, 31, 35, 36, 39-44,47, 49, 53 '494 patent claims 1-3, 6, 8, 25-26, 30, 39, 40, 42
Obvious	Widmer Article	Ewen Article or the knowledge of a person of ordinary skill	Asserted Dally differential signal claims '494 patent claims 25, 26, 30, 39, 40, 42
Obvious	Widmer Article	Ewen Article	Asserted Dally 1GHz claims '857 patent claims 2, 31, 49 '494 patent claim 3, 30, 42
Obvious	Widmer Article	Knowledge of a person of ordinary skill	Asserted Dally multiple transmitter claims with a common processor '857 patent claims 11-13, 32-34, 50-52
Obvious	LSI SL500 art	Knowledge of a person of ordinary skill	Asserted Dally multiple transmitter claims with a common processor '857 patent claims 11-13, 32-34, 50-52

D. The Petitions for Review and Commission Briefing

Rambus petitioned for review of all of the ALJ's invalidity determinations under sections 102 and 103 and the finding of unclean hands.[1] The respondents' contingent petition challenged the ALJ's findings of no anticipation of the Barth patent claims by Farmwald or SyncLink.[2] The respondents also argued that the ALJ improperly found that the respondents waived certain prior-art arguments relating to the Dally patents. The respondents' petition also raises other arguments that the ALJ rejected including lack of written description, noninfringement, inequitable conduct, domestic industry, and standing. The IA filed a contingent petition for review on unclean hands and standing.[3] Each party filed a response to the others' petitions.[4] On May 3, 2012, the Commission determined to review the ID in its entirety. 77 *Fed. Reg.* 27,249 (May 9, 2012). The Commission's notice requested that the parties provide further briefing on specific issues:

1. Claim Construction (Dally patents)
   a. Why "output frequency" requires a construction setting forth a specific data rate per cycle, as opposed to the plain language of the claims, which requires only a particular output frequency, *i.e.*, a number of cycles per second.

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[1] Complainant Rambus Inc.'s Petition for Review (Mar. 19, 2012) ("Rambus Pet.").

[2] Respondents' Contingent Petition for Review of the Initial Determination (Mar. 19, 2012) ("Resp'ts Pet.").

[3] Contingent Petition of the Office of Unfair Import Investigations for Review of the Initial Determination on Violation of Section 337 (Mar. 19, 2012) ("IA Pet.").

[4] Response of Complainant Rambus to Petitions for Review of Respondents and the Staff (Mar. 27, 2012) ("Rambus Reply Pet."); Respondents' Reply to Petition of Complainant Rambus Inc. and Contingent Petition of the Office of Unfair Import Investigations (Mar. 27, 2012) ("Resp'ts Reply Pet."); Combined Response of the Office of Unfair Import Investigations to the Private Parties' Petitions for Review of the Initial Determination on Violation of Section 337 (Mar. 27, 2012) ("IA Reply Pet.").

b. If "output frequency" is construed not to require a particular data rate, the effect of that construction, if any, on the section 102 and 103 determinations on review, as set forth below.

2. Validity
   a. The motivation to combine and secondary indicia of nonobviousness, for each section 103 combination upon which one or more parties petitioned for review. (Barth patents and Dally patents)
   b. The pertinence, if any, of synchronous versus asynchronous prior art, and the motivation to apply the teachings of asynchronous art to synchronous systems. (Barth patents)
   c. Whether the Harriman patent evidences the publication of the NeXTBus. specification, in view of the fact that NeXT is the assignee of the Harriman patent. (Barth patents)
   d. Whether the respondents have demonstrated the publication date of the SyncLink specification (RX-4270C). (Barth patents)

3. Infringement
   a. The disablement of the Cisco products with a disabled transmitter (Dally patents), *see* Resp. Pet. 48, as compared to the disablement of the SL500 prior art products, *see* Rambus Pet. 17-20.
   b. Given that "in every infringement analysis, *the language of the claims*, as well as the nature of the accused products, dictates whether an infringement has occurred," *Fantasy Sports Properties, Inc. v. Sportsline.com, Inc.*, 287 F.3d 1108, 1118 (Fed. Cir. 2002) (emphasis added), whether a finding of infringement or noninfringement of the asserted Dally claims should be guided by the claim language at issue in *Fantasy Sports*, *Silicon Graphics, Inc. v. ATI Technologies., Inc.*, 607 F.3d 784, 794 (Fed. Cir. 2010), *ACCO Brands, Inc. v. ABA Locks Manufacturer Co.*, 501 F.3d 1307, 1310 (Fed. Cir. 2007), or other Federal Circuit caselaw regarding active or enabled components.
   c. The infringement of asserted Dally '494 method claims 39, 40, and 42 in view of the ALJ's discussion at page 77 of the ID regarding enabled features of apparatuses.
   d. Certain STMicroelectronics products are claimed to have substantial noninfringing uses by virtue of their compatibility with SDR memory. *See* Resps. Pet. 25; ID at 67 n.9. Explain with specificity and citations to the evidentiary record what these STMicroelectronics products are and your contention that these products have or lack substantial noninfringing uses.

4. Unclean Hands (Barth patents)
   a. Whether the doctrines of preclusion or *stare decisis* prevent Rambus from challenging the determinations from the 661 investigation as to the date upon which it was obligated to retain documents, or its bad faith.
   b. Explain with specificity the factual distinctions between the records of the 661 investigation and this investigation, with respect to prejudice suffered

or allegedly suffered by the respondents by reason of Rambus's destruction of documents.

5. Inequitable Conduct (Barth patents)

In connection with Commission review, the parties are asked to brief the following issues relating to nondisclosure of the SyncLink specification (RX-4270C), and only that specification (*i.e.*, not other SyncLink publications and not RamLink):

a. Whether the respondents have proven materiality of this particular document.
b. Whether the PTO's reexamination of the '109 patent demonstrates that the broadest reasonable construction of the '109 patent's "signal" is a construction broader than the '405 and '353 patents' "strobe signal."
c. If the broadest reasonable construction of "signal" in the '109 patent is "a signal," and not "a strobe signal," whether the SyncLink specification is cumulative with art presented to the PTO.
d. If inequitable conduct were to be found for the '109 patent, whether the '405 and '353 patents are also unenforceable.

6. Domestic Industry

a. Whether, given the particular scope of the licensed field of each Rambus license, Rambus should nonetheless be required to allocate licensing expenses on a patent-by-patent basis.

7. Patent Exhaustion (Barth patents)

a. Whether the licensed Samsung memory products substantially embody the Barth patents.
b. What evidence, if any, demonstrates that the Samsung memory purchased (by the respondent discussed on the bottom half of page 337 of the ID, *see* Rambus Pet. 95-97), was ever located in the United States prior to incorporation into products overseas, and whether the respondent took possession of the memory in the United States.

8. Standing (Dally patents)

a. Whether Rambus is a *bona fide* purchaser pursuant to 35 U.S.C. § 261.
b. Whether UNC's claim of ownership is barred by laches.

Id. at 27,250.

The notice set page limits of 100 pages for each opening brief and 60 pages for each reply on these issues. In addition to these opening and reply briefs,[5] Rambus and the respondents filed separate briefs on remedy, the public interest, and bonding.

III. ANALYSIS

A. Claim Construction

Rambus and the respondents each petitioned for review of certain claim constructions for the Dally patents. Rambus also challenges certain constructions for the Barth patents.

1. The Dally Patents

Rambus raised one issue of claim construction, and the respondents two. Rambus's disputed construction is meant to avoid certain prior art, and the respondents' two constructions are meant to ensnare certain prior art or to avoid infringement. We begin with Rambus's arguments.

a. "Output frequency"

The ALJ construed "output frequency" to mean "output data rate."[6] ID at 34. Rambus contests this construction, which is material only for claims 2, 31, and 49 of the '857

[5] Complainant Rambus Inc.'s Resp. to the Commission's Notice to Review in the Entirety a Final Initial Determination Finding No Violation of Section 337 (May 21, 2012) ("Rambus Br."); Resp'ts' Resp. to the Commission's Notice of Review (May 18, 2012) ("Resp'ts Br."); Resp. of the Office of Unfair Import Investigations to the Notice of Commission Determination to Review in the Entirety a Final Determination Finding No Violation of Section 337 (May 18, 2012) ("IA Br."); Complainant Rambus Inc.'s Reply to the Resps. of Resp'ts and the Staff to the Commission's Notice to Review in the Entirety a Final Initial Determination Finding No Violation of Section 337 (June 1, 2012) ("Rambus Reply Br."); Resp'ts' Combined Reply to Rambus' and the Staff's Resps. to the Commission's Notice of Review (June 1, 2012) ("Resp'ts Reply Br."); Reply Submission of the Office of Unfair Import Investigations to the Notice of Commission Determination to Review in the Entirety a Final Determination Finding No Violation of Section 337 (June 1, 2012) ("IA Reply Br.").

[6] In our notice of review, we asked the parties to provide further briefing on why the term "output frequency" requires "a construction setting forth a specific data rate per cycle,

(Footnote continued on the next page)

patent and claim 3 of the '494 patent. Those claims require a minimum output frequency of 1 GHz. The Commission has determined to affirm the ALJ's construction.

b. "Processor"

All of the asserted Dally claims include a "processor." The ALJ "discern[ed] no reason to further construe the claims because the dispute between the parties is a factual dispute." ID at 24. For purposes of invalidity, the respondents contended below that a certain device called a "Manchester encoder" falls within the scope of the ordinary meaning of a "processor." Resp'ts Pet. 58-59. This issue matters only in that one prior art reference, U.S. Patent No. 5,541,957 (Lau), uses such Manchester encoders. The ALJ did not reach the issue because he found that the respondents waived reliance on the Lau patent because they failed to include adequate argument in support of Lau in the post-hearing brief, pursuant to the ALJ's ground rules. ID at 224-25. On petition, the respondents contend that this is an issue of claim construction. Resp'ts Pet. 58-59. As we will discuss, *infra*, we affirm the ALJ's determination that the respondents' arguments relying on Lau have been waived. Accordingly, the respondents' argument is moot.

c. "Transmitter circuit" / "Transmitter"

The ID afforded the terms "transmitter circuit" and "transmitter" their ordinary meaning, and, in so finding, that the terms do not disclaim "conventional FIR filters." ID at 34-43. The respondents petitioned for review, asserting that the Dally patent specification

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as opposed to the plain language of the claims, which requires only a particular output frequency, *i.e.*, a number of cycles per second." 77 *Fed. Reg.* at 27250. In response to this question, all parties agree that a person of ordinary skill in the art would interpret the term "output frequency" to correspond to a particular data rate. IA Br. 3-4; Rambus Br. 1-4; Resp'ts Br. 2-9.

and file history constitute a disclaimer of scope. Resp'ts Pet. 42. We disagree with the respondents' interpretation of the specification and find that the disputed terms have not been expressly redefined or their scope clearly disclaimed for the reasons set forth by the ALJ.

The respondents also rely on the prosecution history of a related Dally patent (U.S. Patent No. 7,602,858) (the "Dally '858 patent") as a basis for disclaimer. That patent is a sibling of the two asserted Dally patents because all three patents claim priority directly to a parent application filed on July 10, 2006. The application for the '858 patent included a claim that read in part: "the transmitter being operable to vary strength of the output bit signals so that the strength of each output bit signal is determined by a number of output bit signals since the last preceding transition between output bit signals having different values." RX-2240 at 96. The applicant, in traversing the examiner's patent rejection explained that the prior art was not invalidating because the prior art used a weighting of bit values (like an FIR filter) instead of counting the number of bits. *Id.* at 103-104. More specifically, the applicant explained: "By contrast, with the present invention, the strength of each output bit signal can be simply determined by the number of output bit signals since the last preceding transition." *Id.* at 104. The respondents contend that the use of the language "present invention" is a disclaimer as to CIR filters in any Dally patent claim.

The ALJ rejected the respondents' argument for two reasons. First, citing *Omega Engineering v. Raytek Corp.*, 334 F.3d 1314, 1323 (Fed. Cir. 2003), he found that any disclaimer was not sufficiently unmistakable to change the ordinary meaning of the claim language. ID at 41. We agree with the ALJ and find that this reason is dispositive. The claim language at issue in the '863 patent carves from its scope FIR filters, and the

explanation by prosecution counsel, while using the word "invention," was not clear that the FIR filters were excluded from all Dally claims as opposed to Dally claims with language like that of the '863 claim at issue.

The ALJ's second basis for rejecting the respondents' argument was that "not only is [the] language [of the related patent] different, but these statements were made during the prosecution of a related application that is not a parent or earlier application of the patents-in-suit." ID at 41-42. We do not rely on the fact that the disclaimer was made in a child rather than a parent application, *see Verizon Servs. Corp. v. Vonage Holdings Corp.*, 503 F.3d 1295, 1307 (Fed. Cir. 2007). However, we note that the ALJ's cited cases, which stand for the proposition that when a first patent uses different language from a related second patent, disclaimers will not ordinarily flow from one to the other, *see Ventana Med. Sys., Inc. v. Biologix Labs., Inc.*, 473 F.3d 1173, 1182 (Fed. Cir. 2006); *Invitrogen Corp. v. Clontech Labs., Inc.*, 429 F.3d 1052, 1078 (Fed. Cir. 2005), supports the ALJ's first basis, and our sole basis, for declining to carve out FIR filters from the construction of transmitter.

Finally, we observe that LSI and STMicro are the only two manufacturers left in this investigation and their experts conceded that "transmitter" should include the conventional CIR filter. *See* Tr. 1578-79 (LSI's expert Dr. Hajimiri); JX-147C at Tr. 90 (STMicro's expert Dr. Walker); CX-9542C Q/A 133 (Rambus's expert Dr. Singer discussing Walker's testimony); *see also* IA Reply Pet. 57-60. We conclude that the doctrines of estoppel, waiver, and invited error prohibit LSI and STMicro "from asserting as 'error' a position that [they] had advocated at the trial." *Key Pharms. v. Hercon Labs. Corp.*,161 F.3d 709, 715 &

n.1 (Fed. Cir. 1998); *see also Union Carbide Chems. & Plastics Tech. Corp. v. Shell Oil Co.*, 308 F.3d 1167, 1181-82 (Fed. Cir. 2002).

2. The Barth Patents

Rambus has disputed two claim constructions, in each instance arguing that the ALJ's construction was too broad. Rambus Pet. 32-33 ("memory device"); *id.* at 45 ("write command"). The ALJ construed the term "memory device" as "a device in which information can be stored and retrieved electronically," ID at 108, and "write command" as "an instruction to store data," ID at 93-95. Having reviewed the parties' petitions and submissions, we affirm the ALJ's constructions for the reasons set forth in the ID.

B. Anticipation and Obviousness

The ID analyzed numerous prior art references and combinations of prior art references applied to both patent families. Rambus has petitioned for review of each invalidity determination. On review, the Commission affirms the ALJ's conclusion that all of the asserted patent claims are invalid under 35 U.S.C. §§ 102 or 103.[7]

1. The Dally Patents

The ALJ found that certain asserted patent claims were anticipated by the Widmer Article (RX-4109) and, independently, by a prior-art LSI "SerialLink SL500" system, and that the rest were obvious in view of one of those references combined with other art. *See supra* p. 7.

[7] The Commission also affirms the ALJ's determination that the Barth patents are not invalid for lack of written description support under 35 U.S.C. § 112. ID at 232-37; Resp'ts Pet. 15-23.

a) The Widmer Article

The principal reference that invalidates the Dally patents – anticipating some of the asserted claims, and rendering others obvious – is an article by various scientists from two IBM research laboratories entitled "Single-Chip 4x500MBaud CMOS Transceiver" ("Widmer Article") (RX-4109).

(i) Anticipation

We affirm the ALJ's determination that the Widmer Article was published as part of a bound digest of papers to attendees and is prior art. ID at 129. We further affirm the ALJ's determinations that although the Widmer Article is prior art, the accompanying slides are not (RX-4109.0007 through .0009). ID at 130.

We affirm the ALJ's determination that the Widmer Article is enabled. ID at 131-37. In addition to the reasons set forth in the ID, we find that the respondents' expert testimony (Dr. Hassoun) is persuasive. Tr. 1491-92; Hassoun Witness Statement Q&A 134. In contrast, Rambus's expert Andrew Singer's testimony to the contrary, Tr. 2301-2317, lacks credibility, and at points refuses to acknowledge what the Widmer Article teaches on its face, *id.* at 2302. We also affirm the ALJ's findings that the Widmer Article anticipates Dally '857 claims 1, 4-6, 9-10, 24-28, 35-36, 39-44, 47, 53 and Dally '494 claims 1, 2, 6 and 8, and adopt the ALJ's reasoning in support thereof. ID at 156-60. We agree with the ALJ that Dr. Hassoun's witness statement (RX-5431C), which provided element-by-element support for the respondents' invalidity contentions, is thorough, credible, and persuasive.[8]

[8] *See, e.g.*, RX-5431C Q&A QQ. 126-130; Q&A 131-135 (anticipation of '857 claim 1); Q&A 137 ('857 claim 4); Q&A 138 ('857 claim 5); Q&A 169 ('857 claim 6); Q&A 139 ('857 claim 9); Q&A 140 ('857 claim 10); Q&A 141 ('857 claim 24); Q&A 142 ('857 claim 25); Q&A 143 ('857 claim 26); Q&A 144 ('857 claim 27); Q&A 171 ('857 claim 28); Q&A

(Footnote continued on the next page)

(ii) Obviousness

The ALJ found that the claims that were not anticipated by the Widmer Article were obvious under 35 U.S.C. § 103. In some instances, the ALJ relied on the Ewen Article, and in other instances relied upon the knowledge of a person of ordinary skill, as secondary to the Widmer Article.

(A) Claims with an "Output Frequency" of at Least 1 GHz ('857 claims 2, 31, and 49 and '494 claim 3)

Certain asserted dependent patent claims require minimum output frequencies. Claims 30 and 42 of the '494 patent, for example, require output frequencies of at least 400 MHz. As the ALJ found, there is no genuine dispute that the Widmer Article teaches such frequencies, *see* RX-4019 at 1 ("Each link carries 400Mb/s, corresponding to 500MBaud after 8B/10B encoding."); ID at 154, for which reason we have affirmed the ALJ's determination that those claims are anticipated by the Widmer Article. Other asserted claims require that the transmitter have an "output frequency of at least 1 GHz and a bandwidth greater than 100 MHz." '857 claims 2, 31, 49; '494 claim 3. As quoted above, each serial link in Widmer falls somewhat short of those speeds. The ALJ also found, and the respondents took the position, that the Widmer Article taught using several serial links at the same time, and that those parallel transmissions should be added together. Q&A 155-57. We affirm the ALJ's finding of no anticipation as to these 1 GHz claims. ID at 151-52.

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145 ('857 claim 35); Q&A 146 ('857 claim 36); Q&A 147 ('857 claim 39); Q&A 148 ('857 claim 40); Q&A 149 ('857 claim 41); Q&A 150 ('857 claim 42); Q&A 151 ('857 claim 43); Q&A 172 ('857 claim 44); Q&A 152 ('857 claim 47); Q&A 153 ('857 claim 53); Q&A 186 ('494 claim 1); Q&A 188 ('494 claim 2); Q&A 189 ('494 claim 6); Q&A 192-93 ('494 claim 8).

The ALJ found that the 1 GHz / 100 MHz patent claims were obvious in view of the combination of the Widmer Article and an article entitled "Single Chip 1062Mbaud CMOS Transceiver for Serial Data Communication") ("Ewen Article"). RX-4125; *see* ID at 153. That article was authored by six of the authors of the Widmer Article (including Dr. Widmer), with Dr. John Ewen as its lead author. The Ewen Article is one of two references cited in the Widmer Article. RX-4109 at 2; ID at 147 & n.16. The Ewen Article was directed to a system compliant with the "emerging ANSI fibre channel standard at 1062.5Mbaud." RX-4125 at 1. We agree with the ALJ that a person of ordinary skill would be motivated to combine the Widmer Article and the Ewen Article because the two systems addressed the same need – single-chip high-speed transceivers – but did so with complementary solutions. ID at 153.

In further support, we find that there is was a reasonable expectation of success in combing Widmer and Ewen. Rambus has argued that the two articles could not be combined because if the teachings could be combined, the IBM team consisting of Drs. Widmer and Ewen would have done so. Rambus Pet. 14-15. Rambus's argument suffers from the fallacious assumption that the paramount goal of the IBM team – or for any person of skill – was for each and every transceiver build to be as fast as possible, incorporating all of their inventions into a single transceiver, regardless of the needs at the time. To the contrary, as Dr. Hassoun testified, the Widmer Article's speed of 500 megabaud was "for the chip they were designing for the purposes they were designing it for." Tr. 1501; *see also id.* at 1491-93, 1500-01; *see also* Hassoun Q/A 158-160, 164, 428-32. The Ewen Article sought compliance with an emerging ANSI standard requiring 1052.5Mbaud, and the Widmer Article did not.

(B) "Differential Signaling" Limitations ('494 claims 25, 39 and 42)

The ALJ also found that '494 claims 25, 39 and 42 were obvious in view of the combination of the Widmer Article and the Ewen Article. We agree with the ALJ's conclusion and his analysis in support thereof. ID at 147-150.

(C) Claims with Multiple Transmitters ('857 claims 11-13, 32-34, 50-52)

The ALJ found that the multiple transmitter claims of the '857 patent were not anticipated by, but obvious in view of, the Widmer Article combined with the knowledge of a person of ordinary skill in the art.[9] ID at 155-56. Upon review, the Commission reverses the ALJ's finding of obviousness.

As discussed on page 155 of the ID, certain asserted patent claims require "at least one additional transmitter circuit within the chip" that is also "coupled to the processor" of claim 1. '857 claim 11. The Widmer Article teaches the use of multiple transmitters. RX-4109 at 2 (Fig. 1). However, the claims require that the transmitters be "coupled to the processor." In contrast, Widmer teaches that each transmitter has its own processor, namely the serializer in Fig. 1 of the Widmer Article (shown in more detail in the Widmer Article's Figure 2). The ALJ held that choosing a configuration with a common processor would have been obvious. ID at 155-56.

On review, we agree with the ALJ that the claim language calls for the transmitters to be connected to the same processor, what the ALJ called a "common processor," *id.* at 155,

[9] The multiple transmitter claims in dispute are Dally '863 patent claims 11-13, 32-34, and 50-52. Claims 26 and 40 of the Dally '494 patent call for multiple transmitters but those transmitters need not be connected to a common processor; those claims are therefore anticipated and infringed for the reasons set forth by the ALJ. ID at 81 (infringement); *id.* at 159, 200 (anticipation).

and affirm the ALJ's determination that the multiple-transmitter claims are not anticipated by the Widmer Article. There is no common processor in the Widmer article, and the respondents never explained why the processor should be considered one, and not several, processors. *See* ID at 155; IA Reply Pet. 71-72.

The ALJ's finding of obviousness was based on his citation to Dr. Hassoun's testimony:

> Q. Does the Widmer article disclose multiple line drivers coupled to a common serializer?
>
> A. Well, in – again, in light of the infringement contentions where we treated – well, where Dr. Singer treated four 8B/10Bs each in one channel as a single processor, then to that extent, there is a single processor. Basically all four of the 8B/10B encoders here, you can treat them as a single processor.
>
> And it is not that out of the realm of understanding because you could have, say, a processor that has four cores in it, for example. This would be something equivalent to that.
>
> Q. Do you see the parallel N label on the far left-hand side [of figure 1 of the Widmer Article]?
>
> A. I do.
>
> Q. What is the parallel N coupled to?
>
> A. That's coming from off chip.
>
> Q. Could it be connected to a processor?
>
> A. Absolutely.

Tr. 1542:9-1543:5. We conclude that this demonstration falls short of demonstrating obviousness by clear and convincing evidence. We also note that the reference to Dr. Singer's testimony is inapposite for obviousness. Dr. Singer testified to his belief that there could be multiple processors for the asserted Dally claims: "And I don't believe that I have opined specifically on this question, but my reading of this right now when it says at least

one additional transmitter circuit within the chip, that that brings by reference the processor that was associated with that at least one additional transmitter." Tr. 802:10-16; *accord* Tr. 803:13-15 ("So I can't be certain that what you just said is correct, that it is a one and only one [processor]."). Tr. 803:13-15. Thus, the Singer testimony does not support an argument that various components be considered a single processor, but rather, that the claims were anticipated under a construction rejected by the ALJ, *i.e.*, a construction in which a common processor is not required.[10]

b) LSI SerialLink 500

The ALJ also found certain Dally patent claims anticipated by a system offered for sale by LSI called "SerialLink SL500."[11] *See supra* p. 7. The parties dispute whether the SL500 art included pre-emphasis of high-frequency signals, or whether that pre-emphasis was disabled. In our notice of review, we asked the parties for further briefing on the disablement of the SL500 prior art products compared to an accused product that Rambus contended infringed notwithstanding the fact that it was allegedly disabled. For the same reasons set forth above in connection with the Widmer Article, we reverse the ALJ's finding

[10] We note that the ALJ's requirement of a common processor is not outcome determinative. The respondents petitioned for review on this issue and explained that the Widmer "processor" was the collection of serializers. Resp'ts Pet. 60-62. If no common processor had been required, we find that the Widmer Article anticipates the multiple transmitter claims, because there is no genuine dispute that the Widmer Article discloses multiple transmitters. RX-4109 Fig. 1.

[11] The SL500 art consisted of three components pertinent to this investigation: (1) CWSL500 cores; (2) SL500 chips; and (3) BDSL500 evaluation boards. *See, e.g.*, ID at 173; Tr. 1607; OUII Pet. Reply 79. The "core" was a design for portions of a semiconductor chip, put differently, blueprints or instructions for making a chip. Tr. 1607; *see also* Tr. 1582, 1588-90, RX5506C Q&A 10; Tr. 756-61. The SL500 chip was one (but not the only) chip that incorporated the CWSL500 core. Tr. 1607. LSI produced a BDSL evaluation board that incorporated the SL500 chip. *See, e.g.,* Tr. 1608. Thus, the board includes the chip, and the chip includes the core. *See generally* RX-5430C Q&A 373-75.

of obviousness as to the asserted multiple transmitter claims based on LSI SerialLink 500. *See* ID at 193-94. Although the ALJ observes that Rambus "has not contested this limitation," ID at 194, the burden remained on the respondents to demonstrate obviousness, and they have not done so clearly and convincingly for the multiple-transmitter claims.[12] We otherwise affirm the ALJ's remaining determinations of anticipation and obviousness, including his determination that the LSI SerialLink 500 is prior art.

c) Secondary Considerations

"Secondary considerations," also referred to as "objective evidence of non-obviousness," such as "commercial success, long-felt but unsolved need, failure of others, etc.," may be used to understand the origin of the subject matter at issue and may be relevant as indicia of non-obviousness. *Graham v. John Deere Co.*, 383 U.S. 1, 17-18 (1966). Other "secondary considerations" may include copying by others, prior art teaching away, and professional acclaim. *See, e.g., Perkins-Elmer Corp. v. Computervision Corp.*, 732 F.2d 888, 894 (Fed. Cir. 1984); *Kloster Speedsteel AB v. Crucible Inc.*, 793 F.2d 1565 (Fed. Cir. 1986) (wide acceptance and recognition of the invention). Secondary considerations must be considered in evaluating the obviousness of a claimed invention, but the existence of such evidence does not control the obviousness determination as the court must consider all of the evidence under the *Graham* factors before reaching a decision on obviousness. *Richardson-Vicks Inc. v. Upjohn Co.*, 122 F.3d 1476, 1483-84 (Fed. Cir. 1997).

[12] We note that the ALJ's requirement of a "common processor" is not outcome determinative, because absent such a requirement, we find that the SerialLink products anticipate these claims based on the fact that they were designed to be scalable and could include multiple transmitters. ID at 193-94.

The Commission's notice asked that the parties brief secondary considerations generally, and was not limited to the Barth patents. 77 *Fed. Reg.* at 27250.

Rambus contends that the objective evidence of non-obviousness weighs against a finding of obviousness here. There is some such evidence. *See* Rambus Br. 21-27. In particular, after Dally presented the technology at a conference in 1996, it was praised by some industry members, and was published in an IEEE journal. *Id.* at 26-27. Some licenses to the Dally patents have been taken. *Id.* at 21-23.

The ALJ discounted the evidence presented by Rambus. He found that much of it was presented by Dr. Poulton, who assisted Dr. Dally in developing the technology. *Id.* at 227. He also discounted the licensing by virtue of licensees' interests in avoiding litigation with Rambus. *Id.* at 229. We affirm the ALJ's conclusions.

We also find that had the ALJ credited Dr. Poulton's testimony, that testimony would not have been as strong as Rambus contends. A nexus is required between the merits of the claimed invention and the evidence of secondary considerations. *See, e.g.*, *Western Union Co. v. MoneyGram Payment Sys., Inc.*, 626 F.3d 1361, 1372-73 (Fed. Cir. 2010). Dr. Poulton testified that it was the cheap "transition filter" used in the preferred embodiment that was the point of interest for the industry. Tr. 1768-70. Rambus, however, sought a construction of "transmitter" that included "conventional FIR filters," a construction that the ALJ adopted. In making its arguments, Rambus explained that the limitations of this filter are not found in the claim language of the asserted Dally patents, but instead in the related Dally '858 patent. In making our determinations of obviousness of the asserted Dally claims (in view of Widmer or the LSI SerialLink 500 system) we have considered Rambus's

showing of secondary considerations, and those considerations do not prevent our findings that the asserted patent claims are obvious.

2. The Barth Patents

a) Anticipation

The ALJ found that one or more asserted Barth patent claims were anticipated by each of the following five pieces of prior art: Japanese patent publication no. 3-276344 (Yano); European patent application no. 94,304,672.2 (Dan); NextBus Specification; U.S. Patent No. 5,313,624 (Harriman); and U.S. Patent No. 5,218,684 (Hayes). *See supra* p. 6. In addition, the ALJ rejected the respondents' arguments that any claims were anticipated by U.S. Patent No., 6,584,037 or the SyncLink IEEE Standard. We affirm the ALJ's determination of non-anticipation by Farmwald. We affirm the ALJ's findings of anticipation as to Yano, Dan, the NextBus Specification, Harriman, and Hayes. We reverse the ALJ's finding of anticipation based on the SyncLink IEEE Standard, because we find that it has not been demonstrated to be prior art.

(i) Whether NextBus and SyncLink Are Prior Art

(A) The NextBus Specification

We affirm the ALJ's determination that the NextBus Specification is prior art, ID at 105, and provide additional reasoning in support of that in the ID. The ALJ relied in part upon the fact that the specification was cited in the Harriman patent (U.S. Patent No. 5,313,624), which on its face was assigned to Next Computer, Inc. of Redwood City, California. The Harriman patent reads in pertinent part: "In the preferred embodiment of the present invention, bus 209 is a bus known as the 'NextBus' and is described in NextBus Specification, published by NeXT Computer, Inc., Redwood City, Calif." Harriman patent

col. 15 lines 43-46. We sought further briefing from the parties on this issue: "Whether the Harriman patent evidences the publication of the NextBus specification, in view of the fact that NeXT is the assignee of the Harriman patent." 77 *Fed. Reg.* at 27250. The respondents argue that Harriman demonstrates the publication of the NextBus specification because "if NeXT had actually desired to keep the NextBus Specification confidential as Rambus suggests . . . , NeXT would not have publicly disclosed so many aspects of the NextBus Specification in Harriman and notified persons of ordinary skill in the art that it 'publishe[s]' the NextBus Specification." Resp'ts Br. 59. We agree with the respondents and affirm the ALJ's determination for the reasons stated in the ID and the supplemental discussion above.

(B) The Draft SyncLink Standard

The ALJ did not make a determination whether the draft version of a SyncLink standard (RX-4270C) was prior art. The ID found that even if the draft standard were prior art, it was not anticipatory for purposes of invalidity, ID at 122-23, and was cumulative with other prior art of record for purposes of inequitable conduct, *id.* at 246-47. The Commission notice of review asked for further briefing of whether the respondents demonstrated that the SyncLink standard is prior art. 77 *Fed. Reg.* at 27250.

The Commission has determined that the respondents have failed to put forward clear and convincing evidence that the draft SyncLink standard was publicly accessible in the relevant timeframe. The respondents argue that the draft SyncLink standard "itself evidences its public availability." Resp. Br. 60. The respondents' theory, however, is inconsistent with guiding Federal Circuit caselaw. *See In re Lister*, 583 F.3d 1307, 1312-14 (Fed. Cir. 2009). Moreover, the theory is inconsistent with the document itself. By its terms it is "an unapproved draft" with limitations on distribution and copying. RX-4270C.0001. Other

pages evidence its draft status including the page that notes that the IEEE Standards Board liaisons are "How R. You" and "Eye M. Fine." RX-4260C.006.

The respondents offered no evidence that the draft standards were published. The respondents presented only limited evidence regarding accessibility, other than the document itself. The Respondents argue that at "least as early as September 1993, Rambus had detailed knowledge of SyncLink." Resp. Br. 61 (citing a SyncLink document, ostensibly from 1993, in Rambus's possession, and Rambus emails discussing SyncLink generally). That Rambus had working knowledge of the SyncLink standard-setting process does not evidence that the SyncLink draft standard was publicly accessible. Nor does the fact that Rambus possessed a 1993 document demonstrate that a later document was publicly accessible. Similarly, the fact that a trade publication discussed the SyncLink standard-setting process, Resp. Br. 62 (citing RX-2048C and RX2050C), fails to demonstrate that RX-4270C was publicly available. The respondents offered evidence that Hyundai discussed SyncLink in a May 1996 JEDEC meeting that Rambus also attended. Resp. Br. 61. Hyundai's knowledge of SyncLink generally also does not demonstrate that RX-4270C was publicly available, much less publicly available in the relevant timeframe to serve as prior art.

The respondents' best evidence of public accessibility is a May 1995 email by Rambus employee Richard Crisp, which states: "They offered to put anyone on the SynchLink [*sic*] proposal that wants to be on the list." Resp. Br. 62 (citing RX-2050C.0005). In addition, the respondents cite deposition testimony by Mr. Crisp in 2011 from a Rambus district court action. *Id.* In that testimony, Mr. Crisp recalled, in connection with being asked about SyncLink documents other than RX-4270C, that SyncLink documents may have been accessible from an FTP server. JX-030, at deposition pages 83-85, 97. Crisp did not

remember having seen RX-4270C (which also marked as trial exhibit RX-3451). JX-30 at deposition page 100.

We find that the respondents' evidence falls short of demonstrating the public accessibility of the draft SyncLink document. There is no evidence in the record about how the FTP server worked and whether a member of the public would have known about how to find documents posted there. In other contexts, the Federal Circuit has explained that prior art in a library must be cataloged in a way that enables people to find it based on subject matter. *See, e.g.*, *In re Klopfenstein*, 380 F.3d 1345, 1348-52 (Fed. Cir. 2004). No counterpart showing has been made here. By the respondents' reasoning, any and all SyncLink-related documents would be publicly accessible, and there is simply no reason to believe that to be true. Accordingly, we conclude that there is insufficient evidence to demonstrate that RX-4270C is prior art.

(ii) The Farmwald Patent

We affirm the ALJ's finding that an earlier Rambus patent, U.S. Patent No. 5,584,037 (Farmwald), does not anticipate the asserted claims of the Barth '109 patent. ID at 121-22. In addition to the reasons set forth by the ALJ, we further find that the respondents have waived the opportunity to construe the '109 patent's "signal" in a manner sufficiently broad to anticipate the '109 patent claims. In our earlier *Synchronous DRAM Memory Controllers* investigation, the respondents treated the '109 patent's "signals" as the same as the '353 and '405 patents' "strobe signals." Inv. No. 337-TA-661, Order No. 15 at 12 (June 22, 2009). The parties in this investigation agreed to be bound by those constructions, and the respondents continue to assert that they are not challenging the claim constructions from *Synchronous DRAM Memory Controllers*. Resp'ts Pet 18 n.6; *see* RX-5429C Q&A 220-21

(respondents' construction of "signal" as identical to "strobe signal"). Accordingly, the fact that the PTO in reexamination construed the "signal" of the '109 patent claims more broadly than "strobe signal," *Rambus, Inc. v. NVIDIA Corp.*, No. 2011-5255, slip op. at 9-10 (B.P.A.I. Sept. 1, 2011), is immaterial to this investigation. Farmwald does not teach a strobe signal, and the respondents' argument fails.

(iii) NextBus and The Harriman Patent

We have already affirmed the ALJ's determination that the NextBus Specification is prior art. The ALJ found claims 11-13 of the '353 patent, and claims 1, 20, and 24 of the '109 patent, anticipated by the NextBus Specification. ID at 106-17. We affirm the ALJ's determination that these claims are anticipated by the The NextBus Specification.[13] The NextBus Specification and the Harriman patent (U.S. Patent No. 5,313,624) are closely related, and we also affirm the ALJ's determination of anticipation based on Harriman. ID at 104. However, because of similarities between NextBus and Harriman, the ALJ focused on NextBus. On petition for review, Rambus has contended that the ID's discussion of Harriman was insufficient. Rambus Pet. 40. The following findings supplement the ALJ's discussion of Harriman, and bolster his conclusion that 11-13 of the '353 patent, and claims 1, 20, and 24 of the '109 patent are anticipated by Harriman. We find the respondents' testimony on anticipation persuasive. *See* RX-5429C Q&A 327.

Rambus argues that Harriman "does not disclose the external clock signal and its functionality, recited in '353 patent claims 12 and 13. . . . Harriman's Figure 8 labels 'MCLK' as '(internal),' while MCLKSEL* is described as a signal that selects BusClk 401

[13] We note that Rambus's principal argument is that NextBus does not "disclose issuing a strobe signal to a memory device," based on its construction of "memory device." Rambus Pet. 32-38, 40, but we have already rejected Rambus's claim construction argument.

and not a clock signal." Rambus Pet. 40. The ALJ rejected these same arguments in connection with the NextBus Specification. ID at 116-17. Harriman itself discloses the clocks as follows: "BusClk signal **801** is a 25 megahertz system clock. An MCLKSEL* signal **802** selects every other low phase of BusClk **1401**. MCLKSEL* is the logical OR of BusClk and MCLKSEL*. [*stet*: In Figure 8, it is clearly the MCLK* signal that is the logical OR of the other two signals.] MCLK* signal **803** provides timing for control signals and for single word transfers on the NeXT Bus as illustrated by signal **804** [in Fig. 8]." RX-4266 col. 15 lines 55-60. The data strobe signal in Harriman (DSTB*) is timed off of the BusClk, *id.* col. 15 lines 63-67. Although MCLK* is called "internal" in figure 8, it is based on the external system clock BusClk. *See* RX-5429C Q&A 324, 327, 332.

Rambus also argues that Figure 8 of Harriman "shows a single portion of data, not the first and second portion of data, as claimed" by claims 12 and 13 of the '353 patent. Rambus Pet. 40. Claim 12 of the '353 patent requires that there be two portions of data transfer, and that the first portion of the data be sampled "during an odd phase of an external clock signal," and the second portion be sampled "during an even phase of the external clock signal." The patent claim does not specify what is meant by a portion, and the Harriman system transfers data throughout the basic clock cycle shown in Figure 8. Accordingly one portion of the data is transmitted during one phase of the clock cycle and another portion is sampled during the other phase. *See* RX-5429C Q&A 332. We note that the Barth specification nowhere discusses "portions" of data or otherwise sets forth a narrower meaning. Accordingly, we affirm the ALJ's anticipation determination for Harriman for the ALJ's cited reasons supplemented by our discussion above.

(iv) The Yano and Dan Publications

Yano (RX-4261) and Dan (RX-4262) provide similar disclosures of strobe signals, and the ALJ reached identical conclusions for each. He found that each anticipated '353 claim 11. ID at 90-104. We affirm the ALJ's determinations.

(v) The Hayes Patent

The ALJ also found that U.S. Patent No. 5,218,684 to Hayes (RX-4268) anticipates claim 11 of the '353 patent. ID at 117-21. We affirm the ALJ's determination.

b) Obviousness

The ALJ's obviousness determinations were based in large part on combining Rambus's Farmwald patent – which met all of the asserted claim limitations with the exception of a strobe signal – with the art that contained a strobe signal, namely Yano, Dan, NextBus, or Harriman. The ALJ also found that the Scalable Coherent Interface paper (RX-4278C) or JEDEC Standard 21-C Release 4 (RX-2108C) could substitute for Farmwald in these same combinations. Rambus's main argument is that it would not have been obvious to combine Yano or Dan (which allegedly have asynchronous memory) with Farmwald's synchronous memory system. Rambus Br. 50-51. The Commission notice requested further briefing on the issue.

Rambus's argument is that memory technologies were in a state of transition at the time of the Barth patents, from the asynchronous prior-art systems such as Yano and Dan, on the one hand, to the synchronous systems such as Barth and the JEDEC SDRAM and DDR standards, on the other hand. Rambus Br. 29-36. For the reasons set forth in the ID, and as further clarified in the parties' petitions and briefing to the Commission on review, we disagree with Rambus's proposition for the same reasons as the respondents and the IA,

whose briefs on this point are especially helpful. Resp'ts Br. 52-55 (citing, *inter alia*, RX-5429C Q/A 129, 427-44, 496; RX-4275); IA Br. 27-30 (citing RX-2124; RX-2414C; RX-5429C Q/A 105, 129, 492-96). Synchronous memory was not a repudiation of the previous systems, but an evolution, and there is no reason why a person of ordinary skill would turn his or her back on the earlier developments. *See id.* Rambus argues that the fact that it took JEDEC years to develop its synchronous-memory standard is evidence of the difficulty of applying the prior art to synchronous systems. Rambus Br. 35-36. But the mere fact that it took a consensus-oriented organization some time to arrive at an agreed-upon combination of prior art elements does not prove Rambus's point. Accordingly, we affirm the ALJ's findings with respect to the combination of asynchronous and synchronous systems, ID at 211-12, as supplemented by our discussion above.

The parties debate whether Yano and Dan are synchronous or not. Resp'ts Br. 48-51. We do not believe that this distinction matters, because the value of Yano and Dan as prior art do not depend on it. Rambus also argues that SCI is not prior art. Rambus Pet. 50. Because that art is cumulative with other art presented in this investigation, we have determined not to reach the question whether it is prior art, and therefore base our obviousness determinations on combinations with Farmwald or JEDEC Release 4. We take no position on the ALJ's obviousness determinations that rely on SCI.

We affirm the ALJ's obviousness determinations that rely on the anticipatory art (Yano, Dan, NextBus, Harriman) in combination with Farmwald or JEDEC Release 4. ID at 212-23. As the ID properly and frequently explained in connection with each prior art combination, the known functionalities of the asynchronous prior art yielded "predictable

results."[14] ID at 212-223; *see KSR Int'l Co. v. Teleflex Inc.*, 500 U.S. 398, 417 (2007) ("If a person of ordinary skill can implement a predictable variation, section 103 likely bars its patentability."). We note that the PTO drew the same conclusions during reexamination. *See* ID at 212.

c) Secondary Considerations

The ALJ found that Rambus's secondary-considerations evidence did not preclude his determinations of obviousness. ID at 226-27. We affirm the ALJ's determinations. *Id.* In addition, we further find that even if we credited Dr. Przybylski's testimony, our findings of obviousness would remain the same. The evidence of secondary considerations is weak for the Barth patents. Industry did not jump to the Rambus technology, but instead to the standard developed by the JEDEC standards-setting body. As the IA recognized, the "mere fact that others in the industry adopted 'strobe signal' based technology is insufficient to show secondary considerations of nonobviousness," because otherwise every infringement suit would automatically confirm the nonobviousness of the patent." IA Reply Br. 14 (citing *Wyers v. Master Lock Co.*, 616 F.3d 1231, 1246 (Fed. Cir. 2010)).

C. Inequitable Conduct (Barth – Failure to Disclose SyncLink)

1. Background

We affirm the ALJ's conclusion of no inequitable conduct, but our reasons for finding no inequitable conduct differ from those of the ALJ with respect to the materiality

[14] We find that the respondents demonstrated the motivation to combine the references relied upon by the ALJ to find the asserted patent claims obvious. The respondents' testimony on these issues was thorough, credible, and persuasive. RX-5429C Q/A 486-501, 505-19, 524-42. We also find that the respondents demonstrated a reasonable expectation of success in combining the references, in view of the predictability discussed by the ALJ. *See also* RX-5429C Q/A 533-38.

requirement.[15] The respondents argued that Barth patents are unenforceable because the inventors withheld a SyncLink standards document from the PTO during prosecution. SyncLink was a draft standard for a high-speed memory interface, sponsored by the Microprocessor and Microcomputer Standards Subcommittee of the IEEE Computer Society. RX-4270C.0001. RamLink was a previous IEEE standard, and SyncLink used the RamLink protocols. *Id.* (abstract). To demonstrate materiality, the respondents argued that these standards anticipated claims 11-13 of the '353 patent and claims 1, 20, and 24 of the '109 patent.

The ALJ rejected the respondents' argument. He found that these standards were much like the Farmwald '037 patent that was before the patent examiner and therefore cumulative with the art of record. ID at 123, 246-47. The ALJ also found that the inventors and counsel lacked a specific intent to deceive. *Id.* at 246-47.

2. Materiality

On petition, the Respondents asserted that SyncLink generally, as well as the predecessor RamLink standard, are material. Resp. Pet. 32-34. In their post-hearing brief, the respondents waived RamLink-related arguments. Resp'ts Post-Hearing Br. 42 n.29 ("Due to page limitations, Respondents have elected not to discuss these prior art references [including Ramlink (RX-4272C)] in detail."); *id.* at 216 (stating, without explaining, that

[15] "To prevail on an inequitable conduct defense, a defendant must establish both the materiality of the withheld reference and the applicant's intent to deceive the PTO." *Aventis Pharma S.A. v. Hospira, Inc.*, No. 2011-1018, slip op. at 15 (Apr. 9, 2012) (citing *Therasense, Inc. v. Becton Dickinson & Co.*, 649 F.3d 1276, 1290 (Fed. Cir. 2011) (en banc)). "[B]ut-for materiality is the standard for evaluating the materiality prong of the analysis unless there is affirmative egregious misconduct." *Aventis*, slip op. at 15. "A prior art reference 'is but-for material if the PTO would not have allowed a claim had it been aware of the undisclosed prior art.'" *Id.* at 16 (quoting *Therasense*, 649 F.3d at 1291).

"SyncLink and RamLink anticipate all asserted claims of the '353 patent and claims 1, 20, and 24 of the '109 Patent; thus, they are indisputably material references."). Accordingly, all that the respondents rely upon to demonstrate materiality of RamLink is a single sentence from their post-hearing brief regarding Rambus employee Mr. Crisp's knowledge that a draft RamLink standard stated that "[t]he incoming signals are source-synchronous; the data's *strobeIn* signal, not the *clockRefIn* signal, provides the sample timing for the incoming data." Resp'ts Post-Hearing Br. 211 (modification and emphasis in original) (quoting RamLink Draft 1.0 (RX-4274C.0058)). In their petition for review, the respondents argue that that sentence "[a]lone informs one of skill in the art that in the RamLink interface a strobe signal may be used to time the sampling of incoming data, which is precisely the 'direct control' configuration the ALJ found is within the scope of the asserted Barth patent claims." Resp'ts Pet. 33. This single sentence fails to preserve any substantial argument that RamLink is material prior art.[16]

As to the SyncLink documents, the respondents do not focus on whether any SyncLink document was prior art, but on whether Rambus was familiar with SyncLink proceedings. *Therasense* requires knowledge of invalidating prior art, and the respondents have failed to allege that any documents other than the draft specification from 1995 (RX-4270C) were anticipatory. Respondents Post-Hearing Br. 211-12. We have already found that the respondents failed to demonstrate that RX-4270C was prior art. Accordingly, the respondents have failed to demonstrate materiality of the only document that could result in a

[16] Even if the respondents' arguments were to be found not to have been waived, their petition failed to satisfy their burden to demonstrate that the ALJ's findings were erroneous. 19 C.F.R. § 210.43(b)(1).

finding of inequitable conduct. Accordingly, the Commission takes no position on the issues whether SyncLink was cumulative with Farmwald or whether SyncLink would have been anticipatory if it were prior art. Those issues are moot.

3. Intent to Deceive

The ALJ found that the respondents failed to demonstrate intent to deceive the PTO. ID at 247 (citing the trial transcript). We affirm the ALJ's determination that the respondents' showing was insufficient for the reasons stated in the ID.

D. Infringement

The ALJ rejected all of the respondents' noninfringement arguments. There are a number of infringement questions presented upon Commission review. Some of the issues are limited to specific accused products: certain LSI [redacted] products, and certain Cisco products with transmitters alleged to be disabled. Other issues cut more broadly: whether the Dally multiple-transmitter claims ('857 claims 11-13, 32-34, 50-52) have been infringed; whether Rambus can rely upon direct infringement of the method claims of the Barth and Dally patents to prove a violation of section 337; and whether Rambus's showing of indirect infringement for the Barth and Dally patents was adequate. Some additional issues depend on claim constructions that we have rejected – *e.g.*, whether the Dally "transmitter" excludes "conventional FIR filters" – and we do not address those points further.

1. Direct Infringement

The Commission affirms the ALJ's findings of direct infringement as to the Barth patents. ID at 47-64. Subject to the following discussion specific to the multiple transmitter claims of the Dally patents, as well as whether certain LSI and Cisco products directly

infringe the asserted Dally patent claims, the Commission affirms the ALJ's findings of direct infringement as to the Dally patents, *id.* at 68-74, 78-85.

a) Dally Patents – Multiple Transmitter Claims

Certain asserted Dally patent claims call for "multiple transmitters" ('857 claims 11-13, 32-34, 50-52; '494 claims 26, 40) and the ALJ found these claims to have been infringed. ID at 79-81.

In connection with his invalidity analysis, the ALJ required that the multiple transmitter claims of the '857 patent (but, appropriately, not the '494 patent) be connected to a common processor. ID at 155. In our discussion of invalidity, we affirmed that construction. In applying that same construction for the purposes of infringement, we find that Rambus has failed to demonstrate infringement of the '857 patent's multiple-transmitter claims based on the ALJ's requirement that the transmitters be connected to a common processor. Rambus's argument in support of infringement improperly suggests that it was the remaining respondents' burden to demonstrate non-infringement. Rambus Reply Pet. 30. We have reviewed the record, including the portions of Dr. Singer's witness statement cited by the ALJ for support for his determination of infringement of the multiple-transmitter limitations. CX-9542C at Q/A 294-95, 298-306. For example, Dr. Singer's witness statement asserts infringement of the multiple transmitter claims on the mere basis that "[m]any of the Accused Products contain more than one transmitter circuit." *Id.* at Q/A 295; *accord id.* at Q/A 298 (STMicro products); Q/A 305 (LSI products); accord Rambus Post-Hearing Br. 199 ("The evidence shows that many of the Accused Products include additional transmitter circuits such that they contain these claimed features."). Neither the witness

statement nor the post-hearing brief demonstrates, or alleges, that the accused products have multiple transmitters connected to a common processor, as required by the claims. Furthermore, Dr. Singer's testimony at trial, which permits multiple processors, Tr. 802:6-103:15, prevents the inference that Rambus made such a demonstration. Accordingly, we find the multiple-transmitter claims of the Dally '857 patent not to be infringed.

b) Dally Patents – Certain LSI Products

The respondents petitioned for review of the ALJ's finding that certain LSI products do not infringe the asserted Dally patent claims. They contend that the Dally claims cover equalization "as a function of the digital value represented by that signal level and of the digital values represented by one or more preceding signal levels," '857 claim 24, and nothing else. By contrast, they claim that the LSI accused products also perform equalization as a function of a succeeding bit as well. In short, a filter that relies only on the current and preceding bit is a [redacted]. *See* ID at 75.

The ALJ found that LSI's products [redacted]. *Id.* at 76. There is no genuine dispute on this point. The ALJ then stated:

> [T]he ALJ notes that LSI fails to recognize that the asserted claims of the Dally patents are apparatus claims, not method claims. The law is clear that Rambus need not show actual use of LSI's [redacted] products in [redacted] to demonstrate infringement of the asserted apparatus claims. Rather, Rambus need only show that the LSI [redacted] products are designed for [redacted] and that users of those products can [redacted] without having to modify the product in question.

ID at 77. For support, the ALJ relied on *Silicon Graphics, Inc. v. ATI Technologies., Inc.*, 607 F.3d 784, 794 (Fed. Cir. 2010) and a case cited therein, *Fantasy Sports Properties, Inc. v. Sportsline.com, Inc.*, 287 F.3d 1108, 1118 (Fed. Cir. 2002).

The Commission notice asked two questions about this issue. First, the Commission notice sought further briefing on method claims 39, 40, and 42 of the Dally '494 patent. 77 *Fed. Reg.* at 27250. This was because the ALJ treated these claims as apparatus claims. Second, the notice sought further briefing on *Silicon Graphics*, *Fantasy Sports*, and another case, *ACCO Brands, Inc. v. ABA* Locks *Manufacturer Co.*, 501 F.3d 1307, 1310 (Fed. Cir. 2007), as to the apparatus claims. 77 *Fed. Reg.* at 27250. The ALJ's *Fantasy Sports*-related discussion dealt with the fact that apparatus claims can infringe despite the ability of the products also to be used in noninfringing ways. Method claims, by contrast, necessarily require performance of the method. Although Dally claims 39, 40 and 42 are methods, the ALJ asserted that all of the Dally claims cover apparatuses. ID at 77 ("the ALJ notes that LSI fails to recognize that the asserted claims of the Dally patents are apparatus claims, not method claims").

On review, and as to the asserted method claims of the Dally '494 patent, the Commission vacates the ALJ's finding of infringement for the LSI [redacted] products. The Commission has determined to take no position on whether the LSI [redacted] products infringe '494 method claims 39, 40 and 42. We note that Rambus's brief glossed over the method claims by stating: "Since most of the asserted Dally claims are apparatus claims, demonstrating actual use is not required." Rambus Post-Hearing Reply Br. 105.

As to the asserted apparatus claims, the IA argued that the claim language of *Silicon Graphics* is close to that of the Dally patents. IA Br. 42-43. Rambus agrees. Rambus Br. 44-46. The respondents argue that *ACCO* is closer on point. Resp'ts Br. 28-29. The respondents argue that the language of *Silicon Graphics* and *Fantasy Sports* is distinguishable, but they fail to explain why. *Id.* at 29. We find the IA's discussion persuasive, IA Br. 26-27. *Silicon Graphics* called for "a rasterization circuit . . . that rasterizes the primitive according to a rasterization process." *Silicon Graphics*, 607 F.3d at 788. The Federal Circuit found that the claim language merely required circuitry with the ability to rasterize. *Id.* at 795. We conclude that the claim language at issue here cannot adequately be distinguished from *Silicon Graphics*, and we affirm the ALJ's determination of infringement of the apparatus claims for the reasons stated in the ID supplemented by our discussion above.

c) Dally Patents – Certain Cisco Products

In their petition, the respondents contended that certain Cisco accused products did not infringe the Dally patents because "the accused transmitter is not connected to anything else." Resp'ts Pet. 48. The ID found that Cisco's "merely stating that they are 'not connected' without further detail, is not evidence that the interface is permanently disabled." ID at 72; *see* Resp'ts Post-Hearing Br. 133. The Commission notice of review requested that the parties brief the following question: "The disablement of the Cisco products with a disabled transmitter (Dally patents), see Resp. Pet. 48, as compared to the disablement of the SL500 prior art products, see Rambus Pet. 17-20." 77 *Fed. Reg.* at 27250.

On review, we find that Rambus has not demonstrated infringement of the Dally method claims (Dally '494 patent claims 39, 40, 42). Those claims require, *inter alia*,

"sending a differential output signal," '494 claim 39, and Rambus has not demonstrated the performance of the method claims by these Cisco products.

For the apparatus claims, the IA urges the same result as for the LSI products:

> [B]ecause a user does not have to modify the accused Cisco products (*e.g.*, by manipulating them in a particular manner as in *ACCO*) to include transmitter circuitry with pre-emphasis functionality as claimed, the mere presence of that circuitry in those products is sufficient to support a finding of infringement irrespective of the fact that it must be coupled to an output to enable that functionality.

IA Br. 27. Although these facts for Cisco may present a closer case than for LSI, we have determined to affirm the ALJ's finding of infringement of the apparatus claims.

2. The Barth and Dally Method Claims Generally

All of the asserted Barth claims are methods. Among the asserted Dally claims, the only asserted method claims are independent claim 39 and dependent claims 40 and 42 of the '494 patent. The respondents raise the question of the effect of the Commission Opinion from *Image Processing Systems* [17] with respect to the method claims of both patents, asserting that there can be no violation of section 337. Resp'ts Pet. 23-24. The Commission takes no position whether direct infringement of the method claims, standing alone, would constitute a violation of section 337(a)(1)(B)(i). *Image Processing Systems*, Comm'n Op. at 14-17. The *Image Processing Systems* opinion does not preclude a complainant from relying upon infringement in the United States as a predicate for indirect or contributory infringement. *Id.* at 18 & n.11. Here, as will be discussed immediately below, Rambus

[17] *See Certain Elec. Devices with Image Processing Sys., Components Thereof, and Associated Software*, Inv. No. 337-TA-724, Comm'n Op. (public version Dec. 21, 2011) ("*Image Processing Systems.*").

proved indirect infringement for each of the claims for which direct infringement has been shown.

3. Indirect Infringement

The ALJ found indirect infringement of the method claims of both patent families by reason of inducement and contributory infringement. ID at 65-67, 82-85. The respondents challenge these findings on the basis that they lack sufficient intent to infringe indirectly. We affirm the ALJ's findings that each of the claims that has been infringed directly has also been infringed indirectly, for the reasons set forth in the ID, supplemented by the following discussion.

a. Inducement

The ALJ found that the respondents had taken "active steps demonstrating a specific intent to induce infringement" of the Barth patents, by reason of: "advertising the infringing use and providing technical support, instructions, tutorials, software device drivers and other materials directing end users to operate the Accused Products in an infringing manner." ID at 66. Similarly, for the Dally patents, the ALJ found that respondents LSI and STMicro "induce infringement of end-users by engaging in numerous activities that demonstrate an intent to cause infringement." *Id.* at 83.

The respondents allege that the ALJ's findings are not enough to demonstrate inducement, and that culpable conduct is required. They claim that in light of their "objectively reasonable belief that the asserted claims of the [asserted] patents were non-infringed, unenforceable, and invalid," that they lack such culpability. Resp'ts Pet. 25, 49. We reject the respondents' arguments and affirm the ID for the following reasons

supplemental to the ID. The respondents point to no cases setting the inducement bar as high as they advocate. To the contrary, the types of materials that the ALJ relied upon to demonstrate inducement are ordinary: user manuals for how to perform an action that infringes, and technical support to assist. *See, e.g.*, ID at 66, 83. This is precisely the sort of evidence used by the court of appeals in, for example, *Lucent Technologies, Inc. v. Gateway, Inc.*, 580 F.3d 1301, 1318-19 (Fed. Cir. 2009) and *i4i Ltd. Partnership v. Microsoft Corp.*, 598 F.3d 831, 851-52 (Fed. Cir. 2010), *aff'd on other grounds*, 131 S. Ct. 2238 (2011). Unlike *DSU Medical Corp. v. JMS Co.*, 471 F.3d 1293, 1307 (Fed. Cir. 2006), the respondents offered no evidence that they had received opinions of counsel that they did not infringe. Instead, the respondents merely assert that they had plausible litigation defenses. Many or most accused infringers have such plausible defenses, including the defendants in *Lucent* and *i4i*.

b. Contributory infringement

The ALJ reached similar findings for contributory infringement. He found that there were no substantial noninfringing uses for the accused products. ID at 67, 83. He also found that the respondents have "taken no actions to change how their products work and have not stopped distribution or sale of the Accused Products." *Id.* at 67.

The respondents echo their arguments for inducement: because they purportedly had objectively reasonable defenses, they did not act "knowing" their products were "especially made or especially adapted for use in an infringement of such patent." 35 U.S.C. § 271(c); *see* Resp'ts Pet. 25, 49. We reject the respondents' arguments and supplement the ID's reasoning with the following discussion. The respondents' argument is contravened by the

caselaw. Where there is no substantial noninfringing use, knowledge of infringement is presumed. *Spansion, Inc. v. ITC*, 629 F.3d 1331, 1355 (Fed. Cir. 2010). The respondents do not argue any substantial noninfringing uses as to the Dally patent claims. Accordingly, knowledge of infringement is to be presumed, and contributory liability found. We affirm the ID's analysis and conclusion.

The respondents argue that there are substantial noninfringing uses of the products accused of infringing the Barth patents. Resp'ts Pet. 25. We affirm the ALJ's determinations of no substantial noninfringing uses, ID at 67, subject to the following further reasoning regarding a subset of STMicro's accused products. *See* Resp'ts Pet. 63-64. The ID's treatment of the STMicro issue was limited to a footnote, ID at 67 n.9,[18] and the Commission's notice of review requested further briefing. The parties' briefing has clarified the matter. The accused STMicro memory controllers (the [redacted] products) have infringing and non-infringing modes of operation, but [redacted], they will always infringe. *See* Resp'ts Reply Br. 36-37; Rambus Br. 48-50. Under the guiding Federal Circuit caselaw, the accused circuitry must have no other uses but infringement; one does not establish noninfringing uses based on other features of the accused product. *See* Rambus Br. 49; *see also Fujitsu Ltd. v. Netgear Inc.*, 620 F.3d 1321 (Fed. Cir. 2010); *Lucent Technologies, Inc. v. Gateway, Inc.*, 580 F.3d 1301, 1320 (Fed. Cir. 2010); *Ricoh Co. v. Quanta Computer Inc.*, 550 F.3d 1325, 1340 (Fed. Cir. 2008). In view of these cases, we find that the accused STMicro controllers [redacted]

[18] Footnote 9 of the ID incorrectly attributed the subject STMicro products to respondent Seagate. ID at 67 n.9.

[redacted] that infringes. As such, the substantial-noninfringing-use issue falls away for these STMicro products.

E. Domestic Industry

The ALJ determined that Rambus satisfied the economic prong of the domestic industry requirement for both the Dally and Barth patents. ID at 347-63. We reverse the ALJ's determination and find that Rambus has not met its burden of proving a "substantial investment" in the exploitation of the Dally and Barth patents pursuant to 19 U.S.C. § 1337(a)(3)(C).

In order to establish a violation of Section 337 in a patent-based action, a complainant must demonstrate that a domestic industry either exists in the United States or is in the process of being established. *See* 19 U.S.C. § 1337(a)(2). The statute recites:

> **(2)** Subparagraphs (B), (C), (D), and (E) of paragraph (1) apply only if an industry in the United States, relating to the articles protected by the patent, copyright, trademark, mask work, or design concerned, exists or is in the process of being established.
>
> **(3)** For purposes of paragraph (2), an industry in the United States shall be considered to exist if there is in the United States, with respect to the articles protected by the patent, copyright, trademark, mask work, or design concerned—
>
> > **(A)** significant investment in plant and equipment;
> >
> > **(B)** significant employment of labor or capital; or
> >
> > **(C)** substantial investment in its exploitation, including engineering, research and development, or licensing.

19 U.S.C. § 1337(a)(2)-(a)(3).

The Commission has explained the showing required of a complainant relying on licensing activity to demonstrate the existence of a domestic industry:

> Complainants who seek to satisfy the domestic industry requirement by their investments in patent licensing must establish that their asserted investment activities satisfy three requirements of section 337(a)(3)(C). First, the statute requires that the investment in licensing relate to "its exploitation," meaning an investment in the exploitation of the asserted patent. 19 U.S.C. § 1337(a)(3)(C) . . . . Second, the statute requires that the investment relate to "licensing." 19 U.S.C. § 1337(a)(3)(C) . . . . Third, any alleged investment must be domestic, i.e., it must occur in the United States. 19 U.S.C. § 1337(a)(2), (a)(3). Investments meeting these requirements merit consideration in our evaluation of whether a complainant has satisfied the domestic industry requirement. Only after determining the extent to which the complainant's investments fall within these statutory parameters can we evaluate whether complainant's qualifying investments are "substantial," as required by the statute. 19 U.S.C. § 1337(a)(3)(C). If a complainant's activity is only partially related to licensing the asserted patent in the United States, the Commission examines the strength of the nexus between the activity and licensing the asserted patent in the United States.

Certain Multimedia Display and Navigation Devices and Systems, Components Thereof, and Products Containing Same, Inv. No. 337-TA-694, Comm'n Op. at 7-8 (footnotes omitted) (August 8, 2011) ("*Navigation Devices*").

Thus, there are three inquiries: (1) whether the investment in licensing relates to exploitation of the asserted patents (*i.e.*, the nexus to the asserted patents); (2) whether the investment relates to licensing; and (3) whether the investment is domestic. Once those inquiries are completed, the Commission can assess whether the investment is "substantial" as required by the statute. In this investigation, there are no genuine disputes regarding the second and third inquiries: Rambus's expenses are licensing-related and they accrue in the United States. Accordingly, the two issues we have examined most closely on review are whether the investments identified by Rambus have a sufficient nexus to the asserted patents, and if so whether Rambus's licensing investments are substantial.

To establish that it made investments in licensing with a nexus to both the Dally and Barth patents, Rambus relied on three kinds of evidence: its total investment in its entire

patent licensing program; the amount of licensing revenue received by Rambus for patent portfolios that include the Dally and Barth patents; and the number of licenses for each of these patent families. ID at 343, 358. Specifically, Rambus relied on the following to satisfy the economic prong of the domestic industry requirement:

> Since 2006, Rambus has invested over $[redacted] in activities directly related to its overall licensing operations in the United States and over $[redacted] toward marketing efforts in the United States . . . Since 2006, Rambus has had over 30 U.S. employees directly involved [in its licensing efforts].

Rambus Post-Hearing Br. 289. For the purpose of the domestic industry requirement, Rambus also relied on the fact that it has received over $[redacted] in royalties for licenses to its Concurrent Interface Technology which encompasses the Barth patents, and that it has also received over $[redacted] in royalties for patent license agreements, which include a license to the Barth patents. *Id.* at 290-91; ID at 356. Similarly, Rambus relied on the over $[redacted] in royalty revenue it received for it Serializer-Deserializer (SerDes) technology licenses, which encompass the Dally patents. Rambus Post-Hearing Br. 291; *see also* ID at 360 (over $[redacted] for technology licenses that included the Dally patents). *Id.* at 358-60.

We find that Rambus has not come forth with sufficient evidence for us to identify or reasonably estimate the portion of its overall investments in licensing that have a nexus to the asserted patents, and, accordingly, that there is also insufficient evidence for the Commission to determine whether Rambus's relevant licensing investments are "substantial."[19] The

[19] The Commission assumes for its analysis that Rambus has demonstrated a nexus between the asserted Barth and Dally patents and the portfolios that include them (the Concurrent Interface Technology licenses and the Serializer-Deserializer technology licenses, respectively). *See* ID at 347-48 (Concurrent Interface Technology); *id.* at 358-59 (Serializer-Deserializer). *See generally Navigation Devices*, Comm'n Op. at 12 ("Evidence showing how the asserted patents fit together congruently with other patents in the portfolio covering a specific technology may demonstrate a stronger nexus to the licensing

(Footnote continued on the next page)

Commission is therefore reversing the ALJ's finding of a domestic industry for both asserted patent families based on Rambus's patent licensing program. ID at 343-64.

As the ALJ correctly acknowledged, "strict mathematical proof of the investment in licensing certain patents among others in a portfolio may not be possible" and that the Commission in the *Navigation Devices* did not put the complainant to such a task. ID at 357. The total amount of licensing expenditures and total number of licensing-related employees, however, does not allow the Commission to qualitatively or quantitatively determine what portion of the $[redacted] expended by Rambus, or what portion of the expenses associated with the activities of the 30 Rambus employees that work on the overall licensing program, could be allocated in some fashion to licensing the Dally and Barth patents.

In the ID, the ALJ bridged the absence of any direct evidence relating to Rambus's investments in the Dally and Barth patents by extrapolating from the total licensing revenues and the number of licenses for the portfolios containing the asserted patents. For the Barth patents the ALJ reasoned:

> Focusing on Rambus's overall patent portfolio, the Respondents argue that the fact that the *licensed* groups of patents (*e.g.*, the Concurrent RDRAM group which includes the Barth I patents) on which Rambus relies are of much smaller size than the portfolio as a whole is irrelevant because Rambus is relying on the amount of the entire licensed portfolio. (RIB at 283.) While Rambus has not allocated its expenditures to particular sub-portfolios or sub-groups *per se*, the evidence provides at least some circumstantial evidence of correspondingly significant investments in those portfolios. For example, in 2008, $87,738,202 was attributable to royalties from patent license agreements that grant rights to the Barth Patents. (CX-7617C.0004; *see also* CX-9547C, Smith Direct Q/A 154-156 (testifying as to CX-7617C).) In addition, approximately $266,342 in

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activity . . . ."). Even under that assumption, what is wanting in this investigation, and what is discussed in detail, *infra*, is evidence specifically demonstrating investment made in the licenses upon which Rambus relies, as opposed to overall firmwide licensing expenses.

> revenue was attributable to Concurrent RDRAM royalties, which also relate to the Barth Patents. (CX-7616C.0003; *see also* CX-9547C, Smith Direct Q/A 151-153 (testifying as to CX-7616C). This revenue information is at least strong circumstantial evidence that Rambus's investments in the asserted sub-portfolios/sub-groups are substantial as well.

ID at 349; *see also* ID at 363 (relying on royalty revenue from the SerDes technology licenses that encompass the Dally patents).

Based on the record in this investigation, however, we decline to adopt the reasoning set forth in the ID, which relies entirely on the circumstantial evidence of Rambus's licensing revenues and the number of licenses as an adequate proxy for the "investments" made in licensing the Dally and Barth patents. The Commission remains of the view that licensing revenues can be circumstantial evidence used to support a domestic industry. *See Navigation Devices*, at 24 ("[t]he significance of royalties in evaluating whether Pioneer's investment is substantial was disputed by the parties and the commenters. Although royalties received by a complainant can be circumstantial evidence that an investment was made, they do not constitute the investment itself."); *see also Liquid Crystal Display Devices* at 123-24 ("[w]hile the ALJ found that this was strong evidence that Thomson's investment is substantial, we caution that royalties do not constitute the investment itself. *Navigation Devices*, Comm'n Op. at 24. Rather, they are circumstantial evidence that an investment was made and are consistent with our conclusion that Thomson's investment in the asserted patents was substantial."). However, consistent with the Commission's opinion in *Navigation Devices*, Rambus's licensing revenues for the Dally and Barth patents "do not constitute the investment[s]" themselves. While mathematical precision is not required, only Rambus was in a position to come forth with some analysis of its own licensing operations

from which its investments could be apportioned to the Dally and Barth patents. Rambus did not meet this burden.

Although we find that Rambus failed to come forward with sufficient evidence of a nexus between its investment in licensing and the asserted patents, Rambus was not required to provide a precise allocation of its licensing investments on a patent-by-patent basis in this investigation in order to make a sufficient evidentiary showing. Just as the Commission has found that complainants are not required to define or quantify the domestic industry itself in absolute terms, the Commission has also held that "[i]n addition, we see no reason to believe that Congress intended the domestic industry to be established only on the basis of licenses covering individual patents." *Liquid Crystal Display Devices* at 115-16.

Without an adequate evidentiary basis for evaluating the level of investments for the two asserted patent families, the Commission is left without sound footing for evaluating whether any such investments are "substantial." In *Navigation Devices*, we stated:

> Once a complainant's investment in licensing the asserted patent in the United States has been assessed in the above manner, the next inquiry is whether the investment is substantial. 19 U.S.C. § 1337(a)(3)(C). In performing our analysis, we adopt a flexible approach whereby a complainant whose showing on one or more of the three section 337(a)(3)(C) requirements is relatively weak may nevertheless establish that its investment is "substantial" by demonstrating that its activities and/or expenses are of a large magnitude.

Comm'n Op. at 15. Here, however, the Commission does not know what portion of the $[redacted] in total licensing expenditures incurred by Rambus, or what portion of time or expenses incurred by the 30 Rambus employees, might be allocated to the Dally and Barth patents. We are not seeking exact amounts or quantities of investments. *Liquid Crystal Display Devices* at 115-16 ("[a]s we have stated '[i]ndeed, Congress, by using the word 'substantial,' indicated that no mathematical precision is required when assessing the amount

a complainant has invested in each patent", *citing* 19 U.S.C. § 1337(a)(3)(C), and *Certain Stringed Musical Instruments and Components Thereof*, Inv. No. 337-TA-586, Comm'n Op. at 25-26 (May 16, 2008) ("[T]here is no need to define or quantify the industry itself in absolute mathematical terms."). Yet, even though Rambus almost certainly made investments in licensing the Dally and Barth patents, we are unable to find grounds upon which these unknown investments could be considered "substantial."

Finally, we note that in *Synchronous DRAM Memory Controllers,* Inv. No. 337-TA-661, we did not review the ALJ's summary determination that Rambus demonstrated the existence of a domestic industry.[20] We have reviewed the record in that investigation and note that, unlike the Respondents in this investigation, the respondents' petition for Commission review did not squarely challenge the adequacy of Rambus's firm-wide showing, and instead focused on the unrelated nexus issues of whether the asserted patents were important to the licensed portfolio of patents. *Synchronous DRAM Memory Controllers,* Pet. for Review of Order No. 21 at 9 (Oct. 16, 2009). It is our understanding that in the appellate proceedings for *Synchronous DRAM Memory Controllers*, the respondents attempted to rehabilitate their domestic-industry arguments, including based on Rambus's firm-wide expenses presented in that investigation. In our view, those arguments came too late, and the remedial orders in that investigation have since been rescinded.

In any event, unlike the respondents in *Synchronous DRAM Memory Controllers*, the respondents here have squarely challenged the ALJ's determination based on the

[20] *Synchronous DRAM Memory Controllers*, Notice of Comm'n Determination Not to Review an Initial Determination Granting Complainant's Motion that Its Licensing Activities in the United States Satisfy the Domestic Industry Requirement (Nov. 6, 2009).

Commission opinion in *Navigation Devices*. The respondents particularly fault Rambus for providing information about its licensing investments generally, as opposed to investments in "specific efforts to license the Barth or Dally patents or even portfolios containing them." Resp't's Pet. 69. We agree, for the reasons explained above, that Rambus needed to have provided additional evidence of its investments in licenses specific to the Dally and Barth patents.

For the reasons already explained above, we find that Rambus has failed to demonstrate the existence of a domestic industry, a prerequisite to finding a violation of section 337.

F. Unclean Hands

The ALJ found unclean hands as to the Barth patents based on Rambus's document destruction in the late 1990s.[21] We affirm. The chronology of events is set forth in detail in pages 256-305 of the ID.

In *Synchronous DRAM Memory Controllers*, Inv. No. 337-TA-661, the ALJ found that certain infringement litigation was reasonably foreseeable to Rambus by July 1998, and Rambus failed to put a litigation hold on its document destruction. The ALJ found that Rambus's spoliation subsequent to that date was done in bad faith but that the respondents bore the burden of demonstrating that the document destruction was prejudicial to the respondents, *i.e.*, that some of the destroyed documents were pertinent to the investigation.[22]

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[21] The Dally patents, which Rambus acquired much later from MIT, are not tied up in these allegations of unenforceability.

[22] Inv. No. 337-TA-661, Initial Determination on Violation of Section 337 and Recommended Determination on Remedy and Bond 96-116 (Jan. 22, 2010).

In *Synchronous DRAM Memory Controllers*, the respondents did not carry that burden. Instead of taking discovery on the spoliation, including depositions of the Rambus employees at the time, the respondents in the *Synchronous DRAM Memory Controllers* investigation relied on the evidence taken in the district court actions in *Hynix* and *Micron*.[23] Those infringement actions involved different asserted patents, and different affirmative defenses to which the destroyed documents could have pertained. In each instance where the respondents in *Synchronous DRAM Memory Controllers* asserted – based on the testimony from the *Hynix* and *Micron* lawsuits – that pertinent materials had been destroyed, Rambus demonstrated that the evidence had actually been produced. The Commission determined not to review the ALJ's determination that the respondents had not demonstrated that Rambus's unclean hands in document destruction resulted in the Barth patents' unenforceability.

After the Commission's briefs were filed in the appeals of the Commission determination in *Synchronous DRAM Memory Controllers*, the Federal Circuit issued its *Hynix* and *Micron* opinions. In *Micron*, the Federal Circuit determined, as a question of first impression, that where bad faith destruction is found to occur, the parties alleging spoliation must "only come forward with plausible, concrete *suggestions* as to what the destroyed evidence *might have been*." *Micron*, 645 F.3d at 1328 (modifications omitted; emphasis in original).

In the instant investigation, the ALJ repeated his earlier determination that Rambus's obligation to preserve documents began no later than July 1998. ID at 256-58. The ALJ

[23] *See generally Micron Tech., Inc. v. Rambus Inc.*, 645 F.3d 1311 (Fed. Cir. 2011); *Hynix Semiconductor Inc. v. Rambus Inc.*, 645 F.3d 1336 (Fed. Cir. 2011).

then determined that Rambus failed to show lack of prejudice by clear and convincing evidence, as required by *Micron*. ID at 312. He stated:

> Rambus presents no evidence that the documents destroyed were ever cataloged. A bad faith spoliator cannot expect to benefit from destroying documents in bad faith and then claim lack of prejudice when it has no list or catalog of what was destroyed. In this situation, the presumption that the bad faith spoliator's document destruction prejudiced the Respondents is particularly strong.
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> Specifically, Rambus destroyed numerous emails and backup tapes. For example, Mr. Barth left behind tens of thousands of emails when he abruptly left Rambus, all of which would have been destroyed under the retention policy. (Barth, Tr. 441:11-24, 452:17-23.) Email correspondence, from Mr. Barth alone, could have provided support for Respondents' invalidity contentions. Although Rambus argues that Respondents have not shown that many of these documents ever existed or were destroyed, Rambus confuses whose burden it is to prove the existence or nonexistence of such documents. (CIB 81.) Rambus continually states that Respondents failed to make a concrete and plausible suggestion. However, due to Rambus' bad faith spoliation, Respondents' are not required to meet such a high standard, in fact, it is because of Rambus' bad faith spoliation that they cannot. (CIB 82-94.) Although witnesses testified that they were unaware of documents questioning the patentability of the Barth Patents that were destroyed during one or more of the shred days, this does not amount to clear and convincing evidence. (See Hampel, Tr. 369:09-13, 372:21-373:09; CX-10767, Hampel Rebuttal Q/A 12-17; Barth, Tr. 475:09-13; Vincent, Tr. 2248:06-17.) Therefore, Rambus failed to show, by clear and convincing evidence, that its bad faith spoliation did not prejudice the Respondents.

ID at 313.

The ALJ found that there was no lesser sanction short of finding the patents unenforceable that would be appropriate. *Id.* at 314-15. The ALJ rejected the IA's recommendation for a lesser sanction[24] as inadequate for three reasons. First, he rejected the

[24] The IA had recommended an adverse inference instead of unenforceability, "such as precluding Rambus from antedating prior art (*e.g.*, due to an alleged inability to challenge evidence of conception and reduction to practice), adverse inferences on invalidity (*i.e.*, due

(Footnote continued on the next page)

argument that there was "a lesser degree of culpability here than in the *Micron* and *Hynix* line of cases." *Id.* Rather, the ALJ found the culpability the same. ID at 315-16. Second, the ALJ found that "the degree of prejudice resulting from Rambus' spoliation is severe because the Respondents are forced to rely on incomplete and spotty evidence." *Id.* at 316 (quotation omitted). He observed that the "types of documents destroyed by Rambus relating to the Barth Patents, such as Mr. Barth's emails, documents Mr. Barth received regarding JEDEC, etc., would likely be 'at the heart' of Respondents' invalidity defenses." *Id.* Third, he found that unenforceability was appropriate to "deter such conduct by others." *Id*

Rambus petitioned for review of the ALJ's determination of the 1998 date upon which its document preservation obligations arose. We have determined to affirm the ALJ's findings regarding the date upon which Rambus's obligations arose. Rambus also challenges the ALJ's finding of bad faith, and we affirm the ALJ's findings regarding Rambus's bad faith.

We affirm the ALJ's determination that Rambus has not carried its burden of showing no prejudice as a result of the document destruction. The respondents distinguish the earlier Synchronous DRAM Memory Controllers investigation by arguing that they "asserted here a defense of anticipation based on SyncLink, as well as a defense of inequitable conduct based on SyncLink and RamLink prior art" that were not present in the earlier Synchronous DRAM Memory Controllers investigation. Resp'ts Reply Pet. 91. We agree that the respondents have offered "concrete plausible suggestions" in this case. That we have rejected their anticipation and inequitable conduct arguments on the merits cannot be dispositive because a

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to an alleged possibility that prior art materials were destroyed), etc." IA Post-Hearing Br. 104.

patent need not be invalid or unenforceable for other reasons in order for it to be unenforceable for spoliation. Such an argument would make the remedy for spoliation superfluous. It was Rambus's burden to demonstrate that the materials destroyed did not include prior art, documents that would have been reasonably likely to lead to the discovery of prior art, and documents that could have assisted the respondents' arguments based on RamLink or SyncLink. We find that Rambus has not met its burden. Accordingly, we affirm the ALJ's determination that Rambus failed to show lack of prejudice for the reasons in the ID, and the supplemental discussion above. ID at 312-14.

Rambus also challenges the ALJ's finding that there were no lesser sanctions short of unenforceability that would have been appropriate under the circumstances.[25] Rambus Pet. 92-95; *see* Rambus Post-Hearing Br. 175-79. We agree with the ALJ that finding the Barth patents unenforceable is the most appropriate sanction, and that lesser sanctions would not suffice. ID at 314-17.

G. Patent Exhaustion

The ALJ found the Barth patents exhausted as to certain Garmin products, but not as to certain Cisco products. ID at 335-39. *See generally Quanta Computer, Inc. v. LG Electronics, Inc.*, 128 S. Ct. 2109, 2113 (2008); *Fujifilm Corp. v. Benun*, 605 F.3d 1366, 1368 (Fed. Cir. 2010). On petition, Rambus challenges the finding as to Garmin. Rambus

[25] Rambus suggested that monetary sanctions would be appropriate. Rambus Post-Hearing Br. 178. But Rambus never argued that such penalties are within the Commission's authority to award, and even if they were they fail to account for the conduct here. *See id.* (citing cases for post-complaint document destruction and awarding attorneys fees to compensate for the increased burdens caused by the document destruction). Rambus also suggested an "adverse inference instruction," *id.* at 179, which the ALJ appropriately rejected, ID at 317.

Pet. 98-99. The respondents have not petitioned for review of the ALJ's adverse findings as to Cisco, the respondents have waived or conceded their arguments as to Cisco's incorporation of certain licensed memory products. We have determined to affirm the ALJ's findings with respect to exhaustion by the Garmin products. *Id.* at 335-39.

H. Standing

The ALJ found that Rambus has standing to enforce the Dally patents.[26] ID at 326-30. Upon review, the Commission affirms the ALJ's conclusion that Rambus has standing, but for different reasons than those set forth in the ID. The Commission finds that Rambus has standing as a *bona fide* purchaser of the Dally patents.

The respondents argued that the University of North Carolina ("UNC"), and not the Massachusetts Institute of Technology ("MIT"), was the original assignee of the Dally patents by virtue of a sublicense between MIT and UNC. Rambus acquired its rights in the Dally patents indirectly from MIT. If MIT never owned the patents, then the respondents contend that Rambus owns nothing. The ALJ found that MIT, and not UNC, owned the rights to the Dally patents. ID at 326-30. The Commission notice requested further briefing on two subsidiary issues: (1) If the MIT-UNC contract gave UNC the rights to the Dally

[26] To assert a patent at the Commission, the complainant must own the patent or hold certain exclusive rights thereto. *See Certain Point of Sale Terminals*, Inv. No. 337-TA-524, Order No. 31 (February 7, 2005). The Commission's rules require complainants to demonstrate standing upon filing of the complaint by "showing that at least one complainant is the owner or exclusive licensee of the subject intellectual property." 19 C.F.R. § 210.12(a)(7). In addition, complainants must provide a certified copy of the assignments of each patent as well as a copy of any license agreement relied upon to establish standing to bring the complaint. *See* 19 C.F.R. § 210.12(a)(9)(ii)-(iv). While respondents may raise standing as a defense in their answer to the complaint, the question of whether a party lacks standing can be raised *sua sponte* and cannot be waived. *Pandrol USA, LP v. Airboss Ry. Prods., Inc.*, 320 F.3d 1354, 1368 (Fed. Cir. 2003).

patents, whether Rambus was nonetheless a *bona fide* purchaser under 35 U.S.C. § 261 because UNC never registered its assignment with the P.T.O. (2) Whether UNC's claim of ownership is barred by laches. 77 *Fed. Reg.* at 27250. Because the ALJ found that UNC never had any rights, he did not reach these issues. ID at 328-30. Thus, there are three issues on review, whether UNC had rights, and if so the two issues raised in the Commission notice.

1. The MIT-UNC Contract

Dr. William Dally was a professor at MIT at the time the original Dally patent application was filed in 1997. ID at 327. Dr. Dally's work arose from a contract between the Defense Advanced Research Projects Agency and Dr. Dally/MIT. ID at 327. MIT subsequently entered into a subcontract with UNC naming Dr. John Poulton of UNC as Key Personnel. *Id.*

The respondents alleged that this subcontract between MIT and UNC vested certain rights in UNC, rather than MIT. They further alleged that in view of these rights MIT lacked the authority to transfer its rights (eventually) to Rambus. ID at 327. The key provision is Article 10 of the subcontract between MIT and UNC:

> All rights, title and interests to all inventions, copyrightable materials, computer software, semiconductor maskworks, tangible research property and trademarks ("Intellectual Property") conceived, invented, authorized or reduced to practice, either solely or jointly with others which are developed under this subcontract in the course of or pursuant to sponsored research shall vest in [UNC].

RX-2023C.0007-08. The respondents argued that the Dally invention was developed with UNC's help, and that UNC obtained the intellectual property rights pursuant to this provision.

The IA argued that regardless of the ownership dispute, Rambus, as a *bona fide* purchaser of exclusive license rights, maintained ownership under 35 U.S.C. § 261 ("An assignment, grant, or conveyance shall be void as against any subsequent purchaser or mortgagee for a valuable consideration, without notice, unless it is recorded in the Patent and Trademark Office within three months from its date or prior to the date of such subsequent purchase or mortgage."). *See* IA Pet. 8-11.

The ALJ construed Article 10's "which" clause as modifying "Intellectual Property." ID at 328. Accordingly, he read the subcontract to provide that if the Intellectual Property was "developed under this subcontract" that UNC obtained rights, and if not, UNC didn't. "Development," in the ALJ's view, is a threshold that is satisfied when (a vague and unspecified) amount of work has been performed in connection with an invention: "the plain language of Article 10 includes a separate requirement that the intellectual property covered by this clause must be developed under the subcontract distinct from the other activities." ID at 328. As applied to the facts of this investigation, the ALJ found that the Dally Intellectual Property had already been developed prior to the UNC subcontract because at the time of the subcontract Dally had already established a proof of concept and "had simulations showing that the idea would work." *Id.* at 328. Because "development" is a "separate requirement," the ALJ found it immaterial that the actual reduction to practice of Dally's invention occurred in conjunction with Dr. Poulton under the terms of the subcontract. ID at 328-29.

On petition, the respondents challenged the ALJ's construction of the agreement. Resp'ts Pet. 38-41. They argued that the ALJ's imposition of an independent "development" requirement, distinct from the other activities is nonsensical. The IA repeats his argument that it does not matter in view of Rambus being a *bona fide* purchaser.

There is no dispute that the term "which" modifies Intellectual Property; this is true even under the ALJ's construction. Once that is recognized, it is too strained a reading of the agreement to impose a separate and undefined requirement for "developed."

We are not aware of any basis for such a separate definition for "developed." Webster's Third New International Dictionary defines the process of "development" as follows: "the act, process, or result of developing : the state of being developed : a gradual unfolding by which something (as a plan or method . . .) is developed: gradual advance or growth through progressive changes: EVOLUTION." Webster's Third New Int'l Dictionary 618 (1981); *accord id.* (definition of "develop"). Other dictionaries are to the same effect. Shorter Oxford English Dictionary 666 (6th ed. 2007) (defining "develop" and "development"); Webster's New World Dictionary 376 (3d college ed. 1988).

Even in the field of contracting, and particularly government contracting, "development" was, and is, a term with broad meaning. The Federal Acquisition Regulation in place at the time of the subject agreement read in pertinent part:

> "*Development*," as used in this subsection, means the systematic use, under whatever name, of scientific and technical knowledge in the design, development, test, or evaluation of a potential new product or service (or of an improvement in an existing product or service) for the purpose of meeting specific performance requirements or objectives. Development includes the functions of design engineering, prototyping, and engineering testing. Development excludes:
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> (1) Subcontracted technical effort which is for the sole purpose of developing an additional source for an existing product; or
>
> (2) development effort for manufacturing or production materials, systems, processes, methods, equipment, tools, and techniques not intended for sale.

Notice, 57 *Fed. Reg.* 44264, 44265-66 (Sept. 24, 1992) (amending FAR 31.205-18, codified at 48 C.F.R. § 205-18).[27] This definition is fully consistent with the evidence of record: UNC's witness explained that "developed under" was a generic term "inclusive of the activities that are described earlier." Tr. 2100.

Rambus has characterized the respondents' argument – with which we agree – as "suggest[ing] that 'development' must include a reduction to practice." Rambus Pet. Reply 8. This is incorrect. The respondents' argument is that development *can* include a reduction to practice. Because development occurred or continued at UNC, the subcontract vests UNC with the patent rights.

Rambus also asserts that it was proper for the ALJ to consider UNC's and MIT's after-the-fact conduct. Rambus Pet. Reply 9-11. We disagree. The terms of the agreement are not ambiguous, and no one at UNC with authority over its contract or patent rights was aware of the Dally patents, *see* Resp'ts Pet. 41-42, Tr. 2106-07, 2150-51.

2. Rambus Is a *Bona Fide* Purchaser

Because we conclude that MIT assigned its rights in the Dally patents to UNC, we turn to 35 U.S.C. § 261. In pertinent part, that section provides: "An assignment, grant, or conveyance shall be void as against any subsequent purchaser or mortgagee for a valuable consideration, without notice, unless it is recorded in the Patent and Trademark Office within three months from its date or prior to the date of such subsequent purchase or mortgage." The MIT-UNC sublicense was not recorded, and the parties appear to agree that Rambus

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[27] The Commission may take notice of the FAR definition, which is a promulgated regulation. 44 U.S.C. § 1507. The definition has not since changed. FAR 31.205-18 (48 C.F.R. § 31.205-18 (2012)), *available at* http://ecfr.gpoaccess.gov/cgi/t/text/text-idx?c=ecfr&rgn=div5&view=text&node=48:1.0.1.5.30&idno=48 (last visited July 24, 2012).

lacked actual notice of the sublicense. "Notice" under section 261, however, "can include constructive or inquiry notice, in addition to actual notice." *Board of Trustees of Leland Stanford Jr. Univ. v. Roche Molecular Sys., Inc.*, 583 F.3d 832, 843 (Fed. Cir. 2009). The respondents have contended that "Rambus was at least on inquiry notice of UNC's rights," and any "reasonably diligent investigation into the Dally patents would have uncovered" the UNC subcontract. Resp'ts Reply Pet. 98. Inquiry notice is "notice or information of circumstances to put a reasonable person on inquiry." *Jolly v. Eli Lilly & Co.*, 751 P.2d 923, 927-28 (Cal. 1988); *see also Merck & Co. v. Reynolds*, 130 S. Ct. 1784, 1797 (2010) (standard in securities-fraud cases).

The Commission's notice of review asked the parties to provide further briefing of this issue. The respondents argue as follows:

> Rambus had ample notice of UNC's involvement in developing the Dally technology and could easily have investigated the extent to which UNC had rights in that technology. For example, Dally's 1996 Invention Disclosure Form refers to work done at UNC. Dally also swore repeatedly to the PTO in publicly available filings that documentation from the Fast Links Project, on which Dally collaborated with UNC Professor John Poulton, corroborated conception of his claimed inventions. Rambus could have thus learned that the Dally patents were reduced to practice at UNC pursuant to the DARPA grant . . . . Given the commonplace nature of assignment provisions in high-tech collaborations, Rambus should have asked what interest UNC had in the Dally patents, just as Respondents did in connection with this case.
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> Rambus also could have learned about the UNC assignment if it had followed up on repeated references to the DARPA contract in connection with the Dally patents. . . . Rambus could have learned about the UNC contract, with its automatic assignment provision, by investigating the research that Dally and Poulton repeatedly stated was the source of the Dally Patents.

Resp'ts Br. 97-98. Rambus and the IA disagree. Rambus Br. 94-97; Rambus Reply Br. 58-59; IA Br. 80-86; IA reply Br. 47-49.

Although MIT's and UNC's post-sublicense conduct cannot change the plain meaning of the terms of the sublicense, that conduct is highly relevant to determining the reasonableness of Rambus's investigation into the Dally patent. Even in this investigation, UNC's representative did not assert ownership. Tr. 2116, 2137-39. Indeed, although Rambus could have become aware of Dr. Poulton's participation in the Fast Links-project funded by DARPA, the record does not show any hint to Rambus of UNC's ownership claim. Knowledge of the DARPA contract did not put Rambus on notice that UNC – as opposed to the U.S. government – may possess rights to the Dally patents. UNC, much less the UNC-MIT agreement (which had yet to exist), is not referred to in the DARPA contract. At best, Rambus could have discovered that Dr. Poulton was potentially an unnamed inventor of the Dally patents. Tr. 1696-97. But even if Rambus should have spoken with Poulton about inventorship, Rambus would have learned nothing about ownership, since Poulton believed that UNC had no ownership in the Dally patents. Tr. 1747-48, 1779. The respondents' argument is based on speculation: "Given the commonplace nature of assignment provisions in high-tech collaborations, Rambus should have asked what interest UNC had in the Dally patents . . . ." Resp. Br. 97. We do not believe that is enough. We find that Rambus was not on inquiry notice of UNC's ownership claim, and accordingly find that Rambus is a *bona fide* purchaser protected by 35 U.S.C. § 261.

In their briefs, the respondents argue that the bona fide purchaser defense cannot defeat a standing challenge. Resp'ts Br. 98-99 ; Resp'ts Reply Br. 59-60. They cite a recent district court decision that squarely held that the *bona fide* purchaser provision of 35 U.S.C. § 261 is only an affirmative defense that prevents the *bona fide* purchaser from being accused of infringement by a senior rightsholder. *StemCells, Inc. v. Neuralstem, Inc.*, No. 8:06-cv-

01877-AW, 2012 WL 1184545, at *15 (Apr. 6, 2012). The *StemCells* court recognized that the pertinent portion of section 261 was enacted in 1870, and looked to the common law (apparently non-patent-related) at that point to determine the scope of the rights afforded to a *bona fide* purchaser. The district court held that section 261 cannot cure a lack of legal title. *Id.* at *13.

We disagree with the district court's analysis. Section 261 is not limited to the common law understanding of *bona fide* purchasers of personal property. The Federal Circuit, in *FilmTec Corp. v. Allied-Signal Inc.*, 939 F.2d 1568 (Fed. Cir. 1991) (*FilmTec I*), concluded that although section 261 "does not expressly say, it is clear that the statute is intended to cut off prior *legal* interests, which the common law rule did not." *Id.* at 1573 (emphasis in original). This is inconsistent with *StemCell*'s holding that "the bona fide purchaser defense is only a shield by which the purchaser of a legal title may protect himself against the holder of an equity, not a sword by which the owner of an equity may overcome the holder of both the legal title and an equity." *StemCells*, 2012 WL 1184545, at *14 (quotation omitted). The *StemCells* court never cites or discusses *FilmTec I.*

The respondents' argument is that legal title vested in the University of North Carolina, and that Rambus cannot take that away. *FilmTec* rules to the contrary and the respondents do not adequately distinguish it. Instead, they rely on *Filmtec I*'s subsequent history, but the subsequent cases did not deal with section 261 and are inapposite. *See FilmTec Corp. v. Hydranautics*, 982 F.2d 1546, 1553 (Fed. Cir. 1992) (*FilmTec II*) (applying the Saline Water Conservation Act of 1971); *FilmTec Corp. v. Allied Signal, Inc.*, 988 F.2d 129 (Fed. Cir. Jan. 7, 1993) (Table), *available at* 1993 WL 2309 (*FilmTec III*) (applying the

holding of *FilmTec II*). In view of *FilmTec I*, therefore, we conclude that Rambus has demonstrated standing.

In our notice of review, we also asked the parties to provide further briefing whether UNC's delay in asserting ownership of the Dally patents constitutes laches that interferes with their claim of ownership. Because we find that Rambus is a *bona fide* purchaser under section 261, the laches issue is moot.[28]

I. Remaining Issues in the ID

We turn our attention to a number of smaller issues raised in the parties' petitions.

1. Importation of Products by STMicro

There are two remaining STMicro companies, the Dutch parent whose principal place of business is Geneva, Switzerland ("STMicro-NV"), and its wholly-owned U.S. subsidiary. The respondents petition the ALJ's determination on the basis that STMicro-NV does not import, sell for importation, or sell after importation any of the accused products, and that it should not be subject to an exclusion order. Resp'ts Pet. 66. Rambus opposes the petition on the basis that any remedial orders should also extend to the parent. Rambus Reply Pet. 66-67. Both Rambus and the IA recognize that Commission remedial orders ordinarily encompass parent corporations. *Id.* at 67; IA Reply Pet. 95-96. Accordingly, they argue that the STMicro argument is illusory. We agree and affirm the ALJ's determination.

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[28] In any event, however, laches is an affirmative defense that – unlike section 261 – cannot be used to prove standing. *Board of Trustees of Leland Stanford Jr. Univ. v. Roche Molecular Sys., Inc.*, 583 F.3d 832, 841 (Fed. Cir. 2009) ("*Roche*"), *aff'd on other grounds*, 131 S. Ct. 2188 (2011); *see* Resp'ts Br. 99-100; IA Br. 86.

2. Challenges to Certain ALJ Evidentiary Determinations

Rambus contends that the ALJ should not have excluded certain expert testimony (Dr. Singer) regarding the Widmer prior art, pertinent to the Dally patents. Rambus Pet. 10 n.4. We affirm the ALJ's determination.

The respondents allege that the ALJ should have allowed certain prior art witnesses to testify regarding LSI SL500 prior art, pertinent to the Dally patents. Resp'ts Pet. 51-56. The respondents contend that the testimony of these inventors would have corroborated LSI's invention of the equalization circuitry in the SL500 products. *Id.* at 51. The ALJ granted Rambus's motion *in limine* to exclude the witnesses on the basis that they were not adequately identified in the respondents' pretrial disclosures. The IA defends the ALJ's determination that the respondents' witness list did not provide sufficient guidance as to which witnesses the respondents would actually bring to trial, and the respondents' failure to identify their basis for calling the witnesses until after the discovery period closed. IA Reply Pet. 88-89. We affirm the ALJ's determination.

The respondents also allege that the ALJ erred in finding their reliance on the Lau and Nakamura patents for invalidity to have been waived. *See* U.S. Patent No. 5,541,957 (Lau); U.S. Patent No. 3,806,807 (Nakamura). ID at 224-25. The ALJ found that the respondents waived reliance on the Lau and Nakamura patents because they failed to include adequate argument in support of them in the post-hearing brief, pursuant to the ALJ's ground rules. ID at 24, 224-25. In particular, although the respondents discussed Nakamura and Lau in their post-hearing brief, Resp'ts Post-Hearing Br. 189-200, they purported to "focus only on contested aspects" of Lau and Nakamura, Resp'ts Pet. 57, instead of making affirmative demonstrations of how each and every limitation of the asserted patents is practiced in the

prior art combinations that included Lau or Nakamura, as is their burden in demonstrating invalidity. The result of the respondents' "focus" is a confusing discussion, where the opening brief discusses Rambus counterarguments that had yet to have been made in the post-hearing briefs. We find that the ALJ did not abuse his discretion in the application of his ground rules. We further note that the respondents' opening post-hearing brief was 300 pages long, and notwithstanding the fact that two patent families were asserted, the ALJ's page limitations were generous. Accordingly, we agree with the ALJ that the respondents' reliance on the Lau and Nakamura references has been waived.

3. Rambus's Expert Dr. Przybylski

Rambus requests that the Commission vacate the ALJ's discussion of the credibility of Rambus's technical expert Dr. Przybylski. Rambus Pet. 79-81 (citing ID at 305-09). In that portion of the ID, the ALJ found that Dr. Przybylski's testimony was frequently evasive, and that he gave it no weight. In making our determinations, *supra*, we have independently concluded that Dr. Przybylski's testimony is entitled to little weight. As we noted in connection with Dr. Singer's testimony, experts complicit in a client's overly aggressive positions run the risk of losing their own credibility. That is what happened here. Although the ALJ placed the discussion of Dr. Przybylski's testimony in his discussion of bad faith, we have not found his testimony to be pertinent to our determination to find the Barth patents unenforceable.

IV. CONCLUSION

The Commission determined to review the ID and on review affirms the ALJ's finding of no violation of section 337 for the following reasons: We affirm the ALJ's conclusion that all of the asserted patent claims are invalid under 35 U.S.C. § 102 or 103,

except for the asserted Dally '857 patent's multiple-transmitter claims ('857 claims 11-13, 32-34, 50-52), for which we find that Rambus has not demonstrated infringement. We reverse the ALJ's determination that Rambus has demonstrated the existence of a domestic industry under 19 U.S.C. § 1337(a) for both the Barth patents and Dally patents. We affirm the ALJ's determination that the Barth patents are unenforceable under the doctrine of unclean hands. We affirm the ALJ's finding of exhaustion of the Barth patents as to one respondent. Accordingly, the Commission has terminated this investigation with a finding of no violation of section 337.

By order of the Commission.

Lisa R. Barton
Acting Secretary to the Commission

Issued: August 17, 2012

CERTAIN SEMICONDUCTOR CHIPS AND PRODUCTS CONTAINING SAME **Inv. No. 337-TA-753**

PUBLIC CERTIFICATE OF SERVICE

I, Lisa R. Barton, hereby certify that the attached **ORDER** has been served by hand upon, the Commission Investigative Attorney, Daniel L. Girdwood, Esq., and the following parties as indicated on **August 17, 2012.**

Lisa R. Barton, Acting Secretary
U.S. International Trade Commission
500 E Street, SW, Room 112
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PUBLIC VERSION

UNITED STATES INTERNATIONAL TRADE COMMISSION
Washington, D.C.

In the Matter of	
CERTAIN SEMICONDUCTOR CHIPS AND PRODUCTS CONTAINING SAME	**Investigation No. 337-TA-753**

INITIAL DETERMINATION ON VIOLATION OF SECTION 337 AND RECOMMENDED DETERMINATION ON REMEDY AND BOND

Administrative Law Judge Theodore R. Essex

(March 2, 2012)

Appearances:

For the Complainant Rambus, Inc.:

J. Michael Jakes, Esq.; Doris Johnson Hines, Esq.; Christine E. Lehman, Esq.; Naveen Modi, Esq.; Luke J. Mccammon, Esq.; James Sherwood, Esq.; Kathleen Daley, Esq. of Finnegan, Henderson, Farabow, Garrett & Dunner, LLP of Washington, D.C..

For the Respondents Broadcom Corp.; MediaTek, Inc.; NVIDIA Corp.; STMicroelectronics N.V.; STMicroelectronics Inc.; Cisco Systems, Inc., Motorola Mobility, Inc.; Oppo Digital, Inc.; and Audio Partnership Plc.:

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Thomas D. Pease, Esq. of Quinn Emanuel Urquhart & Sullivan LLP of New York, New York

Paul F. Brinkman, Esq. of Quinn Emanuel Urquhart & Sullivan LLP of Washington, D.C.

Robert J. Becher, Esq. and William C. Price, Esq. of Quinn Emanuel Urqhart & Sullivan LLP of Los Angeles, California

For the Respondents Broadcom Corp. and Mediatek Inc.:

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David E. Sipiora, Esq. and Daniel S. Young, Esq. of Kilpatrick Townsend & Stockton LLP of Denver, Colorado

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Michael J. Abernathy, Esq. and Sanjay Murthy, Esq. of K&L Gates LLP of Chicago, Illinois

Eric Rusnak, Esq. of K&L Gates LLP of Washington, D.C.

For Respondents ASUSTek Computer, Inc.; Asus Computer International, Inc.; Biostar Microtech (U. S.A.) Corporation; Biostar Microtech International Corporation; EliteGroup Computer Systems Co., Ltd.; EVGA Corporation; Galaxy Microsystems, Ltd.; Giga¬Byte Technology Co., Ltd; G.B.T., Inc.; Hewlett- Packard Company; Jaton Corporation; Jaton Technology TPE; Micro-Star International Co., Ltd.; MSI Computer Corporation; Gracom Technologies LLC; Palit Microsystems, Ltd.; Pine Technology Holdings, Ltd.; Sparkle Computer Co., Ltd.; Zotac USA, Inc.; Zotac International (MCO), Ltd.:

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For Respondent Hitachi Global Storage Technologies, Inc.:

Alexander J. Hadjis, Esq. of Morrison & Foerster LLP of Washington, DC

For Respondent Garmin International Inc.:

Louis S. Mastriani, Esq., Sarah E. Hamblin, Esq. and Daniel F. Smith, Esq. of Adduci, Mastriani & Schaumberg, L.L.P. of Washington, DC

For the Commission Investigative Staff:
Lynn I. Levine, Esq., Director; T. Spence Chubb, Esq., Supervising Attorney; Daniel L. Girwood, Esq., Investigative Attorney of the Office of Unfair Import Investigations, U.S. International Trade Commission, of Washington, D.C.

Pursuant to the Notice of Investigation, 76 Fed. Reg. 384 (2010), this is the Initial Determination of the in the matter of *Certain Semiconductor Chips And Products Containing Same*, United States International Trade Commission Investigation No. 337-TA-753. *See* 19 C.F.R. § 210.42(a).

It is held that no violation of section 337 of the Tariff Act of 1930, as amended, 19 U.S.C. § 1337, has occurred in the importation into the United States, the sale for importation, or the sale within the United States after importation of certain semiconductor chips and products containing same by reason of infringement of one or more of claims 11-13, 15, and 18 of U.S. Patent No. 6,470,405, claims 11-13 of U.S. Patent No. 6,591,353, claims 1-6, 11- 13, 20-22, and 24 of U.S. Patent No. 7,287,109, claims 1, 2, 4-6, 9-13, 24-28, 31-36, 39-44, 47 and 49-53 of U.S. Patent No. 7,602,857 and claims 1-3, 6, 8, 25, 26, 30, 39, 40 and 42 of U.S. Patent No. 7,715,494.

TABLE OF CONTENTS

The following abbreviations may be used in this Initial Determination:

CDX	Complainants' demonstrative exhibit
CFF	Complainants' proposed findings of fact
CIB	Complainants' initial post-hearing brief
CORFF	Complainants' objections to Respondents' proposed findings of fact
COSFF	Complainants' objections to Staff's proposed findings of fact
CPX	Complainants' physical exhibit
CRB	Complainants' reply post-hearing brief
CX	Complainants' exhibit
Dep.	Deposition
JSUF	Joint Statement of Undisputed Facts
JX	Joint Exhibit
RDX	Respondents' demonstrative exhibit
RFF	Respondents' proposed findings of fact
RIB	Respondents' initial post-hearing brief
ROCFF	Respondents' objections to Complainants' proposed findings of fact
ROSFF	Respondents' objections to Staff's proposed findings of fact
RPX	Respondents' physical exhibit
RRB	Respondents' reply post-hearing brief
RRX	Respondents' rebuttal exhibit
RX	Respondents' exhibit
SFF	Staff's proposed findings of fact
SIB	Staff's initial post-hearing brief
SOCFF	Staff's objections to Complainants' proposed findings of fact
SORFF	Staff's objections to Respondents' proposed findings of fact
SRB	Staff's reply post-hearing brief
Tr.	Transcript

I. BACKGROUND

A. Institution and Procedural History of This Investigation

By publication of a notice in the *Federal Register* on January 4, 2010, pursuant to subsection (b) of section 337 of the Tariff Act of 1930, as amended, the Commission instituted Investigation No. 337-TA-753 with respect to U.S. Patent Nos. 6,470,405; 6,591,353; 7,287,109; 7,602,857; 7,602,858; and 7,715,494[1] to determine:

> [W]hether there is a violation of subsection (a)(1)(B) of section 337 in the importation into the United States, the sale for importation, or the sale within the United States after importation of certain semiconductor chips and products containing same that infringe one or more of claims 11–13, 15, and 18 of the '405 patent; claims 11–13 of the '353 patent; claims 1, 2, 4, 5, 12, 13, 20, 21, and 24 of the '109 patent; claims 1, 2, 4–6, 9–13, 24–28, 31–36, 39–44, 47, and 49–53 of the '857 patent; claims 1, 2, 4, 7, and 20 of the '858 patent; and claims 1–3, 6, 8, 25, 26, 30, 39, 40, and 42 of the '494 patent, and whether an industry in the United States exists as required by subsection (a)(2) of section 337.

76 Fed. Reg. 384 (2010).

Rambus, Inc. ("Rambus") of Los Altos, California is the complainant. (*Id.*) The respondents named in the Notice of Investigation were: Freescale Semiconductor, Inc. of Austin, Texas ("Freescale"); Broadcom Corporation of Irvine, California; LSI Corporation of Milpitas, California; MediaTek, Inc. of Hsin-Chu, Taiwan; nVidia Corporation of Santa Clara, California; STMicroelectronics NV of Geneva, Switzerland; STMicroelectronics Inc. of Carrollton, Texas (all collectively "Supplier Respondents"); Asustek Computer, Inc. of Taipei City, Taiwan; Asus Computer International Inc. of Fremont, California; Audio Partnership PLC, of London, United Kingdom; Biostar Microtech (USA) Corp. of City of Industry, California; Biostar Microtech International Corp of Hsin Tien, Taiwan; Cisco Systems, Inc. of San Jose, California; Elitegroup

[1] U.S. Patent Nos. 6,470,405, 6,591,353, 7,287,109 are collectively referred to as "the Barth I Patents" or "the Barth Patents." U.S. Patent Nos. 7,602,857 and 7,715,494 are collectively referred to as "the Dally Patents."

Computer Systems of Taipei, Taiwan; EVGA Corporation of Brea, California; Galaxy Microsystems, Ltd. of Kowloon Bay, Hong Kong; Garmin International of Olathe, Kansas; GBT Inc. of City of Industry, California; Giga-Byte Technology Co., Ltd. of Taipei, Taiwan; Gracom Technologies LLC of City of Industry, California; Hewlett-Packard Company of Palo Alto, California; Hitachi Global Storage Technologies of San Jose, California; Jaton Corporation of Fremont, California; Jaton Technology TPE of His-Chih, Taiwan; Micro-Star International Co, Ltd. of Taipei Hsien, Taiwan; MSI Computer Corporation of City of Industry, California; Motorola, Inc. of Schaumburg, Illinois; Oppo Digital, Inc. of Mountain View, California; Palit Microsystems Ltd. of Taipei, Taiwan; Pine Technology Holdings, Ltd. of North Point, Hong Kong; Seagate Technology of Scotts Valley, California; Sparkle Computer Co., Ltd. of Taipei County, Taiwan; Zotac International (MCO) Ltd. of Shatin, N.T. Hong Kong; and Zotac USA Inc. of City of Industry, California (all collectively "Customer Respondents"). (*Id.*) The Commission Investigative Staff ("Staff") of the Commission's Office of Unfair Import Investigations is also a party in this investigation. (*Id.*)

On June 20, 2011, the ALJ issued an order terminating Freescale from the investigation on the basis of settlement agreement. *See* Order No. 26 (June 20, 2011). The Commission determined not to review the order. *See* Notice of Commission Determination not to Review an Initial Determination Terminating the Investigation as to Respondent Freescale Semiconductor, Inc. Based on Settlement Agreement (July 13, 2011).

On August 10, 2011, the ALJ issued an order terminating the '858 Patent from the investigation. *See* Order No. 42 (August 10, 2011). The Commission determined not to review the order. *See* Notice of Commission Determination not to Review Initial Determination Terminating the Investigation as to Certain Asserted Patent Claims (September 9, 2011).

The evidentiary hearing on the question of violation of section 337 commenced on October 11, 2011, and concluded on October 20, 2011. Rambus, Supplier and Customer Respondents, and Staff were represented at the hearing. (Tr., 10:17-14:1.)

On January 17, 2012, the ALJ issued an order terminating respondent Broadcom Corporation from the investigation on the basis of a settlement agreement.[2] *See* Order No. 60 (January 17, 2012.) The Commission determined not to review the order. *See* Notice Of Commission Decision Not To Review An Initial Determination Terminating A Respondent On The Basis Of A Settlement Agreement (February 7, 2012).

On February 22, 2012, the ALJ issued two orders: (1) an order terminating respondent NVIDIA Corporation from the investigation on the basis of a settlement agreement and (2) an order terminating NVIDIA customer respondents from the investigation on the basis of the aforementioned settlement agreement.[3] *See* Order Nos. 62 (February 22, 2012.) Those decisions are still pending before the Commission.

[2] The agreement also terminated the investigation as to certain Customer Respondent products that contain and/or incorporate Broadcom products. According to the motion to terminate, "[t]he Agreements do not, however, resolve any claims raised in Rambus's Complaint based on non-Broadcom products incorporated in any such products of Customer Respondents (regardless of whether the same Customer Respondent product also contains a Broadcom product that is now subject to the Agreements), or any other products of Customer Respondents where the infringement claim is not based on the presence of a Broadcom product." *Joint Motion to Terminate Investigation as to Respondent Broadcom Corporation, and Downstream Broadcom Products, on the Basis of Settlement Agreement*, Motion Docket No. 753-102, at 1, note 1.

[3] The NVIDIA customer respondents are Biostar Microtech Corp., Biostar Microtech International Corp., Elitegroup Computer System Co., Ltd., EVGA Corporation, Galaxy Microsystems, Ltd., Giga-Byte Tech. Co., Ltd., G.B.T., Inc., Jaton Corporation, Jaton Technology TPE, Micro-Star International Co., Ltd., MSI Computer Corp., Gracom Technologies LLC, Palit Microsystems, Ltd., Pine Technology Holdings, Ltd., Sparkle Computer Co., Ltd., Nala Sales, Inc. f/k/a Zotac USA, Inc., and Zotac International (MCO), Ltd.

B. The Parties

Rambus

Rambus is a Delaware corporation with a principal place of business in Los Altos, California. (Complaint, ¶18.)

LSI

Respondent LSI Corporation ("LSI") is a Delaware Corporation with a principal place of business in Milpitas, California. (LSI Corporation's Second Amended Response to Complaint Under Section 337 of the Tariff Act of 1930, as Amended, and to the Notice of Investigation, at ¶162 (Oct. 28, 2011).)

MediaTek

Respondent MediaTek Inc. ("MediaTek") is a Taiwanese corporation with a principal place of business in Hsin-Chu, Taiwan. (Amended Response of MediaTek Inc. to Complaint Under Section 337 of the Tariff Act of 1930, as Amended, and Notice of Investigation, at ¶208 (Oct. 20, 2011).)

STM

Respondent STMicroelectronics N.V. is a Netherlands corporation with a principal place of business in Geneva, Switzerland and respondent STMicroelectronics Inc. is a Delaware corporation (and an indirect wholly-owned subsidiary of STMicroelectronics N.V.) having a principal place of business in Carrollton, Texas (collectively "STM."). (Second Amended Response of STMicroelectronics Inc. and STMicroelectronics N.V. to Complaint Under Section 337 of the Tariff Act of 1930, as Amended, and Notice of Investigation, EDIS Doc. ID 462260 at ¶252 (Oct. 24, 2011).)

ASUS

Respondent ASUStek Computer Inc. is a Taiwanese corporation with a principal place of business in Taipei, Taiwan and respondent ASUS Computer International Inc. is a California corporation (and a wholly-owned subsidiary of ASUStek Computer Inc.) with a principal place of business in Fremont, California (collectively "ASUS"). (The ASUS Respondents' Response to Rambus Inc.'s Complaint and the Commission's Notice of Investigation, at ¶298 (Feb. 1, 2011).)

Audio Partnership

Respondent Audio Partnership PLC is a British corporation with a principal place of business in London, United Kingdom. (Amended Response of Audio Partnership PLC to Complaint Under Section 337 of the Tariff Act of 1930, as Amended, and Notice of Investigation, at ¶333 (Oct. 20, 2011).)

Cisco

Respondent Cisco Systems Inc. is a California corporation with a principal place of business in San Jose, California. (Amended Response of Cisco Systems Inc. to Complaint Under Section 337 of the Tariff Act of 1930, as Amended, and Notice of Investigation, at ¶374 (Oct. 20, 2011).)

Garmin

Respondent Garmin International, Inc. is a Kansas corporation with a principal place of business in Olathe, Kansas. (Amended Response to Complaint and Notice of Investigation by Respondent Garmin International Inc., at ¶482 (Oct. 21, 2011).)

HP

Respondent Hewlett Packard Company is a Delaware corporation with a principal place of business in Palo Alto, California. (Respondent Hewlett-Packard Company's Response to Rambus Inc.'s Complaint and the Commission's Notice of Investigation, at ¶523 (Feb. 1, 2011).)

Hitachi

Respondent Hitachi Global Storage Technologies Inc. is a Delaware corporation with a principal place of business in San Jose, California. (Amended Response of Respondent Hitachi Global Storage Technologies, Inc. to the Complaint and Notice of Investigation, at ¶562 (Oct. 26, 2011).)

Motorola

Respondent Motorola Mobility, Inc. is a Delaware corporation with a principal place of business in Libertyville, Illinois. (Amended Response of Motorola Mobility, Inc. to Complaint Under Section 337 of the Tariff Act of 1930, as Amended, and Notice of Investigation, at ¶642 (Oct. 20, 2011).)

Oppo Digital

Respondent Oppo Digital, Inc. is a California corporation with a principal place of business in Mountain View, California. (Amended Response of Oppo Digital, Inc. to Complaint Under Section 337 of the Tariff Act of 1930, as Amended, and Notice of Investigation, at ¶675 (Oct. 20, 2011).)

Seagate

Respondent Seagate Technology LLC is a Delaware corporation with a principal place of business in Scotts Valley, California. (Seagate Technology's Second Amended Response to

Complaint Under Section 337 of the Tariff Act of 1930, as Amended, and to the Notice of Investigation, at ¶739 (Oct. 28, 2011).)

C. The Patents at Issue and Overview of the Technology

The Barth Patents are generally directed at memory devices and their associated memory controllers as used, for example, in personal computers (PCs), gaming consoles, mobile devices, and the like. (Complaint, ¶¶23-25; CX-9543C, Przybylski Direct at Q&A 66.) This investigation is particularly focused on the memory controllers of consumer electronics that interface with memory devices compliant with industry standards promulgated by the Joint Electron Device Engineering Council ("JEDEC"). (CX-9543C, Przybylski Direct Q&A 40-42, 273, 280-296.) Implicated standards include JEDEC's Double Data Rate ("DDR") memory technology standards, such as JEDEC's DDR, DDR2, DDR3, Graphics DDR3 ("GDDR3"), Low Power DDR ("LPDDR") and LPDDR2 standards (collectively, the "Accused JEDEC Standards"). (CX-9543C, Przybylski Direct Q&A 38, 74.) The Accused JEDEC Standards specify the signaling associated with certain memory device operations, as well as certain physical characteristics of the interfaces for connecting a memory device to an associated memory controller. (CX-9543C, Przybylski Direct Q&A 39-42.)

The Dally patents are generally directed at the use of equalization techniques within transmitter circuits of PCs, gaming consoles, mobile devices and the like. (Complaint, ¶¶26-27; CX-9542C, Singer Direct at Q&A 40-53; Singer, Tr. 571:02-08.) This investigation are particularly focused on the transmitter circuitry of consumer electronics that are compliant with industry standards promulgated by various entities. (CX-9542C, Singer Direct at Q&A 54.) Implicated standards include PCI Express, DisplayPort, Serial Advanced Technology Attachment (SATA), and Serial Attached Small Computer System Interface (SAS) (collectively,

the "Accused Transmitter Standards"). (CX-9542C, Singer Direct at Q&A 54-74.) The Accused Transmitter Standards specify certain signaling parameters associated with various interfaces. (CX-9542C, Singer Direct Q&A 54-74.)

The Barth Patents

a) The '405 Patent

U.S. Patent No. 6,470,405 ("the '405 Patent"), entitled "Protocol for Communication With Dynamic Memory," was filed on May 29, 2001, and issued on October 22, 2002. (JX-3 (the '405 Patent)). Richard M. Barth, Fredrick A. Ware, John B. Dillon, Donald C. Stark, Craig E. Hampel, and Matthew M. Griffin are the named inventors of the '405 Patent, and complainant Rambus is the named assignee. (*Id.*)

The asserted claims of the '405 Patent are claims 11-13, 15, and 18. These claims read as follows:

> 11. A method of controlling a semiconductor memory device, wherein the memory device includes an array of memory cells, the method comprises: providing a plurality of control codes to the memory device wherein the plurality of control codes include a first code which specifies that a write operation be initiated in the memory device and a second code which specifies that a precharge operation be initiated automatically after initiation of the write operation; delaying for an amount of time after providing the plurality of control codes; and issuing an external strobe signal to the memory device after delaying for the amount of time, to signal the memory device to sample data, wherein the data is to be written to the array during the write operation.
>
> 12. The method of claim 11 further comprising issuing a first portion of the data and a second portion of the data to the memory device, wherein the first portion of the data is sampled during an odd phase of an external clock signal, and the second portion of the data is sampled during an even phase of the external clock signal.
>
> 13. The method of claim 12 wherein the first and second portions of the data are both issued during a first clock cycle of the external clock signal.
>
> 15. The method of claim 11 further comprising providing address information to the memory device.

18. The method of claim 11 wherein the plurality of control codes includes a third code which specifies that a row of sense amplifiers be activated.

The '405 patent generally discloses and claims a system and method for performing data transfers within a computer system. (*Id.*)

b) The '353 Patent

U.S. Patent No. 6,591,353 ("the '353 Patent"), entitled "Protocol for Communication With Dynamic Memory," was filed on May 1, 2000, and issued on July 8, 2003. (JX-4 (the '353 Patent)). Richard M. Barth, Fredrick A. Ware, John B. Dillon, Donald C. Stark, Craig E. Hampel, and Matthew M. Griffin are the named inventors of the '353 Patent, and complainant Rambus is the named assignee. (*Id.*)

The asserted claims of the '353 Patent are claims 11-13. These claims read as follows:

11. A method of controlling a memory device that includes a plurality of memory cells, the method comprising: issuing a first write command to the memory device, the memory device being configured to defer sampling data that corresponds to the first write command until a strobe signal is detected; delaying for a first time period after issuing the write command; and after delaying for the first time period, issuing the strobe signal to the memory device to initiate sampling of a first portion of the data by the memory device.

12. The method of claim 11, further comprising issuing the first portion of the data and a second portion of the data to the memory device, wherein the first portion of the data is sampled during an odd phase of an external clock signal, and the second portion of the data is sampled during an even phase of the external clock signal.

13. The method of claim 12, wherein the first and second portions of the data are both issued during a common clock cycle of the external clock signal.

The '353 Patent generally discloses and claims a method and apparatus for controlling data transfers to and from a dynamic random access memory. (*Id.*)

c) The '109 Patent

U.S. Patent No. 7,287,109 ("the '109 Patent"), entitled "Method Of Controlling A Memory Device Having A Memory Core," was filed on October 15, 2004, and issued on October 23, 2004. (JX-5 (the '109 Patent)). Richard M. Barth, Fredrick A. Ware, John B. Dillon, Donald C. Stark, Craig E. Hampel, and Matthew M. Griffin are the named inventors of the '109 Patent, and complainant Rambus is the named assignee. (*Id.*)

The asserted claims of the '109 Patent are claims 1, 2, 4, 5, 12, 13, 20, 21 and 24. These claims read as follows:

> 1. A method of controlling a memory device having a memory core, wherein the method comprises: providing control information to the memory device, wherein the control information includes a first code which specifies that a write operation be initiated in the memory device; providing a signal to the memory device, wherein the signal indicates when the memory device is to begin sampling write data, wherein the write data is stored in the memory core during the write operation; providing a first bit of the write data to the memory device during an even phase of a clock signal; and providing a second bit of the write data to the memory device during an odd phase of the clock signal.
>
> 2. The method of claim 1, wherein the control information further includes: address information that specifies a location in the memory core for the write operation; a second code that specifies whether to perform a sense operation; and a third code that specifies whether to perform a precharge operation.
>
> 4. The method of claim 1, wherein the memory core includes a plurality of banks, wherein each bank of the plurality of banks includes a memory cell array, wherein the method further includes: transmitting bank selection information to the memory device, wherein the bank selection information identifies a bank of the plurality of banks, wherein the write operation is initiated in a subset of the memory cell array included in the bank identified by the bank selection information; and transmitting address information to the memory device, wherein the address information identifies the subset of the memory cell array.
>
> 5. The method of claim 4, wherein the control information further includes a second code which specifies that a precharge operation be initiated in the bank identified by the bank selection information after the write data is written to the subset of the memory cell array.
>
> 12. A method of controlling a memory device, wherein the memory device includes a plurality of banks, wherein each bank of the plurality of banks includes

a memory cell array, wherein the method comprises: providing a plurality of operation codes to the memory device, wherein the plurality of operation codes includes a first code which specifies that a write operation be initiated in the memory device; providing bank selection information to the memory device, wherein the bank selection information identifies a bank of the plurality of banks, wherein the write operation is initiated in the memory cell array included in the bank identified by the bank selection information; providing address information to the memory device, wherein the address information identifies where to initiate the write operation in the memory cell array included in the bank identified by the bank selection information; providing a signal to the memory device, wherein the signal indicates when the memory device is to begin receiving write data to be written during the write operation; providing a first bit of the write data to the memory device during an even phase of a clock signal; and providing a second bit of the write data to the memory device during an odd phase of the clock signal.

13. The method of claim 12, wherein the plurality of operation codes further includes a second code which specifies that a precharge operation be initiated in the bank identified by the bank selection information after the write data is written during the write operation.

20. A method of controlling a memory device having a memory core, wherein the method comprises: providing control information to the memory device, wherein the control information includes a first code which specifies that a transfer operation be initiated with the memory device; providing a signal to the memory device, wherein the signal indicates when the memory device is to begin the transfer operation; and during the transfer operation, transferring a first bit of data during an even phase of a clock signal, and transferring a second bit of data during an odd phase of the clock signal.

21. The method of claim 20, wherein the control information further includes: address information that specifies a memory location of the data; and a second code that specifies whether to perform a sense operation, wherein the data is transferred from a row of the memory core to a plurality of sense amplifiers when a sense operation is performed.

24. The method of claim 20, wherein the transfer operation is a write operation.

The '109 Patent generally discloses and claims a method and apparatus for controlling data transfers to and from a dynamic random access memory. (*Id.*)

The Dally Patents

d) The '857 Patent

U.S. Patent No. 7,602,857 ("the '857 Patent"), entitled "Digital transmitter," was filed on August 31, 2006, and issued on October 13, 2009. (JX-122 (the '857 Patent)). William J. Dally is the named inventor of the '857Patent. (*Id.*)

The asserted claims of the '857 Patent are claims 1, 2, 4-6,9-13, 24-28, 31-36, 39-44, 47 and 49-53. These claims read as follows:

> 1. A component comprising: a semiconductor chip; a processor within the chip; and a transmitter circuit within the chip, the transmitter circuit being coupled to the processor to accept a digital input signal including a plurality of digital values from the processor, the transmitter circuit being operable to send an output signal including a series of signal levels representing the digital values and to emphasize high frequency components of the output signal relative to low frequency components of the output signal so that: (i) an output bit signal of the output signal representing a particular bit value has one signal level when the bit value is the same as a bit value represented by a predetermined preceding output bit signal; and (ii) the output bit signal representing the particular bit value has another signal level when the bit value is different from the bit value represented by the predetermined preceding output bit signal.
>
> 2. The component as claimed in claim 1 wherein the transmitter circuit is operable to send the output signal with an output frequency of at least 1 GHz and a bandwidth greater than 100 MHz.
>
> 4. The component as claimed in claim 1 wherein the transmitter circuit is operable to emphasize signal levels representing values following transitions between values relative to signal levels repre
> senting repeated values.
>
> 5. The component as claimed in claim 1 wherein the chip has I/O connections and the transmitter circuit is coupled to one or more of the I/O connections to send the output signal through the one or more I/O connections.
>
> 6. The component as claimed in claim 5 wherein the transmitter circuit is operable to send the output signal in nonmodulated form.
>
> 9. The component as claimed in claim 1 wherein each digital value is represented by one of the signal levels in the output signal.

10. The component as claimed in claim 1 wherein the digital input signal includes a plurality of bits and each bit of the digital input signal is represented by one of the signal levels in the output signal.

11. The component as claimed in claim 1 further comprising at least one additional transmitter circuit within the chip, each additional transmitter circuit being coupled to the processor and operable to accept an additional digital input signal from the processor and send an additional output signal representing such additional input signal.

12. The component as claimed in claim 11 wherein the chip has I/O connections and the transmitter circuits are coupled to a plurality of the I/O connections and operable to send the output signals through the I/O connections.

13. The component as claimed in claim 11 wherein the transmitter circuits are operable to provide output signals representing a parallel stream of data from the processor.

24. A component comprising: a semiconductor chip; a component circuit within the chip; and a transmitter circuit within the chip, the transmitter circuit being coupled to the component circuit to accept a digital input signal including a plurality of digital values from the component circuit, the transmitter circuit being operable to send an output signal including a series of signal levels representing the digital values and to emphasize high frequency components of the output signal relative to low frequency components of the output signal; wherein each digital value in the digital input signal is represented by one of the signal levels in the output signal and the transmitter circuit is operable to select each signal level as a function of the digital value represented by that signal level and of the digital values represented by one or more preceding signal levels.

25. The component as claimed in claim 24 wherein the component circuit is a processor.

26. The component as claimed in claim 24 wherein the transmitter circuit is operable to emphasize signal levels representing values following transitions between values relative to signal levels representing repeated values.

27. The component as claimed in claim 24 wherein the chip has I/O connections and the transmitter circuit is coupled to one or more of the I/O connections to send the output signal through the one or more I/O connections.

28. The component as claimed in claim 27 wherein the transmitter circuit is operable to send the output signal in nonmodulated form.

31. The component as claimed in claim 24 wherein the transmitter circuit is operable to send the output signal with an output frequency of at least 1 GHz and a bandwidth greater than 100 MHz.

32. The component as claimed in claim 24 further comprising at least one additional transmitter circuit within the chip, each additional transmitter circuit being coupled to the component circuit and operable to accept an additional digital input signal from the component circuit and send an additional output signal representing such additional input signal.

33. The component as claimed in claim 32 wherein the chip has I/O connections and the transmitter circuits are coupled to a plurality of the I/O connections and operable to send the output signals through the I/O connections.

34. The component as claimed in claim 33 wherein the transmitter circuits are operable to provide output signals representing a parallel stream of data from the component circuit.

35. A component comprising: a semiconductor chip; a component circuit within the chip; and a transmitter circuit within the chip, the transmitter circuit being coupled to the component circuit to accept a digital input signal including a plurality of digital values from the component circuit, the transmitter circuit being operable to send an output signal including a series of signal levels representing the digital values and to emphasize high frequency components of the output signal relative to low frequency components of the output signal; wherein each digital value in the digital input signal is represented by one of the signal levels in the output signal and the transmitter circuit is operable to select each signal level as a function of the digital value represented by that signal level and the digital value represented by the immediately preceding signal level.

36. The component as claimed in claim 35 wherein the component circuit is a processor.

39. A component comprising: a semiconductor chip; a component circuit within the chip; and a transmitter circuit within the chip, the transmitter circuit coupled to the component circuit and operable to accept a digital input signal including a plurality of bit values from the component circuit and send an output signal representing the digital input signal, the output signal including a series of output bit signals having signal levels so that: (i) an output bit signal of the output signal representing a particular bit value has one signal level when the bit value is the same as a bit value

represented by a predetermined preceding output bit signal; and (ii) the output bit signal representing the particular bit value has another signal level when the bit value is different from the bit value represented by the predetermined preceding output bit signal.

40. The component as claimed in claim 39 wherein the component circuit is a processor.

41. The component as claimed in claim 39 wherein the transmitter circuit is operable to select each signal level as a function of the bit value represented by that signal level and of the bit values represented by one or more preceding signal levels.

42. The component as claimed in claim 39 wherein the transmitter circuit is operable to select each signal level as a function of the bit value represented by that signal level and the bit value represented by the immediately preceding signal level.

43. The component as claimed in claim 39 wherein the chip has I/O connections and the transmitter circuit is coupled to one or more of the I/O connections to send the output signal through the one or more I/O connections.

44. The component as claimed in claim 43 wherein the transmitter circuit is operable to send the output signal in nonmodulated form.

47. The component as claimed in claim 39 wherein each bit value in the digital input signal is represented by one of the signal levels in the output signal.

49. The component as claimed in claim 39 wherein the transmitter circuit is operable to send the output signal with an output frequency of at least 1 GHz and a bandwidth greater than 100 MHz.

50. The component as claimed in claim 39 further comprising at least one additional transmitter circuit within the chip, each additional transmitter circuit being coupled to the component circuit and operable to accept an additional digital input signal from the component circuit and send an additional output signal representing such additional input signal.

51. The component as claimed in claim 50 wherein the chip has I/O connections and the transmitter circuits are coupled to a plurality of the I/O connections and operable to send the output signals through the I/O connections.

> 52. The component as claimed in claim 51 wherein the transmitter circuits are operable to provide output signals representing a parallel stream of data from the component circuit.
>
> 53. The component as claimed in claim 39 wherein the transmitter circuit is operable to select each signal level as a function of only the bit value represented by that signal level and the bit value represented by the immediately preceding signal level.

The '857 Patent is generally directed to an equalizer in a digital transmitter that compensates for attenuation in a signal channel to a digital receiver. (*Id.*)

e) The '494 Patent

U.S. Patent No. 7,715,494 ("the '494 Patent"), entitled "Digital transmitter," was filed on August 31, 2006, and issued on May 11, 2010. (JX-121 (the '494 Patent)). William J. Dally is the named inventor of the '494Patent. (*Id.*)

The asserted claims of the '494 Patent are claims 1-3, 6, 8, 25, 26, 30, 39, 40 and 42. These claims read as follows:

> 1. A circuit comprising: a semiconductor chip; a transmitter circuit within the chip, the transmitter circuit being operable to accept a digital input signal including a plurality of bits and send an output signal including a series of output bit signals, each bit of the digital input signal being represented by a single output bit signal, the transmitter circuit generating a sign which depends upon the value of the bit represented by such output bit signal and generating a magnitude which is a function of the value of the bit represented by such output bit signal and the values of the bits represented by one or more preceding output bit signals, each output bit signal having sign and magnitude determined by the generated sign and generated magnitude.
>
> 2. The circuit as claimed in claim 1 wherein the function is such that an output bit signal representing a bit having a value different from the value of the bits represented in the one or more preceding output bit signals has a greater magnitude than an output bit signal representing a bit having the same value as the bits represented by the one or more preceding output bit signals.
>
> 3. The circuit as claimed in claim 1 wherein the transmitter is operable to provide the output signal with an output frequency of at least 1 GHz and a bandwidth greater than 100 MHz.

6. The circuit as claimed in claim 1 wherein the transmitter circuit is operable to select the magnitude of each output bit signal based only on the value of the bit represented by that output bit signal and the value of the bit represented by the immediately preceding output bit signal.

8. The circuit as claimed in claim 1 wherein the function is reprogrammable.

25. A circuit comprising: a semiconductor chip; and a transmitter circuit within the chip, the transmitter circuit being operable to accept a digital input signal including a plurality of bits and send a differential output signal including a series of output bit signals, each bit of the digital input signal being represented by a single output bit signal; where the transmitter circuit drives the series of output bit signals to have sign represented by logic level of a first bit that is to be transmitted, and magnitude represented by whether the first bit represents a common logic level relative to an immediately previous bit, the magnitude being driven to be relatively smaller when the first bit has a common logic level with the immediately previous bit, and to be relatively larger when the first bit does not have the common logic level.

26. The circuit of claim 25, where the chip includes plural of said transmitter circuits, each transmitter circuit to output a respective series of output bit signals on lines of a parallel bus.

30. The circuit of claim 25, where the series of output signals is transmitted by the transmitter onto a signal path at a rate of at least 400 megahertz.

39. A method of operation in an integrated circuit having a transmitter, the method comprising: accepting a digital input signal including a plurality of bits and sending a differential output signal including a series of output bit signals, each bit of the digital input signal being represented by a single output bit signal; using the transmitter to drive the series of output bit signals to have sign represented by logic level of a first bit that is to be transmitted, and magnitude represented by whether the first bit represents a common logic level relative to an immediately previous bit, the magnitude being relatively smaller when the first bit has a common logic level with the immediately previous bit, and being relatively larger when the first bit does not have the common logic level.

40. The method of claim 39, where the integrated circuit includes plural of said transmitters, the method further comprising using each transmitter circuit to output a respective series of output bit signals on a respective line of a parallel bus.

42. The method of claim 39, further comprising driving the series of output signals using the transmitter onto a signal path at a rate of at least 400 megahertz.

The '494 Patent is generally directed to an equalizer in a digital transmitter that compensates for attenuation in a signal channel to a digital receiver. (*Id.*)

D. The Products At Issue

The accused products are memory controllers that are designed to interface with DDR, DDR2, DDR3, GDDR3, LPDDR or LPDDR2 compliant memory devices and products incorporating such a controller that infringe the Barth Patents ("the Accused Barth Products"). (Complaint, ¶¶122, 125, 129, 134, 139 (Broadcom accused products); *id.* at ¶¶166, 169, 172, 177, 182 (LSI accused products); *id.* at ¶¶212, 214, 217, 222 (MediaTek accused products); *id.* at ¶¶256, 259, 263, 268, 273 (STM accused products); CX-9543C, Przybylski Direct Q&A 75-90 (Broadcom accused products); *id.* at Q&A 91-113 (LSI accused products); *id.* at Q&A 114-132 (MediaTek accused products); *id.* at Q&A 133-162 (STM accused products); *id.* at Q&A 163-256 (accused downstream products); Stipulation Regarding Representative Broadcom Accused Products, at 2 (June 17, 2011) ("Broadcom Stip"); Smith, Tr. 896:10-897:01 (LSI accused products); *id.* at 898:15-899:02 (Seagate accused products); RX-5505C, Salem Rebuttal Q&A 12-16 (Broadcom accused products).)

The accused products also include interface chips that are designed according to PCI Express, DisplayPort, SATA, and SAS interface standards and products incorporating such an interface chip that infringe the Dally Patents ("the Accused Dally Products"). (Complaint at ¶¶123, 125, 146, 152, 158 (Broadcom accused products); *id.* at ¶¶167, 169, 189, 190, 196, 197, 203, 204 (LSI accused products); *id.* at ¶¶231, 233, 239, 244, 249 (nVidia accused products); *id.* at ¶¶257, 259, 280, 286, 292 (STM accused products); CX-9542C, Singer Direct Q&A 75-86 (Broadcom accused products); *id.* at Q&A 87-96 (LSI accused products); *id.* at Q&A 97-100 (nVidia accused products); *id.* at Q&A 101-104 (STM accused products); *id.* at Q&A 105-110

(downstream accused products); Singer, Tr. 753:25-755:12, 765:10-766:11 (LSI accused products); Ozguc, Tr. 1186:24-1187:05 (nVidia accused products); RX-6271C, Ozguc Rebuttal Q&A 19 (nVidia accused products); Singer, Tr. 674:19-25 (Cisco accused products).)

II. IMPORTATION OR SALE

The ALJ finds that the importation or sale requirement of section 337 has been satisfied. Rambus has entered into a series of stipulations with certain respondents. (CX-9027C, Garmin Stip at 1-3; Stipulation Between Rambus and Cisco Systems, Inc., EDIS Doc. ID 460973 at ¶3 (Oct. 5, 2011) ("Cisco Stip"); Stipulations Regarding ASUS, EDIS Doc. ID 460646 at 1 (Sept. 1, 2011) ("ASUS Stip"); Stipulations Regarding Micro-Star, EDIS Doc. ID 460655 at 1 (Sept. 12, 2011) ("MSI Stip"); Stipulations Regarding ECS, EDIS Doc. ID 460649 at 1 (Sept. 2, 2011) ("ECS Stip"); Stipulations Regarding Biostar, EDIS Doc. ID 460647 at 1 (Sept. 9, 2011) ("Biostar Stip"); Stipulations Regarding Galaxy, EDIS Doc. ID 460651 at 1 (Sept. 9, 2011) ("Galaxy Stip"); Stipulations Regarding Pine, EDIS Doc. ID 460658 at 1 (Sept. 22, 2011) ("Pine Stip"); Stipulations Regarding Sparkle, EDIS Doc. ID 460659 at 1 (July 13, 2011) ("Sparkle Stip"); Stipulations Regarding EVGA, EDIS Doc. ID 460650 at 1 (Sept. 16, 2011) ("EVGA Stip") Stipulations Regarding Gigabyte, EDIS Doc. ID 460652 at 1 (Sept. 12, 2011); Stipulations Regarding HP, EDIS Doc. ID 460653 at 1 (Sept. 27, 2011) ("HP Stip"); Stipulations Regarding Jaton, EDIS Doc. ID 460654 at 1 (Oct. 4, 2011) ("Jaton Stip"); Stipulations Regarding Palit, EDIS Doc. ID 460657at 1 (Sept. 16, 2011) ("Palit Stip"); Stipulations Regarding Zotac, EDIS Doc. ID 460660 at 1 (Sept. 13, 2011) ("Zotac Stip"); Stipulation Between Rambus and Motorola Mobility Inc., EDIS Doc. ID 459583 at ¶3 (Sept. 7, 2011) ("Motorola Stip"); Stipulations Regarding Respondent Hitachi Global Storage Technologies Inc., EDIS Doc. ID 454292 at 1 (July 12, 2011) ("Hitachi Stip").)

Respondents LSI, Seagate, and Oppo do not dispute that they import the accused products into the United States. (RIB at 16-19.) The evidence shows that the importation requirement for these respondents has been satisfied. (CX-7473C.0177-78 (LSI); CX-7274C.0074 (Oppo); JX-115C.00329-30 at 108-11 (Seagate).)

[redacted]

On December 2, 2011, the Commission issued its opinion in *Certain Electronic Devices with Image Processing Systems, Components Thereof, and Associated Software*, Inv. No. 337-TA-724 ("*Electronic Devices with Image Processing Systems*"), which was after completion of the post-hearing briefs in this investigation. In *Electronic Devices with Image Processing Systems*, the Commission stated that "the ALJ's importation analysis must include an evaluation

of whether the type of infringement alleged will support a finding that there has been an importation of an article that infringes in violation of section 337." *Certain Electronic Devices with Image Processing Systems, Components Thereof, and Associated Software*, Inv. No. 337-TA-724, Comm'n Op. at 13, note 8 (December 2, 2011). The Commission held that

> [S]ection 337(a)(1)(B)(i) covers imported articles that directly or indirectly infringe when it refers to "articles that – infringe." We also interpret the phrase "articles that – infringe" to reference the status of the articles at the time of importation. Thus, infringement, direct or indirect, must be based on the articles as imported to satisfy the requirements of section 337.

Id. at 13-14. The Commission further held that "[w]e analyze a violation of section 337(a)(1)(B)(i) based on method claim[s] [] under the statutory rubrics of indirect infringement." *Id.* at 18. In that investigation, the Commission held that the complainant failed to show importation, sale for importation, or sale after importation of articles that infringe a method claim directly or indirectly. *Id.* at 18-19.

Here, as set forth *supra* in Section I.D, the accused products are memory controllers designed to interface with DDR, DDR2, DDR3, GDDR3, LPDDR or LPDDR2 compliant memory devices and products incorporating such devices and interface chips that are designed according to PCI Express, DisplayPort, SATA and SAS interface standards and products incorporating such chips. Rambus has alleged that these accused products directly and indirectly infringe the asserted claims, which include apparatus and method claims, of the Barth and the Dally Patents. As set forth *infra* in Section IV, to the extent that the ALJ finds that Respondents' accused products directly or indirectly infringe the asserted claims of the Barth and the Dally Patents, the importation requirement has been satisfied.

III. JURISDICTION

A. Personal and Subject Matter Jurisdiction

In order to have the power to decide a case, a court or agency must have both subject matter jurisdiction and jurisdiction over either the parties or the property involved. *See Certain Steel Rod Treating Apparatus and Components Thereof*, Inv. No. 337-TA-97, Commission Memorandum Opinion, 215 U.S.P.Q. 229, 231 (1981). For the reasons discussed below, the ALJ finds the Commission has jurisdiction over this investigation.

Section 337 declares unlawful the importation, the sale for importation, or the sale after importation into the United States of articles that infringe a valid and enforceable United States patent by the owner, importer, or consignee of the articles, if an industry relating to the articles protected by the patent exists or is in the process of being established in the United States. *See* 19 U.S.C. §§ 1337(a)(1)(B)(I) and (a)(2). Pursuant to Section 337, the Commission shall investigate alleged violations of the Section and hear and decide actions involving those alleged violations.

Respondents argue that the Commission lacks jurisdiction because (1) Rambus cannot satisfy the domestic industry requirement; (2) Rambus lacks standing to assert the Dally Patents; and (3) certain respondents do not import, sell for importation or sell after importation any accused products. (RIB at 7.) As set forth *supra* in Section II, the ALJ found that the importation requirement has been satisfied. The ALJ notes that Respondents do not dispute that the Commission has *in personam* or subject matter jurisdiction. (RIB at 7.) Respondents have fully participated in the investigation, including participating in discovery, participating in the hearing, and filing pre-hearing and post-hearing briefs. Accordingly, the ALJ finds that Respondents have submitted to the jurisdiction of the Commission. *See Certain Miniature Hacksaws*, Inv. No. 337-TA-237, Pub. No. 1948, Initial Determination at 4, 1986 WL 379287

(U.S.I.T.C., October 15, 1986) (unreviewed by Commission in relevant part). Furthermore, as the Federal Circuit held in *Amgen, Inc. v. Int'l Trace Comm'n*

> As is very common in situations where a tribunal's subject matter jurisdiction is based on the same statute which gives rise to the federal right, the jurisdictional requirements of section 1337 mesh with the factual requirements necessary to prevail on the merits. In such a situation, the Supreme Court has held that the tribunal should assume jurisdiction and treat (and dismiss on, if necessary) the merits of the case.

Amgen, Inc. v. United States Int'l Trade Comm'n, 902 F.2d 1532, 1536 (Fed. Cir. 1990). Thus, as for Respondents' remaining arguments, *e.g.*, lack of domestic industry and lack of standing relating to the Dally Patents, the ALJ will address those *infra* in the appropriate sections.

IV. CLAIM CONSTRUCTION

A. Barth Patents

On June 22, 2009, the ALJ issued *Order No. 12: Construing the Terms of the Asserted Claims of the Patent at Issue* in Investigation No. 337-TA-661.[4] The parties in the instant investigation have agreed that the claim terms construed in that order should govern in this investigation, but that any terms not previously construed should be given their plain and ordinary meaning. (CIB at 11; RIB at 20-21; SIB at 18.) To the extent that the parties disagree about the plain and ordinary meaning of any claim terms, such disputes were addressed in the context of infringement and/or invalidity. As such, the ALJ will follow a similar practice and address those disputes in the relevant sections below.

B. Dally Patents

"Processor"

[4] On June 25, 2009, the ALJ issued a Notice Regarding Order No., 12 where he corrected an error in the order.

Rambus	Staff/Respondents
"Circuitry for processing data"	"Circuitry for processing data"

The parties agree on the construction of "Processor" but disagree on what that definition means. Rambus contends that the parties dispute the application of this construction in the context of certain prior art references. Specifically, Rambus argues that the definition does not include certain prior art references that use Manchester encoders. Respondents and Staff argue that "circuitry for processing data" is broad enough to include Manchester encoders and biphase encoders because these circuits process data. Rambus does not argue that a claim construction compels this result and instead offers factual testimony about whether these prior art references come within the scope of the claims. The ALJ discerns no reason to further construe the claims because the dispute between the parties is a factual dispute. Accordingly, the ALJ will deal with this factual dispute below in the context of the specific prior art references.

"Output Frequency"

Rambus	Staff/Respondents
"One-half of the value of the output data rate"	"output data rate"

Rambus argues that "output frequency" as used in the claims and in the context of the technology requires that "output frequency" be one half the output data rate. Staff and Respondents argue that in light of the disclosure of the patent, the term should be construed as output data rate. The ALJ agrees with Staff and Respondents that the term should be construed as "output data rate."

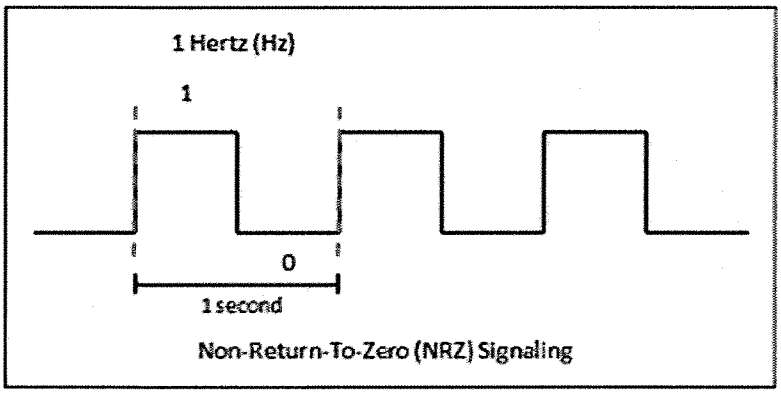
Beginning with the language of the claims, Rambus argues that the plain meaning of "frequency" compels its construction. Rambus notes that frequency is often expressed in units of Hertz, where one Hertz is one cycle per second. (CIB at 181 (citing Tr. 684:9-13.) Rambus further argues that in the context of electrical signaling, one cycle corresponds to one high signal

level and one low signal level. (CIB at 181 (citing Tr. 684:17-685:5).) Rambus argues that the asserted claims of the Dally patents are directed to non-return-to-zero signaling and that in this type of signaling, each high signal level represents one bit of data (*i.e.*, a one) and each low signal level also represents one bit of data (*i.e.*, a zero). (CIB at 181 (citing Tr. 1472:22-1473:5).) Rambus contends that because under this conceptualization, two bits of data are represented in a single Hertz then the plain and ordinary meaning of "output frequency" is one-half of the output data rate. (CIB at 181.)

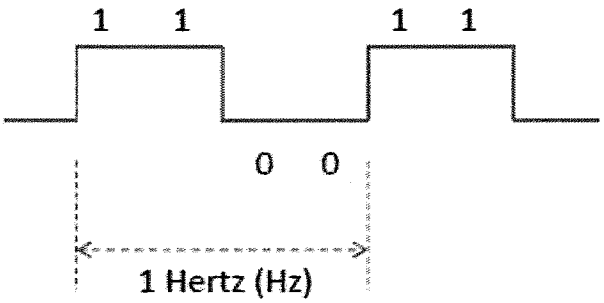
Staff and Respondents disagree with Rambus's plain meaning of the term "output frequency." Contrary to Rambus's assertion regarding the plain meaning, Staff explains that in a digital system such disclosed in the Dally patents, cycles-per-second is often referred to in terms of the system's "symbol rate" (also known as baud (Bd)), with each symbol representing one or more bits depending on the particular implementation. (SIB at 135 (citing Tr. 1555:21-24; RX-5506C at Q/A 59-61).) Staff notes that Dr. Singer, Rambus's expert, agreed with this assessment at his deposition, but attempted to rescind that prior testimony at trial. (SIB at 136 n.87 (citing Tr. 710:09-714:06).) Respondents agree with Staff's assessment and point out that Rambus's model depends on a series of mistaken assumptions. Respondents argue that Rambus's first mistaken assumption is that one cycle corresponds to one high signal level and one low signal level. (RRB at 55.) Respondents assert that this is based testimony from Dr. Singer concerning sine waves oscillating at fixed frequencies and is inconsistent with the type of signaling disclosed in the Dally patents. (RRB at 55.) The second error Respondents point to is Rambus's allegation that the asserted claim relate to non-return to zero signaling. (RRB at 56.) The third error Respondents contend that Rambus makes in its "plain meaning" analysis is that the Dally patents only use the rising edge of the clock to sample each bit of data. (RRB at 56.) Staff

agrees with these criticisms (SRB at 69-71) and argues that these assumptions may not be true. Thus, Staff contends that contrary to Rambus's assertion, there is or no plain meaning that necessarily requires that output frequency be one-half the output data rate. (CRB at 71.)

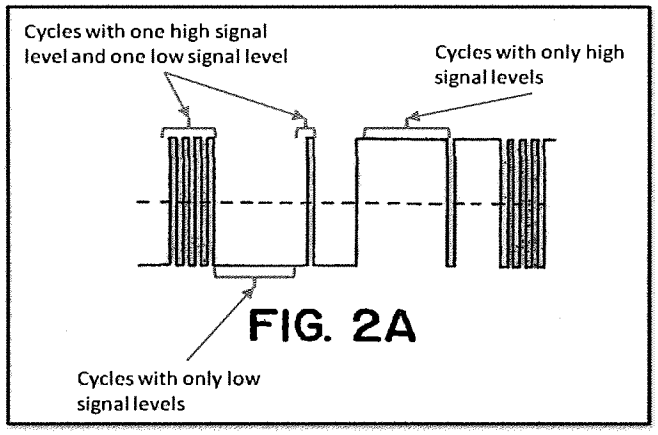
The ALJ agrees with Staff and Respondents that at the very least Rambus's assertion that its definition is necessarily the "plain meaning" of the claim term "output frequency" is simply not correct. The ALJ agrees with Respondents and Staff that Rambus's "proof" requires a number of assumptions that may or may not be true and certainly are not mandated without review of the other intrinsic evidence. As Staff and Respondents cogently illustrated, underlying Rambus's construction is the assumption that the signal is a simple sinusoidal wave (illustrated below):



But as Staff explained, a one hertz clock signal could also be generated using 4 bits, 8 bits, etc… :

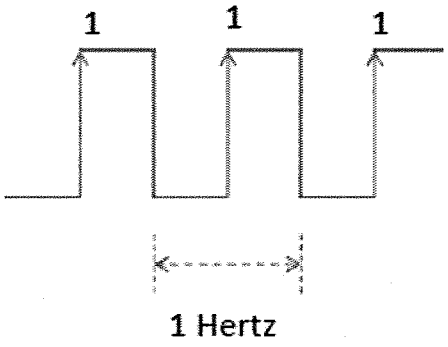


Moreover, Respondents correctly note that the error of Rambus's assumption that one cycle necessarily includes one high signal and one low signal is further illustrated by Figure 2 of the Dally, which does not follow that assumption:



Thus, it is apparent that Rambus's assumption that "[i]n the context of electrical signaling, one cycle corresponds to one high signal level and one low signal level[]" is not necessarily correct and cannot establish that Rambus's definition is the "plain meaning" of the term output frequency.

As for Rambus's assumption that the Dally Patents require Non-Return to Zero signaling, the ALJ finds nothing in the plain language that would support such an assumption. While that assumption might be valid in light of the other intrinsic evidence, Rambus has failed to provide sufficient evidence to establish that based on the claim language alone that such an assumption is warranted. As the Staff further demonstrated, the evidence presented at the hearing established that other coding schemes exist within the art, such as Manchester or bi-phase coding. As Staff demonstrated in the following figure, in Manchester or bi-phase encoding, a clock signal can be represented by alternating high and low values with a clock rate in hertz that is equal to the bit rate required to represent that clock signal:



The ALJ finds that while this information regarding the plain meaning presented by Staff and Respondents does not establish that Staff's and Respondents' construction is necessarily correct, it fundamentally undermines Rambus's principal argument that its construction is necessarily the plain meaning of the term "output frequency."

Respondents also argue that Rambus's construction would render other limitations in the same claims superfluous. (RIB at 120-121 (citing *Stumbo v. Eastman Outdoors, Inc.*, 508 F.3d 1358, 1362 (Fed. Cir. 2007)).) Respondents point to Claim 2, which includes two separate limitations, one related to output frequency and another related to bandwidth. Respondents assert that Dr. Singer acknowledges that under his construction, for a non-modulated system, "just saying the output frequency was at least a gigahertz would make the 100 megahertz irrelevant." (RIB at 121 (quoting Tr. at 725:12-16).) Respondents note that, in contrast, Dr. Hassoun does not specify a relationship between "output frequency" and bandwidth, nor does his construction rely on one; therefore, "[Dr.] Hassoun's construction does not render the bandwidth limitation superfluous." (RIB at 123 (citing RX-5431C at Q/A 68).) Respondents contend that in a modulated system, the "output frequency" is the center or carrier frequency, and not half the data rate. (RIB at 123 (citing Singer Depo Tr. at 350:25-351:24).) Thus, Respondents argue that Rambus's construction only applies to a subset of systems covered by claim 2 (*i.e.* excludes modulated systems) and for nonmodulated systems, its construction renders the bandwidth

limitation superfluous.

Rambus argues that Respondents' argument rests on the assumption that the claims are only directed to nonmodulated systems, but dependent claim 6 recites a nonmodulated limitation demonstrating that the claims are directed to both modulated and non-modulated systems. (CRB at 100.) Rambus asserts that in a modulated system that it is possible to have an output frequency of greater than 1GHz while the bandwidth is less than 100 MHz because the output frequency and bandwidth are independent. (CRB at 100.)

The ALJ agrees with Respondents that this flaw does cast further doubt on Rambus's argument, but it is not dispositive. It simply reinforces the need to look closely at the specification for additional guidance on what a person of ordinary skill in the art would understand this term to mean.

Rambus contends that the specification supports its construction as well. Specifically, Rambus relies on two passages that it contends confirm its construction. In the first passage, the specification relates "a 4 Gb/s signal (FIG. 2A)" and the attenuation of "[t]he highest frequency of interest (2 GHz)." (CIB at 181 (citing JX-120 at 3:59-63).) The second passage states "our operating frequency of 2GHz corresponding to a bit rate of 4 Gb/s." (CIB at 181 (citing JX-120 at 4:16-19).) Rambus argues that these two passages confirm that a Non-Return to Zero signal with an output frequency of 2 GHz has a data rate of 4 Gb/s. (CIB at 181-182.) Rambus asserts that none of the passages cited by the Respondents and Staff can support the one-bit-per Hertz construction that Respondents and Staff advocate. (CIB at 182.) Rambus argues that the passages relied on by Respondents and Staff do not support Respondents' and Staff's construction because they are silent as to the relationship between Hertz and bit rate. (CIB at 182-183.) Rambus argues that the references to 4 GHz pertains to the clock rate used to operate

on the data. (CIB at 183.) Rambus asserts that "[w]hen only the rising edge of a clock is used, the clock needs to operate at twice the frequency of the data." (CIB at 183.)

Respondents and Staff argue that the specification specifically ties data rates to output frequency. Respondents and Staff note that in the Background of Invention section the applicant distinguishes prior art by tying frequency with data rates:

> Most digital systems today use full-swing unterminated signaling methods that are unsuited for data rates over 100 MHz on one meter wires. Even good current-mode signaling methods with matched terminations and carefully controlled line and connector impedance are limited to about 1 GHz by the frequency-dependent attenuation of copper lines.

(JX-120 at 1:32-37.) Respondents urge that this shows that specification uses Hertz in connection with data rates contrary to Rambus's suggestion. (RIB at 119.) Respondents further argue that the specification "closely ties "4 GHz" and "4 Gbps" together in the context of frequency and data rate, demonstrating a 1-to-1 correlation between output frequency and output data rate." (RIB at 119.) Specifically, Respondents note that Figure 12, for example, depicts a transmitter that "accepts 10 bits of data, D_{0-9}, at 400 MHz." (RIB at 119 (quoting JX-120 at 7:5-6).) Respondents assert that the specification shows that these 10 bits of 400 MHz parallel data are ultimately converted and output at 4 Gbps serially. (RIB at 119.) Respondents also point to the discussion of Figure 1 of the Dally patents, which discusses converting 10-bit parallel data at 400 MHz to serial data operating at an output data rate of 4 Gbps. (RIB at 119 (citing JX-120 at 3:16-19).) Finally, Respondents argue that the specification also states that a "4 Gbps serial channel . . . . replaces 40 100 MHz pins," which corresponds to one serial channel at 4 GHz. (RIB at 119 (quoting JX-120 at 8:13-16).) However, Rambus argues that this also supports their construction because it improperly assumes that the reference is to single-ended signaling,

whereas it is in fact differential signaling where two pins are used for a single channel. (CIB at 183-184.)

The ALJ agrees with Respondents and Staff that the specification supports their construction of output frequency. The ALJ notes that outside of the claims, the term "output frequency" is not used in the specification. The preferred embodiments, however, would suggest to a person of ordinary skill in the art what was meant by the term output frequency. One such preferred embodiment is shown in Figure 1, which "shows one channel of a high-speed signaling system embodying the invention." (JX-120 at 3:15-17; *see also* Tr. 1556:20-1560:06.) This Figure appears as follows:

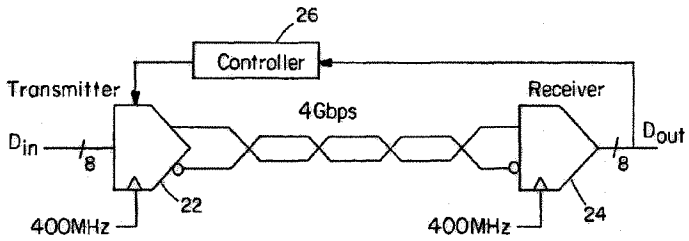


FIG. 1

The ALJ agrees with Staff that in the embodiment of Figure 1, the "transmitter module 22 accepts 8-bit parallel data at 400 MHz." (JX-120 at 3:16-17; *see also* Tr. 1558:12-1559:06.) Staff is correct that the bit rate for data input to the transmitter is thus 8-bits parallel x 400 MHz, *i.e.*, the equivalent of 1-bit serial x 3.2 GHz (*i.e.*, 8 x 400 MHz = 1 x 3.2 GHz). (Tr. 1558:04-11.) Staff is further correct that within the transmitter module 22, the 8-bit parallel data "is coded into 10 bits for band-limiting and forward error correction and transmitted . . . across a single differential transmission line." '(JX-120 at 3:17-19; *see also* Tr. 1558:12-1559:15.) Thus, the transmitter module 22 is processing the equivalent of 10-bits parallel x 400 MHz. (Tr. 1558:12-1559:15.) However, Figure 1 specifies the rate for the serial channel on which the transmitter module 22 transmits those bits in terms of bits-per-second (*i.e.*, 4 Gbps) rather than in terms of

Hertz (*i.e.*, 10 x 400 MHz = 4 GHz). The 4 Gbps label thus suggests that the embodiment of Figure 1 has a 1:1 ratio between bits-per-second and Hertz, which is consistent with the previous discussion of the prior art embodiment in column 1. (Tr. 1559:18-1560:06.)

The ALJ agrees with Staff and Respondents that the embodiment shown in Figure 12 is also consistent with the construction proposed by the Staff and Dr. Hassoun:

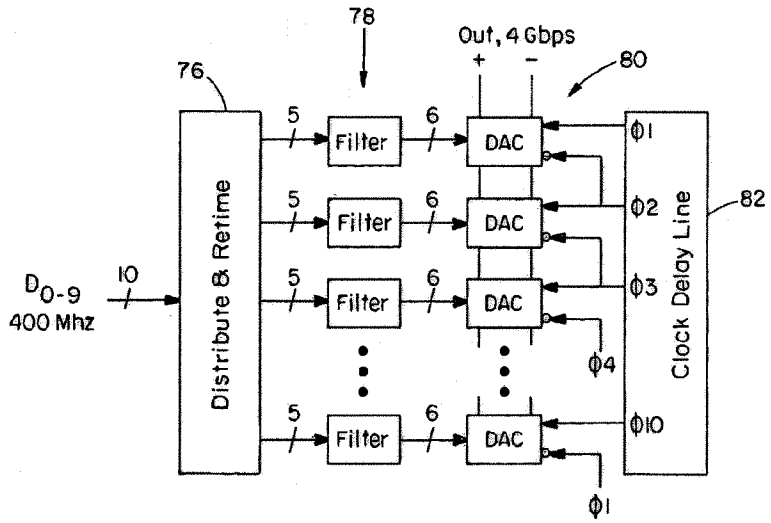


FIG. 12

In this embodiment, "[t]he transmitter accepts 10 bits of data, D_{0-9}, at 400 MHz." (JX-120 at 7:5-6; *see also* Tr. 1560:07-1561:21; Tr. 804:16-805:16, 809:18-22 (Dr. Singer).) The 10 bits of data at 400 MHz (parallel) are ultimately converted and output at 4 GHz serially (over the differential "+ -" output) = *i.e.*, 10 x 400 MHz = 4 GHz. (Tr. 1560:07-1561:21; Tr. 805:19-806:06 (Dr. Singer).) However, Figure 12 does not label its output in terms of GHz. Rather, Figure 12 specifies a "4 Gbps" output, again equating 4 Gbps with the 4 GHz of data known to be leaving the transmitter per the prior calculation. (Tr. 1560:24-1561:21.) Thus, the ALJ agrees with Respondents and Staff that more than just mentioning 4 Gb/s and 4 GHz close to each other, as Rambus suggests (CIB at 183), the embodiment of Figure 12 *and* the embodiment of Figure 1 both appear to use a 1:1 ratio between bits-per-second and Hertz.

The ALJ finds that yet another example supporting a 1:1 ratio appears in column 8, which reads in part:

> A 4 Gbs serial channel can also be used as a replacement technology at both the component and system level. At the component level, a single serial channel (two pins) replaces 40 100 MHz pins.

(JX-120 at 8:13-16.) Forty parallel channels at 100 MHz equates to one serial channel at 4 GHz, *i.e.*, 40 x 100 MHz (parallel) = 4 GHz (serial). The ALJ agrees with Staff that Rambus misreads this passage. Staff is correct that the 4 Gbps single channel described in this embodiment is a "two pin" implementation that uses differential signaling (requiring two pins for a given channel) described elsewhere in the patent. (JX-120 at 3:17-19 (describing differential signaling).) However, Staff is correct that because this passage describes only the single serial channel as a "two pin" differential configuration, the "40 100 MHz pins" also disclosed in this same passage is not "two pin" differential configuration. The ALJ agrees that the "40 100 MHz" configuration instead refers to single-ended signaling, requiring one pin for a given channel. In any event, the ALJ finds that even if Rambus is correct, the fact that one embodiment is inconsistent is not fatal to Respondents' and Staff's construction. *See August Tech. Corp. v. Camtek, Ltd.*, 655 F.3d 1278, 1285 (Fed. Cir. 2011) (quoting *TIP Sys., LLC v. Phillips & Brooks/Gladwin, Inc.*, 529 F.3d 1364, 1373 (Fed. Cir. 2008)) ("The mere fact that there is an alternative embodiment disclosed in the asserted patent that is not encompassed by our claim construction does not outweigh the language of the claim, especially when the court's construction is supported by the intrinsic evidence." (alternations and quotation marks omitted)). Thus, here again the Dally patents speak in terms of Gbps with a 1:1 ratio between bits-per-second and Hertz.

The ALJ further agrees that Rambus is simply incorrect that these examples are merely referring to "clock rate." Moreover, the ALJ agrees with Respondents that the passages cited by Rambus are not particularly persuasive because they are discussing the relationship between data

rate and operating frequency, not output frequency, which do not appear to be the same thing, or at the very least, Rambus has not presented evidence that they are the same thing. (*See* CIB at 181 (JX-120 at 3:59-69, 4:16-19 ("our operating frequency correspond[s] to a bit rate of 4 Gb/s").)

Staff also cite various extrinsic evidence. (SIB at 138; SRB at 72.) However, the ALJ finds that based on the intrinsic evidence, the meaning of the term "output frequency" is clear. The ALJ does not find it necessary to consult this evidence.

Accordingly, the ALJ finds that the intrinsic evidence supports Respondents' and Staff's construction of the term "output frequency" as "output data rate."

"Transmitter Circuit"/ "Transmitter"[5]

Rambus/Staff/LSI Seagate	Respondents (other than LSI/Seagate)
Plain and ordinary meaning	"digital transmitter that comprises an equalizer that generates signal levels as a logical function of bit history to emphasize transition signal levels as distinguished from a conventional FIR filter in which the input is delayed and the individual delayed signals are weighted and summed, but not applied to additional digital circuitry"

Rambus and Staff argue that these terms should be given their plain and ordinary meaning. One of Respondents' experts, who testified on behalf of LSI and Seagate, Dr. Hajimiri agrees. The remaining Respondents (who will be referred to as "Respondents" for the remainder of this section) and their expert, Dr. Hassoun contend that "transmitter circuit" and "transmitter"

[5] Rambus's Initial Post-Hearing Brief and Staff's Initial Post-Hearing Brief also addressed the terms "output signal" and "output bit signal" with "transmitter" and "transmitter circuit." Respondents did not address those terms, so the ALJ is only construing "transmitter" and "transmitter circuit." In any event, Respondents' and Rambus's experts construed "output signal" and "output bit signal" consistent with their respective definitions of "transmitter" and "transmitter circuit."

should be construed as set forth above. The critical dispute between the parties is whether the claims include so-called conventional FIR filters or not or as Respondents put it: a transmitter circuit that "comprises an equalizer that generates signal levels as a logical function of bit history to emphasize transition signal levels as distinguished from a conventional FIR filter in which the input is delayed and the individual delayed signals are weighted and summed, but not applied to additional digital circuitry." Rambus and Staff (and Dr. Hajimiri) argue that Respondents are improperly attempting to read limitations into the claims.

Beginning with the language of the claims, the parties appear to agree that there is nothing in the language of the claims that would support Respondents' construction. Indeed, the parties agree that the plain meaning of the terms "transmitter circuit" or "transmitter" does not exclude conventional FIR filters. (*See* SIB at 141 (citing Tr. 1439:19-1440:12, 1578:25-1579:07, 1579:8-15, 597:13-598:1, 815:9-817:4).)

Rambus also argues that the claims of an unasserted patent related to the asserted Dally patents expressly recite the limitation – "a logical function of bit history" – that Respondents seek to include in the asserted claims. (RIB at 186 (citing CX-9687 at claims 2, 4-6).) Thus, Rambus contends that the applicant could not have meant to define "transmitter circuit" as Respondents do.

The ALJ agrees that the claim language does not support Respondents' construction. There is no dispute that the terms "transmitter" and "transmitter circuit" have a clear and established meaning in the relevant art. As for Rambus's reliance on what can loosely be described as claim differentiation between the claims in the asserted patents and certain claims in other patents in the Dally patent family, the ALJ does not find it particularly convincing. While the ALJ agrees with Rambus that this language does suggest that the applicant could explicitly

include the limitations that Respondents now seek to include in "transmitter" and "transmitter circuit," Respondents are also correct that the claims Rambus seeks to rely do not include the disputed limitations of "transmitter" or "transmitter circuit." Thus, the ALJ finds that this evidence is not particularly persuasive. *See Curtiss-Wright Flow Control Corp. v. Vela, Inc.*, 438 F.3d 1374, 1380 (Fed. Cir. 2006) ("[C]laim drafters can also use different terms to define the exact same subject matter…").

Looking next at the specification, Rambus responds that the specification refutes Respondents' construction. (CIB at 185.) Specifically, Rambus points to a statement in the specification that "[p]referred implementations of the invention include finite input [*sic.* Impulse] response filters. . . ." (CIB at 185 (citing JX-120 at 5:50-52).) Rambus argues that this statement "provides no limitation on the type of FIR filters that may be used to implement the claimed inventions." (CIB at 185.) Finally, Rambus relies on a statement at the end of the specification that "[w]hile this invention has been particularly shown and described with reference to preferred embodiments thereof, it will be understood by those skilled in the art that various changes in form and details may be made therein without departing from the spirit and scope of the invention as defined by the appended claims." (RIB at 185-186 (citing JX-120 at 8:37-42).)

Rambus also argues that the portions of the specification that Respondents rely on do not support Respondents' arguments. For instance, Rambus contends that the statement in the specification distinguishing "conventional FIR filters" is limited to the embodiment in Figure 8 and does not apply to the embodiments shown in Figures 9 and 10. (CIB at 186.) Rambus argues that none of this evidences the clear disavowal required to narrow the claims. (CRB at 102.)

Staff agrees with Rambus that the specification does disclose the non-conventional FIR filter embodiment that Respondents' rely on, but Staff notes that the Dally patents also disclose embodiments that use more rudimentary conventional FIR filter techniques to perform equalization:

> Preferred implementations of the invention include finite input response (FIR) filters, and FIG. 8 illustrates one such implementation. In this case, a 5 tap filter has been selected as a balance between higher fractional bandwidth and circuit complexity. With a greater number of taps, equalization can be obtained at lower frequencies.

(JX-120 at 5:50-55.)

Staff argues that while there are some references in the specification referring to the non-conventional FIR filters as the "present invention" these other embodiments show the invention is broader than that and therefore the use of the "present invention" should not be limiting. (SIB at 143.)

Respondents, on the other hand, contend that the specification "unequivocally limits the patent to a transmitter that generates signal levels as a logical function of bit history and excludes conventional FIR filters that weight and sum individual delayed input bits." (RIB at 115.) Respondents point to a statement in the specification where the inventors distinguished the filter used in one of the embodiments from a "conventional" FIR filter. *See* JX-120 at 5:59-63 ("As in a conventional FIR filter, the input D_i is delayed in successive delay elements 28. However, rather than weighting the individual delayed signals and summing the weighted signals to obtain the desired output, the delayed signals are applied to a 5-to-32 decoder.").

Respondents also argue that none of the preferred embodiments show weighting of individual delayed bits and instead, they argue that each depicts executing a logical function of bit history using 'logic elements (*e.g.*, 5-to-32 decoders, random access memory, and look-up tables)." (RIB at 113.) Respondents further point to statements in the Abstract that describe the

transmitter as including an equalizer and that "[t]he equalizer generates signal levels as a logical function of bit history to emphasize transition signal levels relative to repeated signal levels." (RIB at 115 (quoting JX-120 at Abstract).) Respondents further point to the Summary of the Invention, which states that:

> In accordance with the present invention, a digital transmitter comprises an equalizer which emphasizes transition levels relative to repeated signal levels. In particular, a novel equalizer generates signal levels as a logical function of bit history to emphasize transition signal levels. Preferred implementations define the logical function of bit history in a look up table. (JX-120 at 1:61-67.)

Respondents say they do not dispute that the specification includes embodiments using a FIR filter. Rather, Respondents argue that they dispute whether the specification includes embodiments that use *conventional* FIR filters. (RRB at 59.) Respondents contend that Rambus is incorrect that the statements distinguishing conventional FIR filters are limited to the embodiment shown in Figure 8 and do not involve Figure 9 and 10. (RRB at 60.) Respondents assert that as shown in Figure 8, the individual delayed input signals are applied directly to the decoder without any weighting. (RRB at 60.) Respondents argue that "[t]he Specification explains that the embodiments of Figures 9 and 10 'simplify' the circuit in Figure 8 by replacing the decoder (*i.e.*, the circuitry that performs a logical function of bit history) with a 'find-first-one unit' and 'exclusive-OR gate,' respectively." (RRB at 60.) Respondents contend that "[t]he embodiments [of Figures 9 and 10] 'approximate' the functionality of Figure 8 by simplifying the circuitry that generates the signals as a logical function of bit history." (RRB at 60 (citing JX-120 at 6:8-24).) Respondents assert that "[t]he embodiments of Figures 9 and 10, contrary to Rambus's suggestion, do not weight and sum the individual delayed signals, but rather use the same technique Dally said was his invention." (RRB at 61.) Respondents also contest Staff's assertions arguing that contrary to Staff's suggestion that Figure 8 represents a conventional FIR

filter, the specification explains that Figure 8 in fact is different than a conventional FIR filter. (RRB at 63.)

The ALJ agrees with Rambus and Staff that the specification does not provide the support for Respondents' construction. While the specification does distinguish conventional FIR filters, the ALJ agrees with Rambus that this distinction is being drawn between the FIR filter used in the embodiment shown in Figure 8, not the invention generally, and conventional FIR filters. Moreover, the entire discussion is with respect to "[p]referred implementations" of the invention not the invention generally. As for Respondents' reliance on the statements in the Summary of the Invention that provides that "[i]n accordance with the present invention, a digital transmitter comprises an equalizer which emphasizes transition signal levels relative to repeated signal levels[]" and "[i]n particular, a novel equalizer generates signal levels as a logical function of bit history to emphasize transition signal levels." (JX-120 at 1:61-65.) The ALJ agrees with Rambus and Staff that the quoted passage is consistent with the view that the invention is broad enough to encompass multiple types of transmitter circuits including those that emphasize based on a logical function of bit history as well as those that do not. Indeed, the specification states that "[p]referred implementations of the invention include finute input [impulse] response (FIR) filters, and FIG. 8 illustrates one such implementation." (JX-120 at 5:50-53.) Thus, the specification does not limit itself to a particular subset of FIR filters as Respondents suggest.

While Respondents are correct that the specification does emphasize certain preferred embodiments of the invention, Staff is correct that this does not justify reading those embodiments into the claims. *See Absolute Software, Inc. v. Stealth Signal, Inc.*, 659 F.3d 1121, 1136 (Fed. Cir. 2011) ("[U]se of the phrase 'present invention' or 'this invention' is not always so limiting, such as where the reference to a certain limitation as being the 'invention' are not

uniform, or where other portions of the intrinsic evidence do not support applying the limitation to the entire patent."). As for Respondents' contentions that all of the embodiments are limited in a way similar to Figure 8 in that none of them weight and sum the bits and that all of the equalizers disclosed operate as a logical function of bit history, this is more a question of enablement (which they do not raise) than claim construction. *See Liebel-Flarsheim Co. v. Medrad, Inc.*, 358 F.3d 898 (Fed. Cir. 2004). Accordingly, the ALJ agrees with Rambus and Staff that the specification supports a broad interpretation of "transmitter" and "transmitter circuit" that encompasses both conventional FIR filter techniques and the more elaborate techniques of the preferred embodiments.

Respondents have a few more arrows in their quiver. They also point to the prosecution history in support of their construction. Specifically, Respondents rely on statements made by the applicant during the prosecution of a related patent, U.S. Patent No. 7,602,858, which was previously asserted in this investigation and has since been dropped. Respondents argue that "Dally expressly disclaims weighting and summing in the prosecution history." (RIB at 115.)

During the prosecution of the '858 Patent, the applicant stated that "Burlage [a prior art reference cited by the examiner] weighs prior input bits and sums those weighted values . . . By contrast, with the present invention, the strength of each output bit signal can be simply determined by the number of output bit signals since the last preceding transition." (RX-2240 at 103-104.) Respondents assert that even though the claims in the '858 Patent are different, the applicant was referring to the entire invention and not just the particular claims of that application. (RRB at 63.)

Rambus argues that these statements should not be limiting because they were made about a set of claims that are "fundamentally different than the Asserted claims because they

recited emphasis signals based on the output of a transmitter instead of emphasizing based on its input." (CIB at 187.) Staff agrees with Rambus that "[w]hile similar in some respects, the claims of the [application that became the '858 Patent] are different in several other, material respects from the issued claims of the '858 and '494 patents." (SIB at 143.) Staff argues that "[t]he evidence thus shows that the applicant was at most distinguishing the particular embodiments covered by the pending ['858 Patent] claims from prior art being asserted by the Examiner – *not* that there has been a clear disavowal of conventional FIR filter techniques for the Dally invention as a whole." (SIB at 143 (emphasis in the original).)

The ALJ does not find these statements made in a related co-pending application to be particularly helpful to Respondents for at least two reasons. First, the ALJ agrees with Rambus and Staff that while the claims are similar in some respects, the claims of the '858 Patent are different in several other, material aspects. As Rambus correctly explains, the claims that were actually distinguished by the applicant recited emphasizing based on input. (RX-2240 at 96; CX10764C at 15.) The ALJ agrees with the Staff that the evidence shows that the applicant was at most distinguishing the particular embodiments covered by the pending '858 Patent claims from the prior art being cited by the examiner and does not amount to a clear disavowal of conventional FIR filter techniques for the Dally patent family as a whole. (*See* CX-9542C at Q/A 130-131; Tr. 661:10-667:17; JX-32C at 372:22-373:09.) Given this difference, the ALJ finds that the statement applicant made in the prosecution of the '858 Patent does not meet the requirement that "the alleged disavowing statements to be both so clear as to show reasonable clarity and deliberateness, and so unmistakable as to be unambiguous evidence of disclaimer." *Omega Eng'g v. Raytek Corp.*, 334, F.3d 1314, 1323 (Fed. Cir. 2003). *Second*, this finding is further supported by the fact that not only is language different, but these statements were made

during the prosecution of a related application that is not a parent or earlier application of the patents-in-suit. *See, e.g.*, *Ventana Med. Sys., Inc. v. Biogenex Labs., Inc.*, 473 F.3d 1173, 1182 (Fed. Cir. 2006) ("[T]he doctrine of prosecution disclaimer generally does not apply when the claim term in the decedent patent uses different language."); *Invitrogen Corp. v. Clontech Labs., Inc.*, 429 F.3d 1052, 1078 (Fed. Cir. 2005) ("[T]he prosecution of one claim term in a parent application will generally not limit different claim language in a continuation application."). Accordingly, the ALJ finds that the prosecution history does not limit the plain meaning of the asserted claims here.

Finally, Respondents also rely on statements made by Dr. Dally, the named inventor, and Dr. Poulton, a scientist who worked with Dr. Dally (but who is not a named inventor) to the effect that Dr. Dally did not invent convention FIR filters, but rather something different. (RIB at 116-117.) Rambus responds that this is irrelevant because the claims are not directed to the filter used but something broader and most inventions are combinations of old elements. (CRB at 102.) Staff responds with the definition from an electrical engineering dictionary that defines "transmitter" as "an equipment for producing and sending signals." (SIB at 56 (quoting SX-5 at 597).) The ALJ finds the extrinsic evidence cited by the Respondents to not be persuasive here. Not only is Rambus correct that the claimed invention here is broader than just the filter, this type of post hoc testimony cannot overcome the clear intrinsic evidence in this case. *See N. Am. Vaccine, Inc. v. Am. Cyanamid Co.*, 7 F.3d 1571 (Fed. Cir. 1993) (holding "after-the-fact testimony is of little weight compared to the clear import of the patent disclosure itself").

Accordingly, the ALJ agrees with Rambus and Staff that the terms "transmitter" and "transmitter circuit" should have their plain and ordinary meaning. The ALJ agrees with Staff that the claim language itself is not inherently ambiguous and that there is a well-established

meaning for the disputed terms and that there has been no clear effort to limit the scope of the claims in the intrinsic evidence. (*See* SRB at 56 (citing SX-5 at 597).) The ALJ notes that Respondents have presented a compelling argument, but the ALJ believes that the intrinsic evidence demonstrates that the inventor did not limit his invention in the way that Respondents contend.

V. INFRINGEMENT DETERMINATION

A. Applicable Law

In a Section 337 investigation, the complainant bears the burden of proving infringement of the asserted patent claims by a preponderance of the evidence. *Certain Flooring Products*, Inv. No. 337-TA-443, Commission Notice of Final Determination of No Violation of Section 337, 2002 WL 448690 at 59, (March 22, 2002); *Enercon GmbH v. Int'l Trade Comm'n,* 151 F.3d 1376 (Fed. Cir. 1998).

Each patent claim element or limitation is considered material and essential. *London v. Carson Pirie Scott & Co.*, 946 F.2d 1534, 1538 (Fed. Cir. 1991). Literal infringement of a claim occurs when every limitation recited in the claim appears in the accused device, *i.e.,* when the properly construed claim reads on the accused device exactly. *Amhil Enters., Ltd. v. Wawa, Inc.*, 81 F.3d 1554, 1562 (Fed. Cir. 1996); *Southwall Tech. v. Cardinal IG Co.*, 54 F.3d 1570, 1575 (Fed Cir. 1995).

If the accused product does not literally infringe the patent claim, infringement might be found under the doctrine of equivalents. The Supreme Court has described the essential inquiry of the doctrine of equivalents analysis in terms of whether the accused product or process contains elements identical or equivalent to each claimed element of the patented invention. *Warner-Jenkinson Co., Inc. v. Hilton Davis Chemical Co.*, 520 U.S. 17, 40 (1997).

Under the doctrine of equivalents, infringement may be found if the accused product or process performs substantially the same function in substantially the same way to obtain substantially the same result. *Valmont Indus., Inc. v. Reinke Mfg. Co.*, 983 F.2d 1039, 1043 (Fed. Cir. 1993). The doctrine of equivalents does not allow claim limitations to be ignored. Evidence must be presented on a limitation-by-limitation basis, and not for the invention as a whole. *Warner-Jenkinson*, 520 U.S. at 29; *Hughes Aircraft Co. v. U.S.*, 86 F.3d 1566 (Fed. Cir. 1996). Thus, if an element is missing or not satisfied, infringement cannot be found under the doctrine of equivalents as a matter of law. *See, e.g., Wright Medical*, 122 F.3d 1440, 1444 (Fed. Cir. 1997); *Dolly, Inc. v. Spalding & Evenflo Cos., Inc.*, 16 F.3d 394, 398 (Fed. Cir. 1994); *London v. Carson Pirie Scott & Co.*, 946 F.2d 1534, 1538-39 (Fed. Cir. 1991); *Becton Dickinson and Co. v. C.R. Bard, Inc.*, 922 F.2d 792, 798 (Fed. Cir. 1990).

The concept of equivalency cannot embrace a structure that is specifically excluded from the scope of the claims. *Athletic Alternatives v. Prince Mfg., Inc.*, 73 F.3d 1573, 1581 (Fed. Cir. 1996). In applying the doctrine of equivalents, the Commission must be informed by the fundamental principle that a patent's claims define the limits of its protection. *See Charles Greiner & Co. v. Mari-Med. Mfg., Inc.*, 92 F.2d 1031, 1036 (Fed. Cir. 1992). As the Supreme Court has affirmed:

> Each element contained in a patent claim is deemed material to defining the scope of the patented invention, and thus the doctrine of equivalents must be applied to individual elements of the claim, not to the invention as a whole. It is important to ensure that the application of the doctrine, even as to an individual element, is not allowed such broad play as to effectively eliminate that element in its entirety.

Warner-Jenkinson, 520 U.S. at 29.

Prosecution history estoppel may bar the patentee from asserting equivalents if the scope of the claims has been narrowed by amendment during prosecution. A narrowing amendment

may occur when either a preexisting claim limitation is narrowed by amendment, or a new claim limitation is added by amendment. These decisions make no distinction between the narrowing of a preexisting limitation and the addition of a new limitation. Either amendment will give rise to a presumptive estoppel if made for a reason related to patentability. *Honeywell Int'l Inc. v. Hamilton Sundstrand Corp.*, 370 F.3d 1131, 1139-41 (Fed. Cir. 2004), *cert. denied*, 545 U.S. 1127 (2005)(citing *Warner-Jenkinson*, 520 U.S. at 22, 33-34; and *Festo Corp. v. Shoketsu Kinzoku Kogyo Kabushiki Co.,* 535 U.S. 722, 733-34, 741 (2002)). The presumption of estoppel may be rebutted if the patentee can demonstrate that: (1) the alleged equivalent would have been unforeseeable at the time the narrowing amendment was made; (2) the rationale underlying the narrowing amendment bore no more than a tangential relation to the equivalent at issue; or (3) there was some other reason suggesting that the patentee could not reasonably have been expected to have described the alleged equivalent. *Honeywell*, 370 F.3d at 1140 (citing, *inter alia*, *Festo Corp. v. Shoketsu Kinzoku Kogyo Kabushiki Co.,* 344 F.3d 1359 (Fed. Cir. 2003)(*en banc*)). "Generalized testimony as to the overall similarity between the claims and the accused infringer's product or process will not suffice [to prove infringement under the doctrine of equivalents]." *Tex. Instruments, Inc. v. Cypress Semiconductor Corp.*, 90 F.3d 1558, 1567 (Fed. Cir. 1996).

Section 271(b) of the Patent Act prohibits inducement: "[w]hoever actively induces infringement of a patent shall be liable as an infringer." 35 U.S.C. § 271(b) (2008). As the Federal Circuit stated:

> To establish liability under section 271(b), a patent holder must prove that once the defendants knew of the patent, they "actively and knowingly aid[ed] and abett[ed] another's direct infringement." However, "knowledge of the acts alleged to constitute infringement" is not enough. The "mere knowledge of possible infringement by others does not amount to inducement; specific intent and action to induce infringement must be proven."

DSU Med. Corp. v. JMS Co., 471 F.3d 1293, 1305 (Fed. Cir. 2006) (*en banc*) (citations omitted); *See also Cross Medical Products, Inc. v. Medtronic Sofamor Danek, Inc.*, 424 F.3d 1293, 1312 (Fed. Cir. 2005) ("In order to succeed on a claim inducement, the patentee must show, first that there has been direct infringement, and second, that the alleged infringer knowingly induced infringement and possessed specific intent to encourage another's infringement."). Mere knowledge of possible infringement by others does not amount to inducement. Specific intent and action to induce infringement must be proven. *Warner-Lambert Co. v. Apotex Corp.,* 316 F.3d 1348, 1363 (Fed. Cir. 2003). In *DSU*, the Federal Circuit clarified the intent requirement necessary to prove inducement. As the court recently explained:

> In *DSU Med. Corp. v. JMS Co.,* this court clarified en banc that the specific intent necessary to induce infringement "requires more than just intent to cause the acts that produce direct infringement. Beyond that threshold knowledge, the inducer must have an affirmative intent to cause direct infringement."

Kyocera Wireless Corp. v. Int'l Trade Comm'n, 545 F.3d 1340, 1354, (Fed. Cir. 2008) (citation omitted). "Proof of inducing infringement requires the establishment of a high level of specific intent." *Lucent Techs. Inc. v. Gateway, Inc.*, 2007 WL 925510, at *2-3 (S.D. Cal. 2007)

Under 35 U.S.C. § 271(c), "[w]hoever offers to sell or sells within the United States or imports into the Unites States a component of a patented machine, manufacture, combination, or composition, or a material or apparatus for use in practicing a patented process, constituting a material part of the invention, knowing the same to be specifically made to or specially adapted for use in the infringement of the patent, and not a staple article or commodity suitable for substantial non-infringing use, shall be liable as a contributory infringer."

A seller of a component of an infringing product can also be held liable for contributory infringement if: (1) there is an act of direct infringement by another person; (2) the accused contributory infringer knows its component is included in a combination that is both patented and infringing; and (3) there are no substantial non-infringing uses for the accused component, *i.e.*, the component is not a staple article of commerce. *Carborundum Co. v. Molten Equip. Innovations, Inc.*, 72 F.3d 872, 876 (Fed. Cir. 1995).

To prove direct infringement, Rambus must prove by a preponderance of the evidence that the accused products either literally infringe or infringe under the doctrine of equivalents the method of asserted claims of the '353, '405, '109, '494 and '857 Patents. *Advanced Cardiovascular Sys., Inc. v. Scimed Life Sys., Inc.*, 261 F.3d 1329, 1336 (Fed. Cir. 2001). Notably, method claims are only infringed when the claimed process is performed. *Ormco Corp. v. Align Technology, Inc.*, 463 F.3d 1299, 1311 (Fed. Cir. 2006). Furthermore, in order to establish a violation of Section 337 of a method claim, it is insufficient for Rambus to show that the accused products directly infringe. Rather, Rambus must show that the accused products indirectly infringe those method claims. *Electronic Devices with Image Processing Systems*, Inv. No. 337-TA-724, Comm'n Op. at 18-19.

B. The Barth Patents

Rambus asserts that the Accused Barth Products infringe claims 11-13 of the '353 Patent and claims 1, 2, 4, 12, 20, 21 and 24 of the '109 Patent. (CIB at 25.) Rambus asserts that Accused Barth Products that issue the write command with autoprecharge commands ("the Accused Autoprecharge Products") infringe the claims 11-13, 15 and 18 of the '405 Patent and claims 5 and 13 of the '109 Patent. (CIB at 25.) Staff agrees. (SIB at 18-35.)

The '353 Patent

a) Claim 11

Claim 11 is a method claim and the only asserted independent claim from the '353 Patent. Rambus and Staff argue that the Accused Barth Products meet each and every limitation of claim 11 of the '353 Patent. Respondents argue that the Accused Barth Products do not practice the "strobe signal" elements of claim 11. The ALJ finds that Rambus has shown by a preponderance of the evidence that the Accused Barth Products directly infringe claim 11.

(1) A Method of Controlling a Memory Device that Includes a Plurality of Cells

The evidence shows that the Accused Barth Products include a memory controller that performs a method of controlling a memory device that includes a plurality of cells. (CX-9543C, Przybylski Direct Q&A 136-43, 216-25, 250-51, 265-68, 310-325, 775-77, 789-808, 860-62, 879-82, 1599-1601, 1617-29, 1668-69, 1688, 2124-25, 2210-12; JX-100C at 14:22-24; JX-110C at 110:18-20; CX-6363C.0001-2; CX-8551C.001-2; JX-107C at 82:13-16; JX-053C at 134:24-135:10; CX-8806.0087; JX-135C at 59:16-18; JX-055C at 24:11-25:10; CX-8065C.0006.) Respondents do not dispute that the Accused Barth Products meet this limitation except to the extent that the claim term "memory devices" includes stacked memory. (RIB at 37-38.) As set for *infra* in Section VI.B.1.c, the ALJ has declined to adopt Rambus's construction and, as such, Respondents' argument is moot.

Therefore, the ALJ finds that Rambus has shown by a preponderance of the evidence that the preamble of claim 11 is met during normal operation of the Accused Barth Products.

(2) Issuing a First Write Command to the Memory Device

The evidence also shows that, when operated with a JEDEC-compliant memory device, the memory controllers in the Accused Barth I Products issue a first write command to the

memory device. Specifically, the memory controllers issue one or more bits that specificy that the memory device receive and store data. (CX-9543C, Przybylski Direct Q&A 143-167, 225-36, 251-57, 268-82, 326-31, 777-83, 808-36, 862-69, 882-95, 1601-09, 1629-51, 1669-77, 1688-92, 2125-34, 2212-26; JX-144C at 310:13-18; JX-075C at 67:19-68:2; CX-8566C.0017; CX-6572.0004; CX-8602C.0081; JX-103C at 119:10-18; CX-8807.0087; JX-055C at 53:17-25; Smith, Tr. 901:19-22.) Respondents do not dispute that the Accused Barth Products meet this limitation. (RIB at 29-41.) Therefore, the ALJ finds that the Accused Barth Products meet this limitation.

(3) Delaying for a First Time Period after Issuing the Write Command

The evidence shows that after issuing a write command, the memory controllers in the Accused Barth Products delay for a period of time ("tDQSS," "WL," or some combination of the two) before asserting a strobe signal and that time must elapse before the controller issues the strobe signal. (CX-9543C at Q&A 167-69, 237-41, 257-59, 282-91, 356-359, 783-85, 836-42, 869-73, 895-902, 1609-12, 1651-56, 1678-81, 1692-93, 2134-37, 2226-32; JX-100C at 40:10-19; CX-6879C.0142; JX-053C at 141:5-10; JX-103C at 119:10-18; JX-055C at 208:12-209:1.) Respondents do not dispute that their Accused Barth Products meet this limitation. (RIB at 29-41.) Thus, the evidence shows that this limitation is met during normal operation of the Accused Barth Products.

(4) The Memory Device Being Configured to Defer Sampling Data That Corresponds to the First Write Command until a Strobe Signal Is Detected/ After Delaying for the First Time Period, Issuing the Strobe Signal to the Memory Device to Initiate Sampling of a First Portion of the Data by the Memory Device

Rambus and Staff argue that the Accused Barth Products issue a strobe signal – the data strobe, DQS or WDQS – that initiates sampling in the memory device. (CIB at 27-31; SIB at 27-30.) Respondents argue that the "strobe signal" in the Barth Patents does not cause the actual sampling of data and that DQS signal in the Accused Barth Products does not initiate sampling as required by the claims, but actually causes sampling to happen. (RIB at 29-32.)

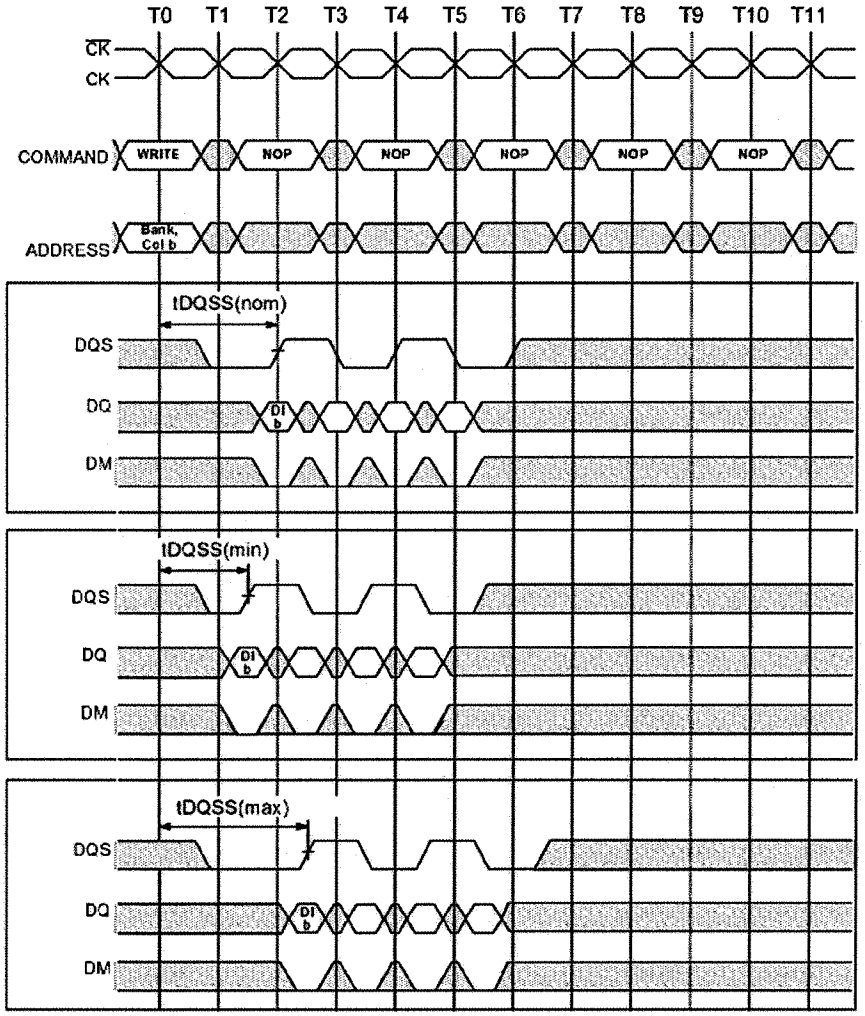
The ALJ finds that the Accused Barth Products meet these claim limitations. The ALJ finds that the "strobe signal" in the Accused Barth Products is the DQS or WDQS strobe signal, depending on the particular JEDEC standard. There does not appear to be a material difference between the two types of signals as they relate to infringement of claim 11. (*See* RIB at 30-32.) Taking the DDR standard as an example, the evidence shows that the DQS strobe signal and its relationship to data propagated on a DQ data bus are mandatory features of the standard:

Symbol	**Type**	**DESCRIPTION**
DQ	I/O	Data Bus: Input/Output
DQS (LDQS) UDQS	I/O	Data Strobe: output with read data, input with write data. Edge-aligned with read data, centered in write data. Used to capture write data. For the X16, LDQS corresponds to the data on DQ0-DQ7; UDQS corresponds to the data on DQ8-DQ15.

CX-4347.0012 (the "DDR Standard"). Indeed, there appears to be no dispute that, when performing a write operation with a JEDEC-compliant memory device, the Accused Barth Products issue a DQS strobe signal to the memory device in accordance with the applicable JEDEC standard.

The evidence further shows that data precedes the DQS signal for some period of time and follows the DQS strobe signal for some period of time. The time period during which data

appears in advance of the DQS signal is generally referred to as "setup" time (t_{DS}). (CX-9543C, Przybylski Direct Q&A 336;CX-4347.0070 (Figure 43); Przybylski, Tr. 2721:06-14.) The setup time t_{DS} ensures that the memory device's sampling circuitry is given sufficient time to stabilize before the edge of the DQS signal initiates sampling of the data. (*Id.*) The time period during which data is held constant after the DQS strobe signal is generally referred to as "hold" time (t_{DH}). (*Id.*) The hold time t_{DH} ensures that the memory device's sampling circuitry has sufficient time to sample the data after the edge of the DQS signal initiates sampling. As shown in Figure 21 of the JEDEC standard, the DQS signal tells the memory device that valid data is on the data lines and the data is sampled on the "rising edge" and the "falling edge" of the DQS signal:



DI b = Data In for column b
Three elements of data are applied in the programmed order following DI b
A noninterrupted burst of 4 is shown
A10 is low with the WRITE command (autoprecharge is disabled)
Example is for a x4 or x8 device where only one Data Mask and one Data Strobe are used. For a X16, UDM and LDM would be required, as well as UDQS and LDQS.

Figure 21
WRITE BURST --Nom., Min., and Max tDQSS

(CX-4347.0039; *see also* CX-9543C, Przybylski Direct Q&A 335-336.) The memory controller's issuance of the DQS strobe signal is carefully coordinated with data transmitted to the memory device. (Przybylski, Tr. 847:06-851:06.) Thus, the DQS signal initiates sampling of data by the memory devices.

The evidence further shows that Respondents' witnesses and documentation confirm that this mandatory strobe to data timing relationship exists with respect to operation of the Accused Barth Products with JEDEC-compliant memory devices. (*See* Jacobs, Tr. 1040:12-1041:21; Smith, Tr. 909:13-910:08, 911:03-913:07, 916:13-19; CX-9543C, Przybylski Direct Q/A 307-393, 489-520, 626-668, 799-831, 902-911, 930-940.) [redacted]

Respondents argue that the Accused Barth Products do not infringe the Barth Patents because (1) the "strobe signal," as construed by Respondents, merely indicates when data transfer can happen, but does not act as a timing signal for actually sampling data and (2) the DQS signal in the Accused Barth Products actually causes sampling of data and does not merely initiate it. Rather, it is the write command that initiates sampling. (RIB at 29-32.) The ALJ finds their arguments unpersuasive.

As for the latter argument, the evidence shows that the write command initiates the write operation, whereas the DQS signal initiates the sampling of data associated with that operation. As set forth *supra*, the evidence shows that the DQS/WDQS signal in the Accused Barth Products initiates sampling of data. Indeed, Respondents' own experts acknowledged that it is the DQS signal – not the write command – that initiates sampling in JEDEC-complaint memory devices. (*See* JX-147C, Walker at 85:07-11; CX-9543C, Przybylski Q&A 350 (quoting deposition testimony of Martin Walker); Jacobs, Tr. 1043:23-1044:17 (discussing same); Smith, Tr. 915-16, 938.) Respondents' expert, Dr. Smith, acknowledges that JEDEC-complaint memory devices delay between the receipt of a write command and the sampling of data

associated with that write command, which supports the view that the DQS signal initiates the sampling of data whereas the write command initiates the write operation. (*See* Smith, Tr. 904:25-905:04.) The evidence further shows that the write command initiates the write operation:

As for Respondents' first argument that the "strobe signal" cannot act as a timing signal for actually sampling data, the ALJ finds that, as Staff correct noted, this is merely a re-hashing of Respondents' written description defense. The ALJ finds that the "strobe signal" that can encompass a signal that is capable of indicating when sampling may begin ("indirect control") and a signal that that actually initiates data sampling ("direct control").

The Barth Patents disclose methods of performing both "read" and "write" data transfer operations with synchronous devices, which inherently requires that a data receiving device "sample" and retain data associated with such an operation.[6] ('353 Patent, 1:11-14; 7:41-43; CX-10765, Przybylski Rebuttal Q&A 175.) There is nothing in the specification or the asserted claims require that sampling (once initiated) be accomplished in a specific manner or by a specific structure. (CX-9543C, Przybylski Direct Q&A 349; Przybylski, Tr. 839:17-840:02.)

[6] In a write operation the memory controller is the data transferring device and the memory device is the data receiving device, such that the memory controller "writes" data to the memory device. *See* RX-5429C, Jacobs Direct Q/A 148-149; Jacobs, Tr. 1052:01-03, 1056:07- 14. By contrast, in a read operation the memory device is the data transferring device and the memory controller is the data receiving device, such that the memory controller "reads" data from the memory device. *See* RX-5429C, Jacobs Direct Q/A 145-147; Jacobs, Tr. 1052:04-06.

Correspondingly, it does not matter whether the strobe is directly or indirectly connected to the sampling mechanism. As Staff correctly noted, one can directly turn a light switch on/off by herself operating the light switch or alternatively indirectly turn the light switch on/off by ordering someone else to do so at a specified time – in both instances the individual has initiated the process by which the light switch is turned on/off.

The ALJ finds Respondents' narrow construction is unsupported by the claims, the specification and the prosecution history. The specification discloses the broad concept of data "sampling" as well as data "sampling" mechanisms that can be employed in a given system. In one such example, the specification explicitly describes a "latch" and the "latching" of data. ('353 patent, 2:13-16 (describing a "latch in the memory controller"); *id.* at 2:25-26 (describing a data input of a memory device that is "latched on the rising edge of the clock"); *id.* at 6:1-2 (describing a memory bank with "a latching sense amplifier cache 604 and 608"); *id.* at 24:19-22, 29:42-44, 37:23-26; Przybylski, Tr. 2734:11-2736:06 (describing "bus samples"). Furthermore, the asserted claims of the Barth Patents are method claims that are broadly directed at the use of a strobe signal that initiates sampling regardless of the specific sampling mechanism for a given system. (CX-9543C, Przybylski Direct Q&A 349; Przybylski, Tr. 839:03-22.) Thus, detailed examples need not be provided for the *claimed* invention to be adequately supported for written description purposes.

The ALJ finds that Respondents' reliance on the testimony of Dr. Przybylski is also misplaced as their arguments mischaracterize his testimony. Dr. Przybylski did not testify that he agrees with the Respondents' experts that sampling in the Accused Barth I Products is initiated by a write command rather than a DQS strobe signal. (RIB at 31-32.) Rather, Dr. Przybylski explained that sampling in a JEDEC-compliant memory device is initiated upon

detection of the DQS strobe signal, *not* the write command, which is timed so as to coincide with the middle of a data packet to be sampled. (Przybylski, Tr. 873:11-17; 878:02-879:13; CX-9543C, Przybylski Direct Q&A 333-336.)

Therefore the ALJ finds that the Accused Barth Products meet the limitations of claim 11.

b) Claim 12

The ALJ finds that the Accused Barth Products meet the limitations of claim 12. Claim 12 depends from claim 11 and states "issuing the first portion of the data and a second portion of the data to the memory device, wherein the first portion of the data is sampled during an odd phase of an external clock signal, and the second portion of the data is sampled during an even phase of the external clock signal." (JX-4 at 41:41-47.) The evidence shows that the Accused Barth Products, when interfaced with a DDR based memory device (*i.e.*, a memory device compliant with any one of the Accused JEDEC Standards, which are all DDR based), issues data in this way. (CX-9543C, Przybylski Direct Q&A 363-390; Jacobs, Tr. 1048:10-1050:07, 1136:06-09; Smith, Tr. 922:11-932:24.) Specifically, two portions of data are provided for sampling during one cycle of an external clock provided to the memory device. The external clock cycle or period may be divided into two portions, one termed an odd phase and the other termed an even phase. Data is presented in each phase and for proper operation the memory device samples the data during those phases. This operation is confirmed by Respondents' testimony and documents and JEDEC standards. (CX-9543C at 171-83, 303-19, 912-31, 1697-1710, 2141-44, 2242-45; CX-7670C.0048; JX-100C at 51:6-52:7; JX-075C at 59:22-60:14; JX-073C at 81:9-11; CX-8178.0005; JX-042C at 59:4-5; CX-8078.0044; JX-055C at 44:5-10.) Indeed, the word "double" in the larger phrase "double data rate" (DDR) refers to the issuance of data during both of the two phases of a clock signal.

Respondents argue the terms "even phase" and "odd phase" in claim 12 fails to encompass any portion of the transitions between the two phases and that since the Accused Barth Products sample data during these transition phases, they do not infringe. (RIB at 33-34.) The ALJ finds such an argument unpersuasive. The evidence shows that a person of ordinary skill in the relevant art would appreciate that an "even" and an "odd" phase of a given clock period together encompass the entire clock period, *including* transitions. (CX-9543C, Przybylski Direct Q&A 177-78; 376-390.) Respondents' own expert agreed that, "[w]hether you say low is odd or low is even is really not significant . . . it is interchangeable. You could just as well refer to odd as high." (Smith, Tr. at 927.) He also agreed that JEDEC defines the transitions as being part of the high and low portions of a clock cycle. (Smith, Tr. at 931.)

Therefore, the ALJ finds that the Accused Barth Products meet every limitation of claim 12.

c) Claim 13

Claim 13 is dependent from claim 12, and further states that "the first and second portions of the data [to be] both issued during a common clock cycle of the external clock signal." (JX-4 at 41:48-50.) In other words, the data is issued during a "common" clock cycle, *i.e.*, the "even" and "odd" phases of claim 12 are back-to-back. The evidence shows that the Accused Barth Products contain double data rate controllers, which issue both portions of the data during a common clock cycle. CX-9543C at 183, 320-36, 391-393; 931-49, 1711-22, 2145-47, 2246-50; CX-6879C.0142; JX-100C at 51:6-52:7; JX-075C at 64:17-23; CX-8178.0005; JX-042C at 59:4-5; CX-8078.0044; JX-055C at 44:5-10.) Respondents' arguments disputing that the Accused Barth Products meet this limitation are the same as those for claim 12. (*See* RIB at

34.) To the extent that they failed with respect to claim 12, they similarly fail with respect to claim 13.

Therefore, the ALJ finds that the Accused Barth Products meet every limitation of claim 13.

'405 Patent

Rambus asserts that Accused Autoprecharge Products infringe the claims 11-13, 15 and 18 of the '405 Patent. (CIB at 25.) Staff agrees. (SIB at 33-34.)

d) Claim 11

Claim 11 of the '405 Patent is similar claim 11 of the '353 Patent and the same type of evidence demonstrating infringement of the '353 Patent similarly can demonstrate infringement of the asserted '405 Patent claims. Claim 11 of the '405 patent is directed to a write with autoprecharge operation and states "a second code which specifies that a precharge operation be initiated automatically after initiation of the write operation." (JX-03.0046.) This is the only additional feature that was not already set forth *supra* in Section V.B.1.a. The ALJ finds that the Accused Autoprecharge Products meet each and every limitation of claim 11.

The evidence shows that the Accused Autoprecharge Products issue write with autoprecharge commands. (CX-9543C, Przybylski Direct Q&A at 24-25, 32-39, 61-63, 188-97, 342-43, 355-58, 407-412, 954-56, 978-80, 999-1000, 1726-27; JX-066C 90:3-7, 122:21-24; JX-110C 112:6-12.) Before a read or write operation can occur on a different row of data than the one present in the sense amplifiers, a precharge operation must occur, which can be initiated via a separate precharge command, or it can be specified to occur automatically after a column operation is completed, such as at the conclusion of a write operation. The latter is known as automatically precharging (or autoprecharging). The mechanism for accomplishing an

autoprecharge in the Accused Autoprecharge Products is for the controller to provide a second code to the memory device when a read or write command is issued. That code is generally provided by signaling HIGH on address line A10. The evidence shows that the Accused WAP Products practice the asserted '405 patent claims for the reasons discussed above in the context of the asserted '353 patent claims. (CX-9543C, Przybylski Direct Q&A 184-197, 338-378, 950-1012, 1723-1733, 400-406, 413-424.)

Respondents' only dispute is that certain of the Accused Barth Products do not use the "write with autoprecharge" and that Rambus has failed to prove that these products infringe on this basis. (RIB at 36-37.) The ALJ finds Respondents' argument irrelevant as Rambus has not asserted that these non-accused products infringe the '405 Patent. (CIB at 25 (separating "products that issue write with autoprecharge commands" from all of the Accused Barth Products.) Thus, Respondents have failed to provide any valid argument as to why the Accused Autoprecharge Products to not meet each and every limitation of claim 11.

Therefore, the ALJ finds that the Accused Autoprecharge Products meet each and every limitation of claim 11.

e) Claims 12 and 13

Claims 12 and 13 of the '405 Patent are similar to claims 12 and 13 of the '353 Patent. The evidence shows that the Accused Autoprecharge Products and are infringed for the same reasons. (CX-9543C at Q&A 198-199, 378-392, 1013-1031, 1733-1737.) Therefore, the ALJ finds that the Accused Autoprecharge Products meet each and every limitation of claims 12 and 13.

f) Claims 15 and 18

Dependent claim 15 recites providing "address information to the memory device." (CX-9543C at 393.) The evidence shows that Accused Autoprecharge Products provide address information to memory devices in the form of bank, row, and column addresses. (CX-9543C at 199-200, 393-396, 1032-1040, 1738-1739; CX-6880C.0083; CX-6879C.0142; JX-144C at 284:25; JX-039C at 123:25-124:4; CX-6572.0004; JX-042C at 66:9-15.)

Dependent claim 18 recites "the plurality of control codes includes a third code which specifies that a row of sense amplifiers be activated." (CX-9543C at 200.) The evidence shows that the Accused Autoprecharge Products provide activate commands to the attached memory device, which includes address information to identify a particular row in a particular bank. That row is then transferred to a set of sense amplifiers. (CX-9543C at 200-201, 397-400, 1040-1046, 1739-1740; CX-6880C.0083, 0021-22; JX-100C 35:18 36:3, 36:16 21, 38:1 3, 38:4 11, 70:2 18; JX-039C 121:16-24; CX-6572C.0004; JX-103C 108:12-20.)

Therefore, the ALJ finds that the Accused Autoprecharge Products meet each and every limitation of claims 15 and 18.

'109 Patent

Rambus asserts that the Accused Barth Products infringe claims 1, 2, 4, 12, 20, 21 and 24 of the '109 Patent. (CIB at 25.) Rambus asserts that the Accused Autoprecharge Products infringe claims 5 and 13 of the '109 Patent. (CIB at 25.) Staff agrees. (SIB at 18-35.) Respondents do not dispute that the Accused Barth Products meet the limitations of the asserted claims of the '109 Patent, except to the extent that they do not meet the '353 and the '405 Patents. (RIB at 29-41.)

The evidence shows the Accused Barth Products infringe claims 1, 2, 4, 12, 20, 21, and 24 of the '109 Patent, and that the Accused Autocharge Products infringe claims 5 and 13 of the '109 patent. (CX-9543C at 202-214, 402-774, 1048-1598, 1741-2122, 2148-2210, 2251-2357.) The analysis as to the '109 Patent is substantially the same as the analysis above with respect to the '353 and '405 Patents. (CX-9543C, Przybylski Direct Q&A 439-481, 554-625, 714-798, 845-884, 912-929, 941-959; Smith, Tr. 920:10-921:23.) The evidence further shows that the Accused Barth Products provide a code that specifies whether to perform a precharge operation (claim 2) and transmitting bank selection information (e.g., claim 4). Specifically, the control information provided by the controllers in each of the Accused Barth Products includes "a third code that specifies whether to perform a precharge operation," as recited in '109 Patent claim 2. (CX-9543C at 206-08, 488-90, 493, 504-8, 1164-66, 1177-81, 1185, 1193-96, 1829-30, 1839-42, 1845-48, 2165, 2283-85; CX-8558C.0009; CX-8566C.0017; JX-066C.044; CX-8593C.0004; CX-7029C.0043.) This feature is found in the Accused Barth Products because they provide automatic precharge commands, standalone precharge commands, or both, which were discussed in connection with the '405 claims. For example, the JEDEC DDR SDRAM Specification provides for a standalone precharge code in its command truth table, which is a table that identifies the signals that must be present on the various signal lines to form the listed commands. (CX-4020.0018.) The precharge command "is used to deactivate the open bank in a particular row or the open row in all banks." *Id.* at 26.

As for "transmitting bank selection information, wherein the bank selection information identifies a bank of the plurality of banks," the evidence shows that that this occurrs on lines

BA0 and BA1 when an active command is sent in the Accused Barth Products.[7] (CX-9543C at 508-551, 1196-1263, 1848-92, 2166-172, 2286-95; CX-4020.0025; CX-6880C.0122-25; CX-6879C.0142; CX-8566C.0017; CX-7051C.0070; CX-6387C.0005; CX-6385C.0107-12; CX-7029C.0043.)

Therefore, the ALJ finds that the Accused Autoprecharge Products meet each and every limitation of the asserted claims of the '109 Patent.

Sufficient Evidence to Prove Direct Infringement

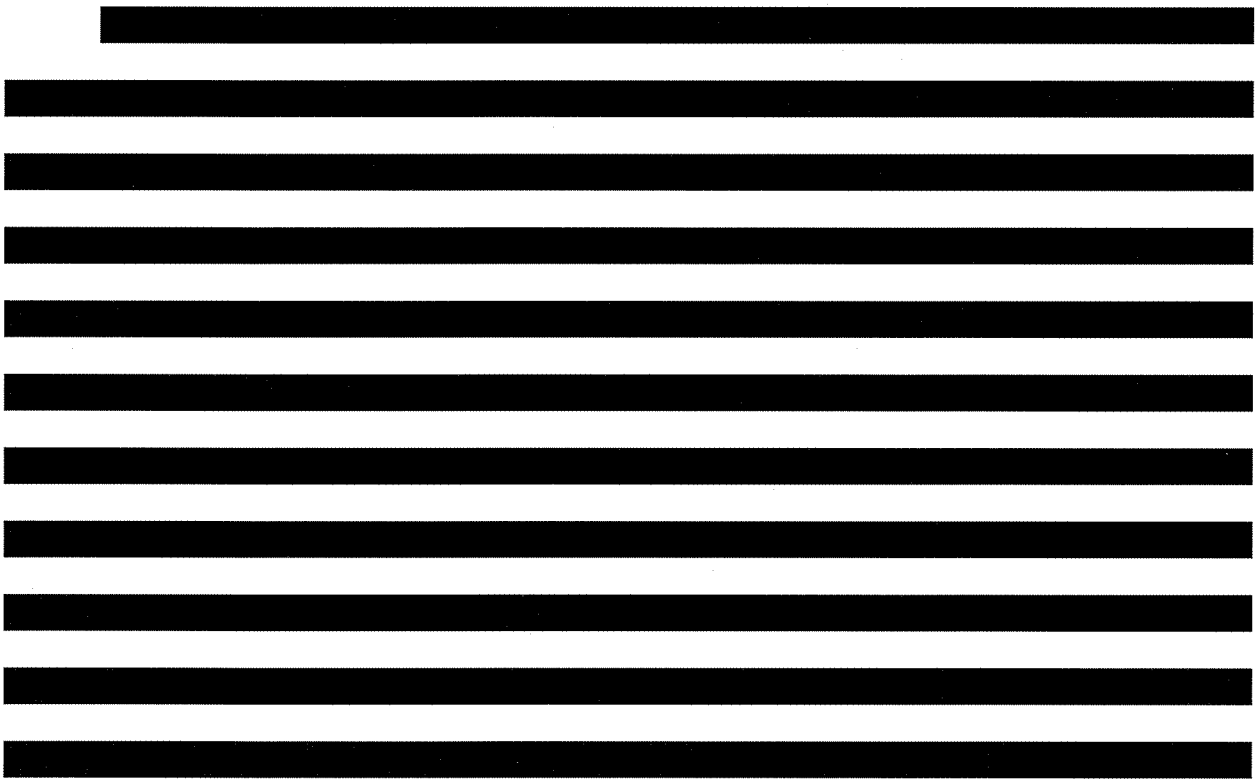
[redacted]

The ALJ finds Respondents' arguments unpersuasive. First, the Accused Barth Products include memory controllers and products containing the same, which include products with memory controllers and memory devices, such as a Tivo, storage adapter, Blu-ray disc player,

[7] It is not disputed that the Accused Products interface with memory devices that have memory cores, i.e., storage area of the memory device that includes memory cells and support circuitry for receiving and performing memory options, such as row decoders, column decoders, and sense amplifiers, or that they have banks. RPB at 80-90; CX-6880C.0122-23; JX-075C at 70:10-71:7; CX-8566C.0017; CX-8593C.0004; CX-8607C.0036; JX-042C at 65:13-14; CX-7029C.0043; CX-9543C at 11-12, 205 (discussing memory cores).

and phone. (CX 9543C.0026-0112.) The evidence shows that these products were purchased in the United States and include both a memory controller and memory devices. (*Id.*) The evidence shows that the Accused Barth Products contain memory controllers that are designed for use and are used with DDR-type memory. (*Id.*)

In addition, the evidence shows that Respondents have extensively sold the Accused Products in the United States. *See* CX-9543C.2370-75; CIB 40-41. Such extensive sales support a finding of direct infringement. *See Lucent Techs., Inc. v. Gateway*, Inc., 580 F.3d 1301, 1318-19 (Fed. Cir. 2009); *Moleculon Research Corp. v. CBS, Inc.*, 793 F.2d 1261, 1272 (Fed. Cir. 1986); 661 ID at 43. The ALJ finds it implausible, nor is there any evidence, that such customers would purchase the products in the United States and never use them here. (CX-9543C.2373-74.)



[redacted]

The ALJ further finds that LSI's argument that Rambus cannot show infringement by the LSI 3Ware products because it "has not presented a limitation-by-limitation infringement analysis for any of these products" to be unpersuasive. The evidence shows that the Accused Barth Products are used in conjunction with JEDEC-complaint memory devices and, as standardized products, operate in substantially the same way for infringement purposes. (Jacobs, Tr. 1045:08-17; Smith, Tr. 897:02-20, 900:04-901:02.) Thus, Rambus need not provide a detailed product-by-product infringement analysis to show infringement of certain asserted claims to the extent that they practice the JEDEC industry standard. *See Fujitsu Ltd. v. Netgear, Inc.*, 620 F.3d 1321, 1327 (Fed. Cir. 2010) ("We hold that a district court may rely on an industry standard in analyzing infringement. If a district court construes the claims and finds that the reach of the claims includes any device that practices a standard, then this can be sufficient for a finding of infringement.").

[redacted]

Contributory and Induced Infringement

Rambus argues that Respondents induce or contribute to the direct infringement of others within the United States. (CIB at 42-44.) Staff agrees. (SIB at 28-35.) Respondents argue that they do not contributorily infringe because there is no evidence that Respondents "knew that the combination for which its components were especially made were both patented and infringed" and Rambus has failed to show that there are no substantial non-infringing uses. (RIB at 39-40.) Respondent further argue that they do not induce infringement because there is no evidence that any Respondent possesses the requisite intent for inducement or that the Supplier Respondents solicit or encourage their customers to infringe. (RIB at 40-41.)

As set forth *supra*, all of the Accused Barth Products infringe the asserted claims of the '353, '405 and the '109 Patent. The ALJ further finds that the Respondents induce or contribute to the direct infringement of others, such as end users of their products, within the United States.

The evidence shows that Respondents have induced infringement. Respondents' knowledge of the Asserted Patents cannot be disputed since they have had notice since at least December of 2010, when the Complaint in this Investigation was filed. (*See,* CX-10856C.0001; CX-8173C.0003; Garmin Stip at 4; ASUS Stip at 2; MSI Stip at 2; Biostar Stip at 2; ECS Stip at 1; Galaxy Stip at 2; Pine Stip at 2; Sparkle Stip at 2; EVGA Stip at 2; Gigabyte Stip at 2; HP Stip at 1; Jaton Stip at 2; Palit Stip at 1; Zotac Stip at 2; Motorola Stip at ¶7; Hitachi Stip at 3.) *See Certain Inkjet Ink Cartridges With Printheads And Components Thereof*, Inv. No. 337-TA-723, Initial Determination, 2011 ITC LEXIS 1503 at *145 (June 10, 2011) (unreviewed in relevant part) (finding knowledge requirement for contributory infringement satisfied based on service of

the complaint). In addition to the Complaint, the evidence shows that certain of the Barth I Respondents were made aware of the Asserted Patents during licensing negotiations. (*See infra* Section XIV.) Furthermore, the issuance of the Final Initial Determination on Violation in *Certain Semiconductor Chips Having Synchronous Dynamic Random Access Memory Controllers and Products Containing Same,* Inv. No. 337-TA-661 also put the Respondents on notice of infringement by Respondent nVidia and its named customers. (*See* Public Version of 661 ID, EDIS Doc. ID 423948 at 20-31, 41-44.)

Despite having notice of the Asserted Patents and their infringement, none of the Respondents has stopped selling the Accused Products or made any design changes to avoid infringement. (CX-9543C at 2383, 2386-88, 76; CX-8173C.0003. *See Ricoh*, 550 F.3d at 1343 ("a failure to remove or diminish infringing features of a distributed product is relevant to a party's intent that those features be used for direct infringement").) The Barth I Respondents have nonetheless taken active steps demonstrating a specific intent to induce infringement, such as advertising the infringing use and providing technical support, instructions, tutorials, software device drivers and other materials directing end users to operate the Accused Products in an infringing manner. (CX-9543C, Przybylski Direct Q&A 982-992, 994-998, 1000, 2374-88; CX-9543C at 2374-88; JX-044C at 32:8-33:6; JX-072C at 62:8-20; JX-016C at 131:7-138:8; JX-080C at 95:17-22; JX-042C at 214:23-215:23; CX-10856C.0002; CX-8173C.0003; Garmin Stip at 4; ASUS Stip at 2; MSI Stip at 2; Biostar Stip at 2; ECS Stip at 2; Galaxy Stip at 2; Pine Stip at 2; Sparkle Stip at 2; EVGA Stip at 2; Gigabyte Stip at 2; HP Stip at 2; Jaton Stip at 2; Palit Stip at 2; Zotac Stip at 2; Hitachi Stip at 4.) Therefore, the ALJ finds that these actions induce infringement and demonstrate Respondents' intent to encourage infringement by end-users.

Respondents also contribute to infringement by end-users. The evidence shows that the Respondents had specific knowledge of the asserted Barth Patents and Complainant's infringement allegations at least as of the filing of the Complaint on December 1, 2010. The evidence further shows that there are no substantial non-infringing uses. The only way to use the Accused Barth Products is in a manner that infringes the asserted claims since all of the Accused Barth Products use a data strobe in the manner claimed in the Barth Patents and will not operate without the remaining claimed features.[8] (CX-9543C at 1002-1013, 2388-93; JX-135C at 136:14-19; JX-016C at 98:25-99:4.) Furthermore, the manuals provided by Respondents list only a single, infringing method of use.[9] (*Id.*)

Respondents have known of their infringement since at least December 2010. Yet they have taken no actions to change how their products work and have not stopped distribution or sale of the Accused Products, which have no substantial noninfringing uses. (CX-9543C at 2383, 2386-93, 76; CX-8173C.0003.) Respondents thus contribute to direct infringement by end-users.

As for Respondents' argument that the Accused Products are capable of substantial non-infringing uses because they perform both read and write operations, the evidence shows that the Accused Products must issue write commands or there will be no data to read. (CX-9543C at Q&A 1010, 2391.) In fact, Respondents have not alleged that their controllers do not issue write commands and the Accused Products cannot operate without writing to a memory device. (*Id.*)

Therefore, the ALJ finds that the Accused Barth Products directly and indirectly infringe the asserted claims of Barth Patents.

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[8] The Customer Respondents do not alter the way the memory controllers of the Primary Respondents operate when incorporating those controllers into their products. (CX-9543C at 76, 78-79, 2386; CX-10863C.0002; CX-10763C.0001; CX-8173C.0003.)

[9] Respondents identify Seagate chips that can operate with SDR (RPB at 98), but when those products are set up to operate with DDR, they cannot instead operate with SDR, nor can the customer change the chips to operate with SDR. HTr. 1202.

C. The Dally Patents

The Asserted Claims can be divided into three groups, as discussed below, the ALJ finds that the evidence demonstrates that each Accused Dally Product infringes one or more groups of claims. (CX-9542C.0063-473).

Asserted Claims	Infringing Products
'857 patent claims 1, 4-6, 9, 10, 24-28, 35, 36, 39-44, 47, and 53 '494 patent claims 1, 2, 6, 8, 25, 30, 39, and 42	All Accused Dally Products
'857 patent claims 11-13, 32-34, and 50-52 '494 patent claims 26 and 40	Accused Dally Products with multiple transmitters
'857 patent claims 2, 31, and 49 '494 patent claim 3	Accused Dally Products able to output data at 2 Gb/s or greater

[redacted]

The Accused Products Infringe the Independent Claims of the Dally Patents

The ALJ finds that the Accused Products have all of the features recited in the asserted independent claims.

a) "A Component Comprising a Semiconductor Chip"

Independent claims 1, 24, 35, and 39 of the '857 Patent each recite "[a] component comprising: a semiconductor chip." Independent claims 1, 25, and 39 of the '494 patent also

recite a semiconductor chip or an integrated circuit. Rambus and Staff contend that all of the accused products meet this limitation. Respondents do not dispute that their products meet this limitation. Indeed, Respondents' experts concede that the Accused Products include these features. (Tr. 1471:14-17, 1584:23-25.) The evidence shows that all of Respondents' accused Products are semiconductor chips. (CX-9542C at Q/A 204-206, 234-237; JX-68C; CX-4055.0005 (LSI); CX-4087.0004 (ST Micro)).)

(a) "A Processor Within the Chip" and "A Component Circuit Within the Chip"

Independent claim 1 of the '857 Patent recites "a processor within a chip." Independent claims 24, 35, and 39 similarly recite "a component circuit within the chip." The ALJ finds that the evidence shows that Respondents' Accused Dally Products include a processor or component circuit within the chip. (CX-9542C at Q/A 57, 63, 69, 72, 149-155, 207-209, 238-242.) Moreover, the relevant PCI Express, DisplayPort, SATA, and SAS standards all require the use of an 8b/10b encoder. (CX-4027.0152.) For example, the Accused Dally Products all include an 8b/10b encoder or analogous circuitry. (Tr. 1470:17-23; RX-5506C; JX-68C at 82:2-83:05; JX-95C at 118:05-21.) Because an 8b/10b encoder includes circuitry for processing data, *i.e.*, to perform the encoding function thereof, it literally meets the proposed constructions of this term. (*See* CX-9542C at Q/A 154-155; Tr. 1470:20-1471:21.) Respondents do not challenge that their Accused Dally Products include these elements. (*See* Tr. 1470:20-1471:21, 1587:3-15.)

b) "A Transmitter Circuit Within the Chip"

Independent claims 1, 24, 35, and 39 of the '857 Patent and claims 1 and 25 of the '494 Patent each recite "a transmitter circuit within the chip." Independent claim 39 of the '494 Patent similarly recites "an integrated circuit having a transmitter." The ALJ finds that the

evidence shows that each of the Accused Dally Products includes a transmitter circuit or transmitter within the chip within the plain and ordinary meaning as construed by the ALJ. (CX-9542C at Q/A 210-222; 248-254; Tr. 1461:22-1464:06; 1588:14-20.) Respondents contested this element, but only based on the rejected construction proposed by Dr. Hassoun. Accordingly, this element is present in the Accused Dally Products.

c) Transmitter Circuit Coupled to a Processor or Component Circuit

Independent claim 1 of the '857 Patent recites "the transmitter circuit being coupled to the processor to accept a digital input signal including a plurality of digital values from the processor." Claims 24, 35, and 39 recite similar features but in relation to coupling the transmitter circuit to the claimed "component circuit." The ALJ finds that the evidence shows that Respondents' Accused Dally Products include these features. (CX-9542C at Q/A 210-222; 248-254; Tr. 1461:22-1464:06; 1588:14-20.) Moreover, the ALJ finds that the relevant standards require that the Accused Dally Products include a transmitter circuit within the chip. (CX-4027.0202; CX-4029.0242; CX-9368.0024; CX-4033.0166; CX-4036.0082.)

As discussed above, the Accused Dally Products use 8b/10b encoding. The ALJ finds that the transmitter circuits in the Accused Dally Products receive a parallel digital input signal with a plurality of digital values or bit values from the 8b/10b or similar encoder. (*See e.g.*, JX-144C.0022 at 61:4-8; CX-7398C.0010-11.) The ALJ finds that the transmitter serializes the values before transmitting them, and, as a result, the processor or component circuit must be coupled to the transmitter circuit to provide the input signal for transmission. (CX-4027.0152. *See e.g.*, JX-144C.0022-23 at 61:12-62:13; JX-81C.0020 at 59:4-60:3; JX-68C.0026 at 98:8-99:18; CX-6610C.0044; CX-7398C.0010-11.)

d) Transmitter Circuit Operable to Send an Output Signal

Independent claims 1, 24, and 35 of the '857 Patent each recite "the transmitter circuit being operable to send an output signal including a series of signal levels representing the digital values and to emphasize high frequency components of the output signal relative to low frequency components of the output signal." Independent claim 39 of the '857 Patent and independent claims 1, 25, and 39 of the '494 Patent also recite similar limitations directed to sending an output signal. The ALJ finds that the evidence shows that in Respondents' Accused Dally Products, the transmitter circuit is operable to send an output signal as claimed. (CX-9542C at Q/A 162-172, 221-224, 255-257.) Respondents do not appear to dispute that this limitation is met.[10] (Ozguc, Tr. 1187:09-11, 1187:16-23, 1188:05-1190:23, 1192:13-23 (Ozguc);Tr. 1465:08-1467:10, 1469:22-1470:06 (Hassoun); JX-068C at 80:11-81:18 (Kobayashi).)

The ALJ also finds that the relevant standards require that the transmitter circuits in the Accused Dally Products send output signals that include a series of signal levels representing the digital values as claimed. As an example, the PCI Express standards require devices to send an output signal including a series of signal levels. The signal levels represent the digital values provided to the transmitter. (*See e.g.*, CX-4029.0169 (illustrating that the transmitter outputs data serially).) The PCI Express standards also show that the transmitters emphasize high-frequency components of the output signal relative to low-frequency components of the output signal. (*Id.* at 255.) All PCI Express 2.0 transmitters support this type of signal de-emphasis.

[redacted]

(*See e.g.*, CX-4029.0169, 255.) The ALJ finds that the evidence also shows that for the Accused Dally Products that operate in accordance with other relevant standards, the transmitter circuit is operable to send an output signal including a series of signal levels representing the digital values and to emphasize high-frequency components of the output signal relative to low-frequency components of the output signal. (CX-9542C at Q/A 171.)

As Rambus correctly notes, independent claim 1, 25, and 39 of the '494 Patent also requires the transmitter circuit to generate a sign and a magnitude, with its output bit signal having a sign and magnitude. The ALJ finds that evidence shows that the transmitter circuits in each of the Accused Dally Products generate a differential output signal that has both a sign and a magnitude. (CX-9542C at Q/A 430-438; CX-6841C; JX-144C.0026 at 74:21-75:4; JX-144C.0031 at 95:12-96:8; JX-95C.0018 at 62:20-63:4; JX-117C.0024 at 83:9-84:21; CX-6610C.0044; JX-68C.0017 at 63:12-21; JX-68C.0021 at 80:11-24; JX-102C.0024 at 77:8-24; CX-6815C.0090.)

Cisco raises the argument that certain of its accused products do not infringe because the accused interface is not connected to anything within the accused product. (RIB at 133.) Cisco argues that there can be no infringement because "[w]ith these downstream products, the products cannot practice the accused standard because the interface is not used in the accused end product." (RIB at 133.) However, the ALJ agrees with Staff and Rambus that merely stating that they are "not connected" without further detail, is not evidence that the interface is permanently disabled. (CRB at 106; SIB at 153.) Moreover, as Rambus notes, Cisco has

e) Sending Output Signals with Emphasis

Claims 1 and 39 of the '857 Patent recite a transmitter circuit sending an output signal so that "(i) an output bit signal of the output signal representing a particular bit value has one signal level when the bit value is the same as a bit value represented by a predetermined preceding output bit signal; and (ii) the output bit signal representing the particular bit value has another signal level when the bit value is different from the bit value represented by the predetermined preceding output bit signal." Independent claims 24 and 35 of the '857 Patent and independent claims 1, 25, and 39 of the '494 Patent also recite similar limitations. The ALJ finds that the evidence shows that the Accused Dally Products include these "Output Signals with Emphasis" features these claims. (CX-9542C at Q/A 0099-104, 124-37, 181-87, 237-58.)

f) ST Microelectronics

[redacted]

[redacted]

g) LSI

The ALJ finds that the evidence shows that LSI's Accused Products include the claimed Output Signals with Emphasis, as required by the independent claims of the '857 and '494 Patents. (*See* CX-9542C at Q/A 258-261.) [redacted]

[redacted]

The ALJ finds that the record fails to support LSI's arguments in this regard.

The ALJ agrees with Staff and Rambus that neither of these arguments has any support. First, as Staff points out, documentation from LSI contradicts its position that [redacted]

[redacted] The ALJ finds that this evidence confirms the position of Rambus and the Staff that

LSI's [redacted] products operate as an infringing [redacted] product when [redacted]

As for LSI's second argument, the ALJ notes that LSI fails to recognize that the asserted claims of the Dally patents are apparatus claims, not method claims. The law is clear that Rambus need not show actual use of [redacted] to demonstrate infringement of the asserted apparatus claims. Rather, Rambus need only show that the [redacted] are designed for operation in an infringing [redacted] and that users of those products can enable the [redacted] mode without having to modify the product in question. *See Silicon Graphics, Inc. v. ATI Techs., Inc.*, 607 F.3d 784, 794 (Fed. Cir. 2010) (quoting *Fantasy Sports Props., Inc. v. Sportsline.com, Inc.*, 287 F.3d 1108, 1118 (Fed. Cir. 2002) (holding infringement of an apparatus claim occurs "so long as the product is designed 'in such a way as to enable a user of that [product] to utilize the function . . . without having to modify [the product].'")). LSI admits that such a showing has indeed been made. [redacted]

In its reply brief, LSI attempts to argue for [redacted] implementations that [redacted] takes LSI's [redacted] outside the assert Dally claims." (RRB at 65.) [redacted] Thus, the ALJ finds that this [redacted] has no impact on the output signal level. (*See* Tr. 1421:9-1422:1; 1437:7-1438:18; CX-9542C at Q/A 53.) [redacted]

[redacted] (CX-9542C at Q/A 47-53; Tr. 1437:7-1438:18; 1421:9-1422:1.) Accordingly, the ALJ finds that this is within the scope of the asserted claims of the Dally patents.

The Accused Products Infringe the Dependent Claims of the '857 and '494 Patents

The ALJ finds that the evidence further shows that the Accused Dally Products infringe dependent claims 2, 4, 5, 6, 9, 10-13, 25-28, 31-34, 36, 40-44, 47, 49-53 of the '857 Patent. The Accused Dally Products also infringe dependent claims 2, 3, 6, 8, 26, 30, 40 and 42 of the '494 Patent.

Dependent claims 2, 31, and 49 of the '857 Patent all require that "the transmitter circuit is operable to send the output signal with an output frequency of at least 1 GHz and a bandwidth greater than 100 MHz." Claim 3 of the '494 Patent recites similar features. The ALJ finds that the Accused Dally Products that output data at a rate of at least 2 Gb/s satisfy these claims. CX-9542C at Q/A 92-96, 103-104.) Indeed, the ALJ notes that the relevant PCI express standards all require a data rate of at least 2 Gb/s for each output. (*See*. CX-9542C at Q/A 263.) The ALJ also finds that Respondents' witnesses and documents also confirm that many of the Accused Dally Products operate at these speeds. (JX-094C.0023 at 81:13-17; JX-137C.0043 at 147:5-148:4; JX-137C.0047 at 163:3-16; JX-56C.0021 at 71:4-6; CX-9104C.0001-2; CX-9105C.0001.) Respondents have not disputed that their Accused Dally Products that output data at a rate of at least 2 Gb/s include the features recited in these claims.

Dependent claims 4, 9, 10, 26, 41, 42, 47, and 53 of the '857 Patent and claims 2 and 6 of the '494 Patent each recite features related to the previously discussed output-signals-with-emphasis features of the claims. The ALJ finds that the same evidence showing that the Accused

Dally Products have those features, discussed above also demonstrates that the Accused Dally Products include the features of these claims. (*See* CX-9542C at Q/A 273-275.)

Dependent claim 11 of the '857 Patent recites that the component circuit includes "at least one additional transmitter circuit within the chip, each additional transmitter circuit being coupled to the processor and operable to accept an additional digital input signal from the processor and send an additional output signal representing such additional input signal." Dependent claims 32 and 50 of the '857 Patent recite similar limitations. The ALJ finds that the evidence shows that many of the Accused Dally Products include additional transmitter circuits such that they contain these claimed features. (*See* CX-9542C at Q/A 294-295, 298-306.) In addition, the ALJ finds that Respondents' documents and witnesses confirm that many of the Accused Dally Products contain multiple transmitter circuits. (*See* JX-144C.0038 at 124:4-13; JX-144C.0046 at 156:3-10; CX-6847C.0005; CX-6848C.0004; CX-6849C.0003; JX-95C.0028 at 115:10-21; JX-117C.0018 at 58:8-9; CX-6349C.0021; CX-9208C.0008.)

Dependent claims 5, 27, and 43 of the '857 Patent recite that "the chip has I/O connections and the transmitter circuit is coupled to one or more of the I/O connections to send the output signal through one or more I/O connections." The ALJ finds that the evidence shows that the Accused Dally Products include a number of different types of I/O connections, such as PCI Express, SATA, or SAS, as well as memory controller and other I/O connections. (*See* CX-9542C at Q/A 276-277.) In addition, by virtue of having one or more of these I/O connections, the transmitter circuits in each of the Accused Dally Products is coupled to one or more of those I/O connections. (*Id.*)

Dependent claims 12, 33, and 51 of the '857 Patent, which depend on claims that require multiple transmitters, recite that "the chip has I/O connections and the transmitter circuits are

coupled to a plurality of the I/O connections and operable to send the output signals through the I/O connections." The ALJ finds that the same evidence discussed above with respect to claims 5, 27, and 43 of the '857 Patent shows that the Accused Dally Products with multiple transmitters include the features of dependent claims 12, 33, and 51 of the '857 Patent. (*See* CX-9542C at Q/A 307-309.)

Dependent claims 6, 28, and 44 of the '857 Patent recite that "the transmitter circuit is operable to send the output signals in a nonmodulated form." The ALJ finds that the evidence shows that the relevant PCI Express, DisplayPort, SATA, and SAS standards all require signals to be sent in nonmodulated form. (*See* CX-9542C at 279-280.) The ALJ also finds that Respondents' documents and witnesses confirm that the transmitter circuits in the Accused Dally Products are operable to send the output signal in a nonmodulated form. (*See* CX-9542C at Q/A 283-286; JX-144C.0032 at 100:6-12; CX-6841C; CX-6844C, CX-6847C - CX-6864C; CX-7398C.0013; JX-137C.00130-31 at 535:20-538:2; JX-094C.0024 at 82:15-83:3; CX-6401C.0011; CX-6946C.0011; CX-6610C.0046; CX-9229C.0017; CX-6408C.0018.)

Claim 13 of the '857 Patent recites that "the transmitter circuits are operable to provide output signals representing a parallel stream of data from the processor." Claims 34 and 52 of the '857 Patent similarly recite that "the transmitter circuits are operable to provide output signals representing a parallel stream of data from the component circuit." The ALJ finds that the evidence shows that many of the Accused Dally Products include the features of dependent claims 13, 34, and 52 of the '857 Patent. (*See* CX-9542C at Q/A 310-320.) The ALJ finds that the same evidence showing that "[t]he transmitter circuit being coupled to the processor to accept a digital input signal including a plurality of digital values from the processor" of '857 Patent claim 1 also shows that many of the Accused Dally Products include the features of claims 13,

34, and 52 of the '857 Patent. In addition, the ALJ finds that Respondents' documents and witnesses confirm that many of the Accused Dally Products include these features. (*See* CX-9542C at Q/A 310-320; JX-144C.0022-23 at 61:12-62:13; CX-6844C; JX-95C.0030 at 123:15-125:19; JX-117C.0026 at 91:9-92:7; CX-6610C.0044; CX-6406C.0008-09; CX-6408C.0009-10; JX-68C.0026 at 98:11-99:18.)

Dependent claims 25, 36, and 40 of the '857 Patent each recite that the "component circuit is a processor." The ALJ finds that the same evidence showing that the Accused Dally Products include "a processor within the chip" as recited in '857 Patent claim 1 shows that the Accused Dally Products have this claimed feature. *See* CX-9542C at Q/A 356-358.)

[redacted]

Dependent claims 26 and 40 of the '494 Patent recite that the chip "includes plural of said transmitter circuits [or transmitters]" and that each transmitter circuit or transmitter outputs "a respective series of output bit signals on [respective] lines of a parallel bus." The ALJ notes that these claims are similar to claims 11 and 13 of the '857 Patent. The same evidence showing that the Accused Dally Products include the features of those claims also demonstrates that the Accused Products include the features of claims 26 and 40 of the '494 Patent. (*See* CX-9542C at Q/A 464.)

Dependent claims 30 and 42 of the '494 Patent both recite that "the series of output signals" be transmitted by the "transmitter onto a signal path at a rate of at least 400 megahertz." The ALJ notes under the ALJ's construction that a rate of 400 megahertz corresponds to a rate of 400 Mb/s. All Accused Dally Products with PCI Express, DisplayPort, SATA, and SAS interfaces meet this claim requirement, and the same evidence discussed with respect to claim 2 of the '857 Patent showing that the Accused Dally Products operate at speeds of at least 2 Gb/s also demonstrates that the Accused Dally Products include the features of these claims. (*See* CX-9542C at Q/A 465.)

Respondents Directly and Indirectly Infringe the Dally Patents

[redacted]

stores, and/or testing them to ensure proper operation. (CX-8173C; CX-10763C; CX-10863C; CX-9027C.0007-9; JX-26C.0017 at 57:16-24; JX-24C.0028 at 94:20-95:6; JX-28C.0022 at 93:7-14; JX-50C.0033 at 127:21-128:4; JX-62C.0025 at 90:5-17; JX-133C.0029 at 98:11-17; JX-139C.0024 at 86:7-24.)

End-users of the Accused Dally Products also always directly infringe the asserted apparatus claims. (CX-9542C.0498.) The high volume of products that Respondents import into the United States (CX-9542C.0498-500), indicates that end-users do in fact use the products in the United States and thus directly infringe the Asserted Claims. *Lucent Techs. v. Gateway, Inc.*, 580 F.3d 1301,1318-19 (Fed. Cir. 2009); *Moleculon*, 793 F.2d at 1272.

[redacted]

December 2010, yet there is no evidence that any of them have changed their practices since that time. (*Id. Broadcom*, 543 F.3d at 699-700.

Respondents LSI and Seagate also assert that "Rambus has failed to prove infringement with respect to LSI and Seagate products because its expert, [Dr.] Singer failed to evaluate the issue of infringement in relation to each and every limitation of the Asserted Claims of the Dally Patents." (RIB at 139.) LSI and Seagate raise several specific complaints. The ALJ finds these arguments to be frivolous. First, they complain that Dr. Singer only performed his analysis on the LSI SerDes core – a functional circuit block that is incorporated into an integrated circuit. (RIB at 139.) LSI and Seagate argue that "[e]ach of the asserted claims of the Dally Patents requires a 'semiconductor chip' and various components are required to be on the chip." Based on this, LSI and Seagate conclude that "an appropriate infringement analysis requires evaluation of a SerDes core in the context of the semiconductor chip." (RIB at 139.) It is beyond any doubt that the SerDes cores are intended to incorporated into a semiconductor chip. The SerDes cores include the essential circuitry relevant to the issues at hand. Unless LSI and Seagate identified specific elements of the claims where Rambus's analysis is lacking, the ALJ is not going to consider their broadside assault on Rambus's analysis.

Second, LSI and Seagate complain that Dr. Singer did not analyze every one of the hundreds of products at issue in this investigation. However, Dr. Singer testified he relied on testimony by LSI witnesses that the products operated in the same fashion and proceeded accordingly. There is nothing wrong with this approach. *See TiVo, Inc. v. Echostar Comm'ns Corp.*, 516 F.3d 1290, 1308 (Fed. Cir. 2008) ("there is nothing improper about an expert testifying in detail about a particular device and then stating that the same analysis applies to other allegedly infringing devices that operate similarly"). LSI complains that these witnesses

were not corporate representatives. But there is no requirement that the deposition testimony be disregarded for infringement purposes because she is not a corporate witness and LSI points to no reason why the ALJ should disregard her testimony. *See Martek Biosciences Corp. v. Nutrinova, Inc.*, 579 F.3d 1363, 1372 (Fed. Cir. 2009) ("A patentee may prove infringement by any method of analysis that is probative to the fact of infringement") (internal quotation marks omitted). Accordingly, LSI's and Seagate's arguments are rejected.

VI. VALIDITY

A. Background

One cannot be held liable for practicing an invalid patent claim. *See Pandrol USA, LP v. AirBoss Railway Prods., Inc.*, 320 F.3d 1354, 1365 (Fed. Cir. 2003). However, the claims of a patent are presumed to be valid. 35 U.S.C. § 282; *DMI Inc. v. Deere & Co.*, 802 F.2d 421 (Fed. Cir. 1986). Although a complainant has the burden of proving a violation of section 337, it can rely on this presumption of validity.

Respondents have the burden of overcoming the presumption that the asserted patents are valid and must prove invalidity by clear and convincing evidence in order to do so. *Technology Licensing Corp. v. Videotek, Inc.*, 545 F.3d 1316, 1327 (Fed. Cir. 2008) (stating, "When an alleged infringer attacks the validity of an issued patent, [the] well-established law places the burden of persuasion on the attacker to *prove invalidity by clear and convincing evidence*." (emphasis added)); *see also Checkpoint Systems, Inc. v. United States Int'l Trade Comm'n*, 54 F.3d 756, 761 (Fed. Cir. 1995). Respondents' burden of persuasion *never shifts* to Rambus; the risk of "decisional uncertainty" remains on the respondent. *Id.*; *see also PowerOasis, Inc. v. T-Mobile USA, Inc.*, 522 F.3d 1299, 1303, 1305 (Fed. Cir. 2008); *Pfizer, Inc. v. Apotex, Inc.*, 480 F.3d 1348, 1360 (Fed. Cir. 2007). Thus, it is Respondents' burden to prove by clear and

convincing evidence that any of the alleged prior art references anticipate or render obvious the asserted claims of the patents in suit. Failure to do so means that Respondents loses on this point. *Id.* (stating, "[I]f the fact trier of the issue is left uncertain, the party with the burden [of persuasion] loses.").

Respondents also bears the burden of going forward with evidence, *i.e.*, the burden of production. *Id.* This is "a shifting burden the allocation of which depends on where in the process of a trial the issue arises." *Id.* However, this burden does not shift until a respondent presents "evidence that might lead to a conclusion of invalidity." *Pfizer*, 480 F.3d at 1360. Once a respondent "has presented a prima facie case of invalidity, the patentee has the burden of going forward with rebuttal evidence." *Id.*

B. Anticipation

A patent may be found invalid as anticipated under 35 U.S.C. § 102(a) if "the invention was known or used by others in this country, or patented or described in a printed publication in this country, or patented or described in a printed publication in a foreign country, before the invention thereof by the applicant for patent." 35 U.S.C. § 102(a). A patent may be found invalid as anticipated under 35 U.S.C. § 102(b) if "the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of the application for patent in the United States." 35 U.S.C. § 102(b). Under 35 U.S.C. § 102(e), a patent is invalid as anticipated if "the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent." 35 U.S.C. § 102(e). Anticipation is a question of fact. *Texas Instruments, Inc. v. U.S. Int'l Trade Comm'n*, 988 F.2d 1165, 1177 (Fed. Cir. 1993) ("*Texas Instruments II*"). Anticipation is a two-step inquiry: first, the claims of the

asserted patent must be properly construed, and then the construed claims must be compared to the alleged prior art reference. *See, e.g., Medichem, S.A. v. Rolabo, S.L.*, 353 F.3d 928, 933 (Fed. Cir. 2003). It is axiomatic that claims are construed the same way for both invalidity and infringement. *W.L. Gore v. Garlock, Inc.,* 842 F.2d 1275, 1279 (Fed. Cir. 2008.)

"Claimed subject matter is 'anticipated' when it is not new; that is, when it was previously known. Invalidation on this ground requires that *every element and limitation* of the claim was *previously described in a single prior art reference*, either *expressly or inherently*, so as to place a person of ordinary skill in possession of the invention." *Sanofi-Synthelabo v. Apotex, Inc.*, 550 F.3d 1075, 1082 (Fed. Cir. 2008) (emphasis added) (citing *Schering Corp. v. Geneva Pharms., Inc.*, 339 F.3d 1373, 1379 (Fed. Cir. 2003) and *Continental Can Co. USA v. Monsanto Co.*, 948 F.2d 1264, 1267-69 (Fed. Cir. 1991)).

To anticipate, a single prior art reference must be enabling and it must describe the claimed invention, *i.e.*, a person of ordinary skill in the field of the invention must be able to practice the subject matter of the patent based on the prior art reference without undue experimentation. *Sanofi*, 550 F.3d at 1082. The presence in said reference of *both* a specific description and enablement of the subject matter at issue are required. *Id.* at 1083.

To anticipate, a prior art reference also must disclose all elements of the claim within the four corners of said reference. *Net MoneyIN, Inc. v. VeriSign, Inc.*, 545 F.3d 1359, 1369 (Fed. Cir. 2008) ("*NMI*"); *see also Abbott Labs. v. Sandoz, Inc.*, 544 F.3d 1341, 1345 (Fed. Cir. 2007) (stating, "Anticipation is established by documentary evidence, and requires that every claim element and limitation is set forth in a single prior art reference, in the same form and order as in the claim."). Further, "[b]ecause the hallmark of anticipation is prior invention, the prior art reference--in order to anticipate under 35 U.S.C. § 102--must not only disclose all elements of

the claim within the four corners of the document, but must also disclose those elements 'arranged as in the claim.'" *Id.* (quoting *Connell v. Sears, Roebuck & Co.*, 722 F.2d 1542, 1548 (Fed. Cir. 1983)). The Federal Circuit explained this requirement as follows:

> The meaning of the expression 'arranged as in the claim' is readily understood in relation to claims drawn to things such as ingredients mixed in some claimed order. In such instances, a reference that discloses all of the claimed ingredients, but not in the order claimed, would not anticipate, because the reference would be missing any disclosure of the limitations of the claimed invention 'arranged as in the claim.' But the 'arranged as in the claim' requirement is not limited to such a narrow set of 'order of limitations' claims. Rather, *our precedent informs that the 'arranged as in the claim' requirement applies to all claims and refers to the need for an anticipatory reference to show all of the limitations of the claims arranged or combined in the same way as recited in the claims, not merely in a particular order*. The test is thus more accurately understood to mean 'arranged or combined in the same way as in the claim.'

Id. at 1370 (emphasis added). Therefore, it is not enough for anticipation that a prior art reference simply contains all of the separate elements of the claimed invention. *Id.* at 1370-71 (stating that "*it is not enough [for anticipation] that the prior art reference discloses part of the claimed invention, which an ordinary artisan might supplement to make the whole*, or that it includes multiple, distinct teachings that the artisan might somehow combine to achieve the claimed invention." (emphasis added)). Those elements must be arranged or combined in said reference in the same way as they are in the patent claim.

If a prior art reference does not expressly set forth a particular claim element, it still may anticipate the claim if the missing element is inherently disclosed by said reference. *Trintec Indus., Inc. v. Top-U.S.A. Corp.*, 295 F.3d 1292, 1295 (Fed. Cir. 2002); *In re Robertson*, 169 F.3d 743, 745 (Fed. Cir. 1999). Inherent anticipation occurs when "the missing descriptive material is 'necessarily present,' not merely probably or possibly present, in the prior art." *(Id.)*; *see also Rhino Assocs. v. Berg Mfg. & Sales Corp.*, 482 F. Supp.2d 537, 551 (M.D. Pa. 2007). In

other words, inherency may not be established by probabilities or possibilities. *See Continental Can*, 948 F.2d at 1268. Thus, "[t]he mere fact that a certain thing may result from a given set of circumstances is not sufficient." *Id.*

The critical question for inherent anticipation here is whether, as a matter of fact, practicing an alleged prior art reference necessarily features or results in each and every limitation of the asserted claim at issue. *See, e.g., Toro Co. v. Deere & Co.*, 355 F.3d 1313, 1320 (Fed. Cir. 2004). Such is the case even if one of ordinary skill in the art would not have recognized said inherent anticipation at the time of the invention of the '829 Patent. *Id.* at 1320-21.

If there are "slight differences" between separate elements disclosed in a prior art reference and the claimed invention, those differences "invoke the question of obviousness, not anticipation." *NMI*, 545 F.3d at 1071; *see also Trintec*, 295 F.3d at 1296 (finding no anticipation and stating that "the difference between a printer and a photocopier may be minimal and obvious to those of skill in this art. Nevertheless, obviousness is not inherent anticipation."). Statements such as "one of ordinary skill may, in reliance on the prior art, complete the work required for the invention," and that "it is sufficient for an anticipation if the general aspects are the same and the differences in minor matters is only such as would suggest itself to one of ordinary skill in the art," *actually relate to obviousness*, not anticipation. *Connell*, 722 F.2d at 1548; *see infra.*

The Barth I Patents

Respondents argue that certain of the asserted claims of the '353 and the '109 Patents are anticipated by the following references: (1) Japanese Patent Publication No. 3-276344 ("Yano"); (2) European Patent Application No. 94304672.2 ("Dan"); (3) the NextBus Specification ("NextBus"); (4) U.S. Patent No. 5,313,624 ("Harriman"); (5) U.S. Patent No. 5,218,684

("Hayes"); (6) U.S. Patent No. 6,584,037 ("Farmwald"); and (7) the SyncLink draft IEEE Standard ("SyncLink").[11] (RIB at 43.)

a) Yano

Respondents argue that Yano anticipates claim 11 of the '353 Patent. (RIB at 43.) Staff agrees. (SIB at 46-55.) Yano, entitled "Method for Writing Data to Memory," was filed by Sharp K.K. Company in Japan on March 26, 1990, and lists Eijiro Yano as the sole inventor. (RX-4261 at 1.) Yano discloses a system by which a processor can write data to memory through the use of a write command, a delay period, and a data strobe. (*Id.*) It was published on December 6, 1991 and, therefore, qualifies as prior art to the Barth Patents under 35 U.S.C. § 102(b). (*Id.*) Figure 1 of Yano illustrates the major pieces of the system disclosed in the application (with annotations):

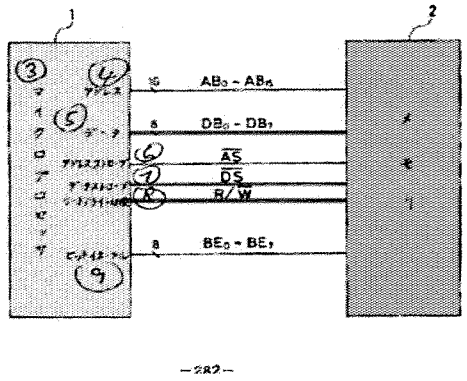


Figure 1

(Simplified Construction Diagram of One Embodiment of This Invention)

(3) microprocessor
(4) address
(5) data
(6) address strobe
(7) data strobe
(8) read/write switching
(9) bit enable
2 ~ memory

As shown, Yano discloses a microprocessor (yellow), that controls a memory device (blue). "As shown in the figure, 1 is an 8 bit microprocessor, 2 is a memory, $AB_0 \sim AB_{15}$ is an address bus

[11] Respondents have chosen not to discuss the following prior art references in detail even though they argue that they also anticipate the Barth Patents: Japanese patent Publication No. 7-262769 ("Seki"); U.S. Patent No. 5,343,503 ("Goodrich"); RamLink High-Bandwith Memroy Interface Based on SCI Signaling Technology ("Ramlink"); and Motorola 6800 Art ("MMI").

with 16 lines, $D_{B0} \sim D_{B7}$ is a databus with 8 lines, AS is a control bus for address strobe signal, DS is a control bus for data strobe signal, and R/W is a control bus for the read/write switching signal." (RX-4261 at 3:30-33.)

Figure 2, annotated below, is a timing diagram for a write operation disclosed in Yano.

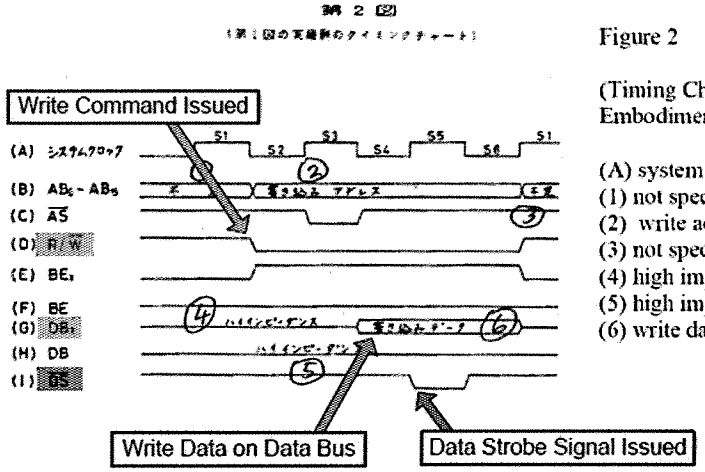


Figure 2

(Timing Chart of the Embodiment of Figure 1)

(A) system clock
(1) not specified
(2) write address
(3) not specified
(4) high impedance
(5) high impedance
(6) write data

The memory controller sends command, address, and data information to the memory device timed in accordance with the system clock (A). Specifically:

> Figure 2 is a timing chart of the embodiment shown in Figure 1. As shown in the figure, (A) indicates the system clock, (B) indicates address buses ($A_{B0} \sim AB_{15}$), (C) is the address strobe signal (AS), (D) is the read/write changeover signal (R/W), (E) is a bit enable signal (BEx) corresponding to a bit that is to be overwritten, (F) is a bit enable signal (BE) corresponding to other bits, (G) is a databus corresponding to a bit in which writing is to be conducted, (H) is a databus (DB) corresponding to other bits and (I) is the data strobe signal (DS).

(*See id.* at 3:40-46) As shown, each transition of the command, address, and data information is aligned with either a rising or falling edge of the system clock. (RX-5429C at Q232; RDX-3441; Tr. at 2608:23-2613:3.)

Rambus' argues that Yano is an asynchronous memory interface that fails to disclose the strobe signal that "initiate[s] sampling of a first portion of the data" and write command of claim 11 that is "one or more bits which specify that the memory device receive and store data." (CIB

at 59-60; 65-66; CRB at 27-34.) Rather, the data strobe in Yano creates an "active state," which is an indeterminate amount of time during which data flows into the memory. (CIB at 65.) The asynchronous memory does not receive a clock signal or any other signal used to capture data at a discrete point in time and, as such, does not issue the claimed strobe signal. (CIB at 65-66.) Yano discloses a R/W signal that must be held through the execution of the operation and fails to convey information indicative of a write operation. (CIB at 65-66.)

For the reasons set forth below, the ALJ finds that Respondents and Staff have shown by clear and convincing evidence that Yano discloses each and every element of claim 11 of the '353 Patent.

(1) *A Method of Controlling a Memory Device That Includes a Plurality of Memory Cells, the Method Comprising:*

The evidence shows that Yano discloses the preamble of claim 11. (RX-5429C, Jacobs Direct Q&A 241.) Figure 1 of Yano depicts a memory 2 that is controlled by a microprocessor 3:

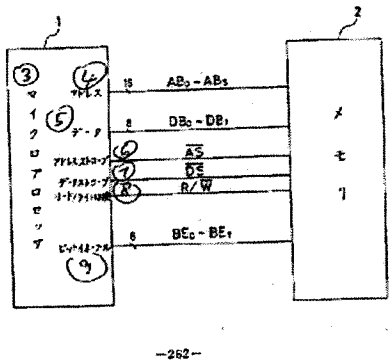


Figure 1

(Simplified Construction Diagram of One Embodiment of This Invention)

(3) microprocessor
(4) address
(5) data
(6) address strobe
(7) data strobe
(8) read/write switching
(9) bit enable
2 ~ memory

(RX-4261 at Figure 1; Jacobs, Tr. 1137:12-18; Przybylski, Tr. 2599:04-2600:25, 2605:07-12.) As Yano explains, the microprocessor 3 and memory 2 depicted in Figure 1 can be used to perform a method for writing data to memory 2:

> Specifically, according to a method for writing data to microprocessor memory, at the same time when said microprocessor outputs an address signal, a control signal is output specifying any bit within multiple bits creating the structure of 1 word. In addition, data corresponding to said any bit is transmitted through a databus so that this transmitted data is written to the memory corresponding to any of said bits specified by the address signal and by the control signal.

(RX-4261.0003; Przybylski, Tr. 2597:14-2598:17 (testifying as to same).) Rambus does not dispute that Yano discloses this element. (CIB at 27-34.) Therefore, the evidence shows that Yano discloses the preamble of claim 11.

(2) *Issuing a First Write Command to the Memory Device*

The evidence also shows that Yano discloses the first portion of the first step of claim 11. (Jacobs, Tr. 1142:14-21, 1144:09-1145:01; RX-5429C, Jacobs Direct Q&A 233, 234, 241, 247.) The R/W signal disclosed in Yano corresponds to the write command called for in claim 11. Figure 1 of Yano depicts a "R/W switching" line 8 running between the microprocessor 3 and memory 2. A timing diagram in Yano (reproduced below) depicts the R/W signal (as propagated on the R/W switching line of Figure 1) asserted low from clock phase S2 through clock phase S6 during which a write operation takes place:

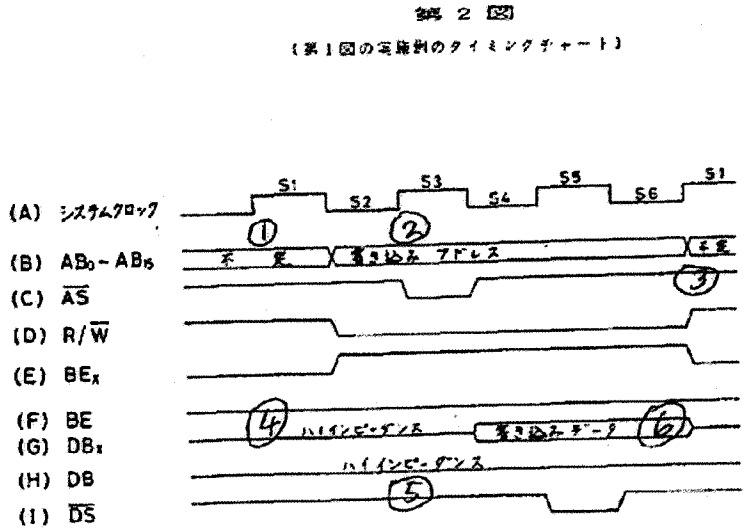


Figure 2

(Timing Chart of the Embodiment of Figure 1)

(A) system clock
(1) not specified
(2) write address
(3) not specified
(4) high impedance
(5) high impedance
(6) write data

(RX-4261 at Figure 2; *see also* Jacobs, Tr. 1144:09-1145:01; Przybylski, Tr. 2603:09-2604:02, 2632:24-2633:12, 2636:22-2637:01.)

As set forth *supra*, Rambus disputes whether the "write command" limitation of claim 11 is broad enough to encompass a signal or combination of signals asserted through the entire write operation, as was common in asynchronous memory systems available at that time. The ALJ finds that the claimed "write command" is broad enough to encompass a combination of signals asserted through the entire write operation. (RX-5429C, Jacobs Direct Q&A 247.) Various electronics dictionaries from the relevant timeframe define "write command" as simply an instruction to store data:

> **write** store data in a MEMORY.

(SX-6, Harper Collins Electronics Dictionary (1991) at 360 (emphasis in original).)

> **write** In computer practice, to transfer data from one form of storage to another form.

(SX-5, Illustrated Dictionary of Electronics (5th Ed. 1991) at 655 (emphasis in original).)

> **command** . . . **1.** In computer practice, the group of selected pulses or other signals which cause the computer to execute a step in its program. **2.** Instruction.

Id. at 113 (emphasis in original). Respondents' expert Dr. Jacobs testified that the dictionary definitions set forth above are consistent with how a person of ordinary skill in the relevant art would have interpreted the "write command" of the Barth I patents in light of the intrinsic record. (RX-5429C, Jacobs Direct Q&A 234; Jacobs, Tr. 1142:22-1144:08.) Indeed, nothing in the intrinsic record supports limiting the claimed "write command" to a particular form (*e.g.*, represented by one or more bits) or to a particular duration as Rambus contends. This is confirmed by the testimony of one of the inventors of the Barth Patents.[12] (JX-47C.0043 at

[12] In fact, the Examiner in charge of reexamining the '353 Patent recently explained:

166:21-167:8.) Thus, the plain and ordinary meaning of "write command," as supported by the weight of the intrinsic and extrinsic evidence of record, is simply an instruction to store data (*i.e.*, irrespective of form and duration), such as the R/W signal of Yano.

Rambus argues that the write command must take the form of "one or more bits" because the specification of the Barth I patents supposedly use the terms command control information, operation code, command, and bits interchangeably. (CIB at 66; CX-10765C, Przybylski Rebuttal Q&A 163.) The evidence shows, however, that one of ordinary skill in the art would understand the specification at most confirms that different techniques *can* be used instruct the memory device to store data associated with a write operation. In other words, the use of an operation code consisting of one or more bits is merely one preferred technique falling within the broader scope of write commands in general. (RX-5429C, Jacobs Direct Q&A 234.) One of ordinary of skill in the art would view the R/W signal of Yano as satisfying this element of claim 11 of the '353 Patent.

Thus, the ALJ finds that Respondents and Staff have shown by clear and convincing evidence shows that Yano discloses a R/W signal that satisfies the "write command" of claim 11 of the ''353 Patent.

(3) *The Memory Device Being Configured to Defer Sampling Data that Corresponds to the First Write Command Until a Strobe Signal is Detected*

The evidence shows that Yano discloses the second portion of the first step of claim 11. (Jacobs, Tr. 1147:07-12; 1148:13-1150:20; RX-5429C, Jacobs Q&A 235, 236, 241, 248.)

> [T]he claims do not make any requirement that a command be "complete". The claims only require the receipt of a command. Thus, there is no requirement that a command be received and then "completed" with a de[as]sertion.

(SX-0009, 11/14/2009 Office Action at pp. 22-23; RX-4245.0024-25.)

Specifically, Yano discloses "data strobe (DS)" signal that is issued from microprocessor 3 to memory 2:

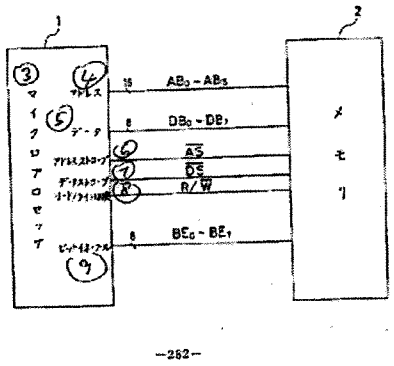


Figure 1

(Simplified Construction Diagram of One Embodiment of This Invention)

(3) microprocessor
(4) address
(5) data
(6) address strobe
(7) data strobe
(8) read/write switching
(9) bit enable
2 ~ memory

(RX-4261, Yano at Figure 1; 4:18-21; Przybylski, Tr. 2601:01-2602:07, 2604:03-12.) Yano further discloses a delay after issuing the write command (at time S2 on the system clock) until S5 on the system clock before issuing the "data strobe (DS)" signal from microprocessor 3 to memory 2. (RX-4261.0004 at 4:18-21; *see also* Figure 2.) Yano describes the use of its data strobe (DS) in the context of a write operation as follows:

> [T]he memory cell corresponding to the bit in which writing is performed is discriminated with address signals (AB_0 ~ AB_{15}) and with the bit enable signal (BEx) on the side of memory 2, the data strobe signal (DS) creates the active state, the write data is transmitted by the databus (DBx) corresponding to this bit and the data is written to this bit.

(RX-4261.0004 at 4:18-21.) The evidence shows that one of ordinary skill in the art would understand that this disclosure in Yano, *i.e.*, the creation of an "active state" by the data strobe during which the data is written to the bit, corresponds to the sampling disclosed in the Barth specification. (RX-5429C at Q&A 236.)

Rambus argues that data strobe (DS) disclosed in Yano is distinguishable from the claimed strobe signal because the data in Yano "is simply passed into memory" rather than

"sampled" at a discrete point in time. (CIB at 65-66.) However, the weight of the evidence does not support this purported distinction. (RX-5429C, Jacobs Direct Q&A 248.) Figure 2 shows that the data strobe signal (DS) is asserted low contemporaneous with the high phase of the system clock at S5 which causes data to be written to memory 2 at that point in time:

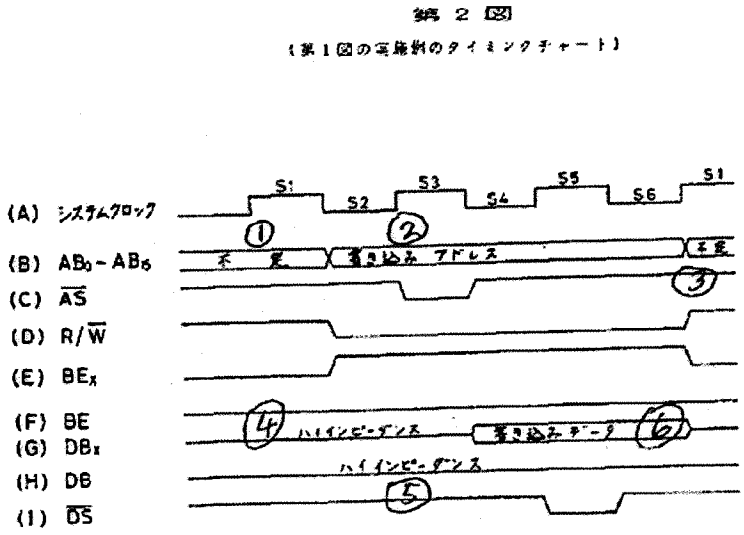


Figure 2

(Timing Chart of the Embodiment of Figure 1)

(A) system clock
(1) not specified
(2) write address
(3) not specified
(4) high impedance
(5) high impedance
(6) write data

(RX-4261, Yano at Figure 2; *see also* RX-5429C, Jacobs Direct Q&A 232, 235-236, 241, 248; Jacobs, Tr. 1139:23-1140:16; Przybylski, Tr. 2629:18-2631:21.) Therefore, the ALJ finds that Respondents and Staff have shown by clear and convincing evidence shows that Yano's memory devices defer sampling data that corresponds to the write command until the data strobe (DS) is detected as claimed.[13]

(4) *Delaying for a First Time Period after Issuing the Write Command*

[13] Moreover, even assuming that Rambus is correct that Yano's data strobe (DS) does not initiate sampling as claimed, the evidence shows that it would at least have been obvious to modify Yano so as to achieve the functionality of the claimed strobe signal. Namely, Yano's data strobe (DS) is asserted contemporaneous with valid data on the data bus. A person of ordinary skill in the relevant art would have looked to utilize such a technique as an alternative, improved approach to initiate sampling by a memory device, particularly as synchronous systems started overtaking asynchronous systems and the speeds of memory systems increased in the critical time frame (*i.e.*, as of the October 1995 priority date of the Barth I patents). (RX-5429C, Jacobs Direct Q/A 463-501, 532-542.)

The evidence shows that the microprocessor 3 in Yano delays for a first time period after first asserting low the R/W signal and before asserting low the data strobe (DS). (RX-5429C, Jacobs Direct Q&A 237, 241.) Indeed, as depicted in the timing diagram of Figure 2, one and a half clock cycles (corresponding to S2 to S4) lapse between the assertion of the R/W signal at the transition from S1 to S2 and the assertion of the data strobe (DS) at the transition from S4 to S5:

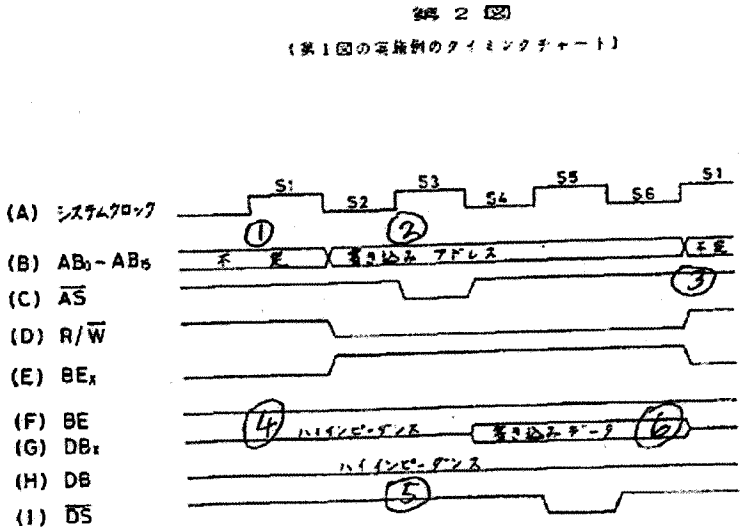


Figure 2

(Timing Chart of the Embodiment of Figure 1)

(A) system clock
(1) not specified
(2) write address
(3) not specified
(4) high impedance
(5) high impedance
(6) write data

(RX-4261, Yano at Figure 2, 4:8-21; *see also* RX-5429C, Jacobs Direct Q&A 237, 241.) Rambus does not dispute that Yano disclosed this limitation. (CRB at 27-34.) Indeed, Dr. Przybilski stated :

> Q. Do you see there is a delay between the R/W bar being asserted and the DS bar being asserted from here to here (indicating [in RDX-3293])?
>
> A. Yes. There is a temporal difference between the -- between the transition on the read/write line and the transition on the DS signal.
>
> Q. There is a delay, right?
>
> A. There is -- there is a delay. There is a temporal difference, right.

(Przybylski, Tr. 2604:22-2605:04.) Thus, the ALJ finds that Respondents and Staff have shown by clear and convincing evidence that Yano delays for a first period of time as claimed.

(5) After Delaying for the First Time Period, Issuing the "Strobe Signal" to the Memory Device to Initiate Sampling of a First Portion of the Data by the Memory Device

The final disputed limitation in claim 11 as to Yano involves the "strobe signal" recited in the last clause of the last step, and is closely related to the "strobe signal" limitation recited in the first step of this same claim. As set forth *supra* in Section Vi.B.1.a.3, the evidence shows that the data strobe (DS) in Yano is issued by microprocessor 3 to *initiate* sampling of data by memory 2 as claimed by the Barth Patents.

b) Dan

Respondents argue that Dan anticipates claim 11 of the '353 Patent. (RIB at 50.) Staff agrees. (SIB at 55-60.) Dan was filed by Tandem Computers, Inc. in the European Union on June 27, 1994, and lists Yei-Fong Dan as the sole inventor. (RX-4262 at cover page.) It was published on January 4, 1995 and, therefore, qualifies as prior art to the Barth Patents under 35 U.S.C. § 102(b). (*Id.*)

Rambus argues that Dan is an asynchronous memory interface that fails to disclose the strobe signal that "initiate[s] sampling of a first portion of the data" and write command of claim 11 that is "one or more bits which specify that the memory device receive and store data." (CIB at 59-60; 63-65; CRB at 27-34.) Rather, the data strobe in Dan does not initiate sampling of the data by the memory 110, but, rather, data flows into the memory over a period of time. (CIB at 63.) The clocking in the Dan reference refers to the system clock of the memory controller and does not disclose a signal that initiates the capture of data at a discrete point in time. (CIB at 63.) Dan discloses an external write strobe signal that initiates the write operation and not the sampling of data. (CIB at 63-64.)

For the reasons set forth below, the ALJ finds that Respondents and Staff have shown by clear and convincing evidence that Dan discloses each and every element of claim 11 of the '353 Patent.

.

(1) ***A Method of Controlling a Memory Device That Includes a Plurality of Memory Cells, the Method Comprising:***

The evidence shows that Dan discloses the preamble of claim 1. (RX-5429C, Jacobs Direct Q&A 262.) Figure 1 of Dan includes a memory interface unit 120 and a memory 110:

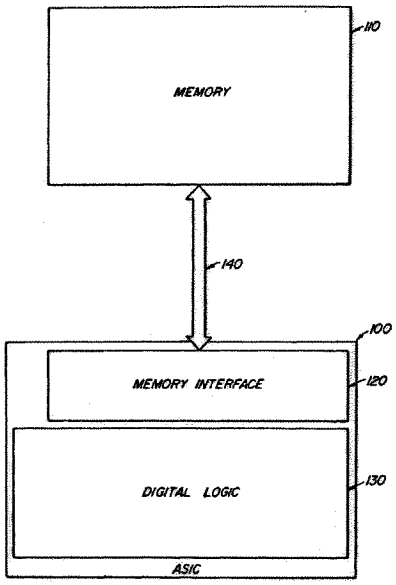


FIG. 1.

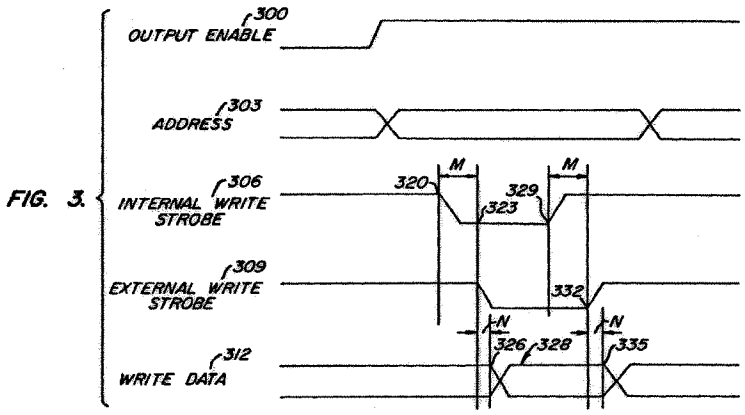
(RX-4262, Dan at Figure 1; RX-5429C, Jacobs Direct Q/A 255 (describing same).) As Dan explains, the memory interface unit 120 shown in Figure 1 can be used to perform a method for writing data to memory 110:

> The present invention relates generally to *an interface on a semiconductor integrated circuit (IC) to write and read data to an external memory.* More specifically, the present invention relates to a memory interface on a semiconductor IC that transfers data to a data bus and writes the data to an external memory upon the clocking of a write strobe signal. The memory interface enables and disables the semiconductor IC from transferring data to the data bus upon the assertion and deassertion of the write strobe signal.

(*Id.* at 1:01-10 (emphasis added).) Rambus does not dispute that Dan discloses this limitation. (CRB at 27-34.) Thus, the ALJ finds that Respondents and Staff have shown by clear and convincing evidence shows that Dan discloses the preamble of claim 11.

(2) *Issuing a First Write Command to the Memory Device*

The evidence also shows that Dan discloses this limitation of claim 11. (RX-5429C, Jacobs Direct Q&A 256-257, 262.) Specifically, Dan discloses a write command in the form of an "output enable signal 300" that is similar to the R/W signal of Yano. (RX-4262, Dan at 6:44-7:41 ("To begin the write cycle, memory interface unit 120 deasserts output enable signal 300, which is normally asserted low…to indicate external memory 110 that a write operation will take place."), *see also* Figure 3 (timing diagram for a write operation); RX-5429C, Jacobs Direct Q&A 256-257, 262.) This output enable signal 300 of Dan is depicted in the context of a write operation in the timing diagram of Figure 3:



(RX-4262, Dan at Figure 3; RX-5429C, Jacobs Direct Q&A 256 (describing same).)

Rambus's arguments that Dan fails to disclose this limitation are similar to those set forth *supra* for Yano, namely arguing for a narrow construction of the "write command." As set forth *supra* in Section VI.B.1.a.2, Rambus's arguments fails for the same reason as they failed for Yano. (RX-5429C, Jacobs Direct Q&A 257, 262, 266.) Therefore, the ALJ finds that

Respondents and Staff have shown by clear and convincing evidence that Dan discloses the "write command" limitation of the Barth Patents.

(3) *The Memory Device Being Configured to Defer Sampling Data that Corresponds to the First Write Command Until a Strobe Signal is Detected*

The evidence also shows that Dan discloses this limitation of claim 11. (RX-5429C, Jacobs Direct Q&A 258-260, 262.) Specifically, Dan discloses a "write strobe signal 309" that initiates the sampling of data by a memory device:

> The present invention relates generally to an interface on a semiconductor integrated circuit (IC) to write and read data to an external memory. More specifically, the present invention relates to a memory interface on a semiconductor IC that transfers data to a data bus and *writes the data to an external memory upon the clocking of a write strobe signal.* The memory interface enables and disables the semiconductor IC from transferring data to the data bus upon the assertion and deassertion of the write strobe signal.

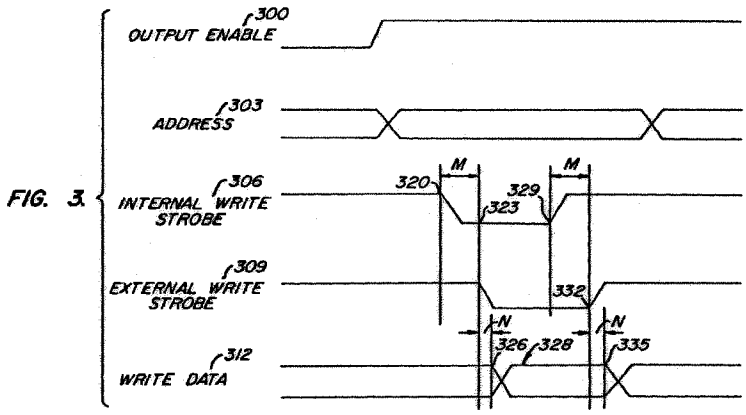
(*Id.* at 1:01-10 (emphasis added).) As Dr. Jacobs testified at trial, this strobe signal 309 in Dan causes data to be sampled by the memory device in essentially the same manner as the claimed strobe signal of the Barth I patents. (RX-5429C, Jacobs Direct Q&A 258-260, 262.)

Rambus's arguments that Dan fails to disclose this limitation are similar to those set forth *supra* for Yano, namely arguing for a narrow construction of the "sampling." As set forth *supra* in Section VI.B.1.a.3, Rambus's arguments fails for the same reason as they failed for Yano. (RX-5429C, Jacobs Direct Q&A 258-259, 262, 267.) Therefore, the ALJ finds that Respondents and Staff have shown by clear and convincing evidence that Dan discloses this limitation of the Barth Patents.

(4) *Delaying for a First Time Period after Issuing the Write Command*

The evidence shows that the memory interface unit 120 delays for a first time period after first asserting the output enable signal 300 and before asserting write strobe signal 309. (RX-

5429C, Jacobs Direct Q&A 260, 262.) Indeed, as depicted in the timing diagram of Figure 3, some period of time lapses between the assertion (low-to-high) of the output enable signal 300 and the assertion (high-to-low) of the external write strobe 309 as part of a write operation:



(RX-4262 at 6:44-7:2, Figure 3; RX-5429C, Jacobs Direct Q&A 256 (describing same).) Therefore, the ALJ finds that Respondents and Staff have shown by clear and convincing evidence shows that Dan delays for a first period of time as claimed.

(5) *After Delaying for the First Time Period, Issuing the "Strobe Signal" to the Memory Device to Initiate Sampling of a First Portion of the Data by the Memory Device*

The final disputed limitation in claim 11 as to Dan involves the "strobe signal" recited in the last clause of the last step, and is closely related to the "strobe signal" limitation recited in the first step of this same claim. The evidence shows that the memory interface unit 120 issues the write strobe signal 309 to *initiate* sampling of data by memory 110 as claimed. (RX-4262 at 1:3-7 ("the present invention relates to a memory interface on a semiconductor IC that transfers data to a data bus and writes the data to an external memory upon the clocking of a write strobe signal.") For reasons discussed above with respect to the first step of claim 11, clear and convincing evidence shows that the write strobe signal 309 in Dan is issued by memory interface

unit 120 to *initiate* sampling of data by memory 110. (RX-4262, Dan at Figure 3; RX-5429C, Jacobs Direct Q&A 256 (describing same).)

c) NextBus/Harriman

Respondents argue that NextBus anticipates claims 11-13 of the '353 Patent and claims 1, 20, and 14 of the '109 Patent. (RIB at 53-62.) Staff agrees. (SIB at 62-72.)

U.S. Patent No. 5,313,624 ("Harriman") incorporates by reference the NextBus specification. Respondents argue that to the extent that NextBus fails to disclose each and every element, Harriman also anticipates claims 11-13 of the '353 Patent and claims 1,20 and 24 of the '109 Patent. Staff agrees. (SIB at 62-72.) While Respondents performed an element by element analysis of Harriman in their initial post-hearing brief, that analysis is similar to the NextBus analysis set forth below. Indeed, many of Rambus's arguments against Harriman parallel those to NextBus, *e.g.*, Harriman does not disclose the claimed "memory device." (CRB at 37-40.) To the extent that the anticipation analysis for Harriman is strikingly similar to the analysis for NextBus, the ALJ incorporates by reference his analysis below for the Harriman reference. The ALJ finds that setting forth the analysis for Harriman would be a duplicative effort, especially in light of the fact that Harriman specifically incorporates by reference the entire NextBus specification.

Rambus argues that NextBus is not prior art and, further, that it fails to anticipate because the claimed memory device does not include a memory board containing a memory controller as disclosed by NextBus. (CRB at 37-40.) Rambus further argues that NextBus fails to anticipate claims 12 and 13 of the '353 Patent and claims 1, 20 and 24 of the '109 Patent because it fails to disclose sampling during the odd and even phases. (CRB at 40.)

(1) *NextBus is prior art*

The NextBus Specification is a document by NeXT Inc. bearing a 1990 copyright date, and generally describes a synchronous bus architecture that could be used, for example, in a NeXT computer system. (RX-4265.0002.) If the NextBus Specification was indeed made publicly available sometime in 1990 as its copyright date suggests, it would constitute prior art under 35 U.S.C. § 102(b) based on the Barth I Patent's October 1995 priority date. However, Rambus disputes whether the the NextBus Specification was publicly available any time prior to October 1995. (CRB at 34-37.)

The Federal Circuit has articulated the standard for determining the public availability of a reference as follows:

> In order to qualify as a printed publication within the meaning of § 102, a reference "must have been sufficiently accessible to the public interested in the art." "Because there are many ways in which a reference may be disseminated to the interested public, 'public accessibility' has been called the touchstone in determining whether a reference constitutes a 'printed publication' bar under 35 U.S.C. § 102(b)." Whether a reference is publicly accessible is determined on a case-by-case basis based on the "facts and circumstances surrounding the reference's disclosure to members of the public." A reference is considered publicly accessible if it was "disseminated or otherwise made available to the extent that persons interested and ordinarily skilled in the subject matter or art exercising reasonable diligence, can locate it."

In re Lister, 583 F.3d 1307, 1311 (Fed. Cir. 2009) (internal citations omitted).

The ALJ finds that the NextBus Specification is prior art under 35 U.S.C. § 102(b). The evidence shows that the NextBus Specification was publicly available sometime prior to the October 1995 priority date of the Barth I patents. In particular, the 1990 copyright date, a specified reorder number N6010 (that allowed customers to order the NextBus Specification), and technical support telephone number within the NextBus Specification collectively suggest that the document was indeed publicly available. (RX-4265.0002, RX-4265.0017; Jacobs, Tr. 1152:24-1154:07; Przybylski, Tr. 2647:14-22.) In addition, other publicly available documents

in the 1991 timeframe, such as Harriman, specifically incorporate by reference a NextBus Specification, further suggesting that persons of ordinary skill in the relevant art exercising reasonable diligence could locate a copy of that reference. (RX-4277.0019 at 15:43-46; Jacobs, Tr. 1154:08-1155:07, 1165:10-1167:17.) *See Orion IP, LLC v. Hyundai Motor Am.*, 605 F.3d 967, 974-75 (Fed. Cir. 2010) (finding an Electronics Parts Catalogue with a 1987 copyright date to qualify as prior art *before* the 1988 critical date of the asserted patent "because it was accessible to those interested in the business of auto parts prior to November 10, 1988"). For at least these reasons, the ALJ finds that the evidence shows the NextBus specification is prior art at least under 35 U.S.C. § 102(b).

Rambus argues that the NextBus Specification is not prior art because there is no publication date or a retrieval date and that the reorder number and warranty information are insufficient to show public availability. (CRB at 34-35.) Rambus further argues that the cases relied upon by Staff and Respondents fail to support their arguments. (CRB at 34-37.) The ALJ finds Rambus' arguments unpersuasive in light of the evidence. Specifically, the facts and circumstances surrounding the public availability of the NextBus Specification, as set forth *supra*, support a finding that it was publicly available. Rambus's arguments simply state that such evidence is insufficient without providing a reason as to why they are insufficient.

(2) *"A method of controlling a memory device that includes a plurality of memory cells" ('353 Patent claim 11)/ "A method of controlling a memory device having a memory core" ('109 Patent claims 1, 20, 24)*

The NextBus Spec discloses a system that connects a processor, such as a CPU, to other devices, including memory devices with a plurality of cells. Figure 1-1 of the NextBus Spec illustrates the component parts of the NextBus system:

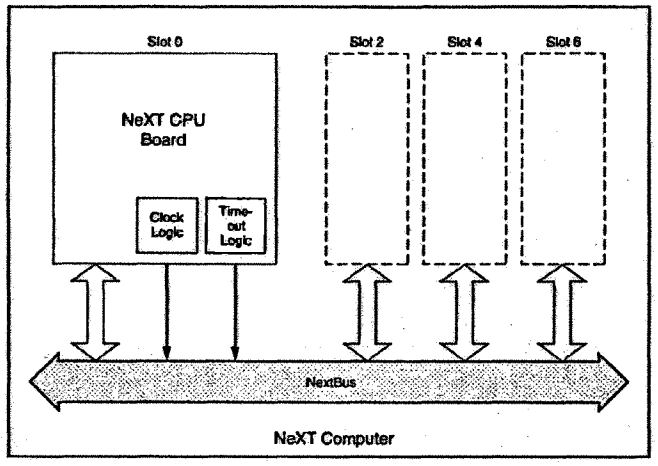


Figure 1-1. NextBus in the NeXT Computer

(RX-4265.00014.) The NextBus connects the "master" (CPU) with the "slave" devices located in Slots 2, 4, and 6 that the CPU controls, including "memories." (*See* RX-4265.0040.) The evidence shows that "a person of ordinary skill in the art would know that one type of board you could put into [slot 2] is a memory board." (Przybylski, Tr. at 2655:15-18.) The memory board may be used to perform burst write transactions wherein the data is written from a memory controller to a DRAM on the memory board:

> Figure 4-11 shows timing for a NextBus burst write transaction in which the slave board uses the TMO* signal to indicate that it will not accept more than one four-word data burst.

RX-4265.0048.

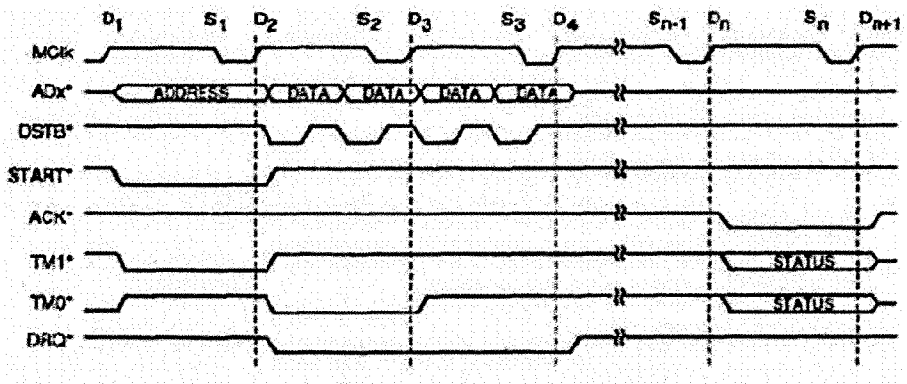


Figure 4-11. NextBus Burst Write Transaction

(RX-4265.0049.)

Rambus argues, however, that the memory boards disclosed in the NextBus Spec are not "memory devices" as required in the asserted Barth claims. (CX-10765C at Q247; CRB at 37-38.) Rambus argues that the "memory device" in the Barth Patents is an "integrated circuit device—meaning a circuit constructed on a single monolithic substrate, commonly called a chip-in which information can be stored and retrieved electronically" and that the NextBus Spec only applies to "memory boards," which Rambus claims are not "memory devices." (CX-10765C at Q244, 246; CRB at 37-38.)

The ALJ finds Rambus's arguments unpersuasive. First, Rambus fails to point to anything in the Barth Patents that supports their construction of "memory device." Rather, the evidence shows that a memory device is simply "a device in which information can be stored and retrieved electronically." (RX-5429C at Q310.) The IEEE dictionary, which defines the term "***device***" as a "circuit or logical group of circuits resident to ***one or more boards*** capable of interacting with other such devices through a bus." (*Id.* (emphasis added).) Indeed, Rambus fails to offer any extrinsic evidence (not a single dictionary definition) to support their proposed construction that the term "memory device" has to be limited to a single monolithic substrate. (Tr. at 2657:19-2658:25.)

Second, Rambus's proposed construction of the "memory device" term was recently rejected by the Examiner during reexamination of the Barth Patents:

> The Examiner agrees that a memory device can be considered a single chip, however, the Examiner notes that a memory device is not always limited to a single chip and that the patent specification also does not support that the broad term 'memory device' is a signal chip.

(SX-0008, February 26, 2010 Office Action at 2; RX-4246.0005; *see also* Przybylski, Tr. 2660:08-20 (disputing the construction adopted by the Examiner during reexamination of the

'353 patent).) This is further supported by the evidence in this investigation. (RX-5429C, Jacobs Direct Q/A 306, 310; Jacobs, Tr. 1157:08-1158:06, 1158:25-1161:13.) For example, Dr. Jacobs testified:

> First, the Barth patents do not provide any special meaning to the term memory device. In fact, nothing in the Barth patents gives any indication that a memory device can only be a single monolithic chip. While I agree that a memory device can be a single monolithic chip, I do not believe a general term like memory device is that limited in scope.
>
> Second, in the reexamination of the '353 patent, the Examiner considered this issue and agreed with my opinion. Specifically, the Examiner found in the Right of Appeal Notice on page 7, which is found in R.X-4246, that a term memory device is not limited to only a single monolithic chip, but rather "a device in which information can be stored and retrieved electronically." The Examiner then cited to the IEEE dictionary definition to provide the plain and ordinary meaning of "device" as a "circuit or logical group of circuits resident to one or more boards capable of interacting with other such devices through a bus." With respect to the plain meaning of the term memory device, I agree with the Examiner. It is my opinion that one of ordinary skill considering the term "memory device" as used in the asserted drums of the Barth patent would understand that a memory device can be more than simply a monolithic chip.
>
> The NextBus Specification (RX-4265) discloses "memories" that can be connected to the NextBus in Slots 2, 4 and/or 6 as shown in Figure 1.1. A person of ordinary skill would certainly consider such "memories" as memory devices. Dr. Przybylski argues that NextBus Specification only discloses memory boards. Even [if] this is true, a person of ordinary skill would consider a memory board to be a memory device.

(RX-5429C, Jacobs Direct Q&A 310; *see also* Jacobs, Tr. 1119:15-1121:07, 1122:21-1123:17, 1156:02-1161:20.) The evidence shows that one of ordinary skill in the art would conclude that the "memories" of the NextBus Spec are "memory devices" within the meaning of the asserted claims.

Therefore, the ALJ finds that Respondents and Staff have shown by clear and convincing evidence that the NextBus Specification anticipates (or renders obvious) the "memory device" limitations and the preamble of the asserted Barth I patent claims.

(3) ***"issuing a first write command to the memory device" ('353 Patent, claim 11)/ "providing control information to the memory device, wherein the control information includes a first code which specifies that a write/transfer operation be initiated in the memory device" ('109 Patent claims 1, 20, 24)***

The NextBus Spec discloses sending a write command to the memory device using a combination of signals. Specifically, as shown in Table 4-1 below, a write command for a burst write transaction is TM1* (L), TM0*(H), AD1*(L), and AD0*(H). (*See* RX-4265.0035; RX-5429C at Q295; CX-10765C at Q244-246.)

The evidence shows that NextBus discloses the first portion of the first step of claim 11 by sending a write command to the memory device using a combination of signals. (RX-4265.0035; RX-5429C at Q295, 306; CX-10765C at Q244-246.) More specifically, NextBus discloses a combination of signals TM1* (L), TMO*(H), ADl *(L), and AD0*(H) that collectively represent a write command as shown in Table 4-1 below:

Table 4-1. Encoding of Transaction Type and Size

TM1*	TM0*	AD1*	AD0*	Type of Cycle
L	L	L	L	Write byte 3
L	L	L	H	Write byte 2
L	L	H	L	Write byte 1
L	L	H	H	Write byte 0
L	H	L	L	Write halfword 1
L	H	L	H	Write burst
L	H	H	L	Write halfword 0
L	H	H	H	Write word
H	L	L	L	Read byte 3
H	L	L	H	Read byte 2
H	L	H	L	Read byte 1
H	L	H	H	Read byte 0
H	H	L	L	Read halfword 1
H	H	L	H	Read burst
H	H	H	L	Read halfword 0
H	H	H	H	Read word

(RX-4265.0035; RX-5429C, Jacobs Direct Q&A 295, 306.) Rambus does not dispute that NextBust discloses this limitation. (CRB at 37-38.) As set forth *supra*, the ALJ declines to adopt Rambus's proposed narrow construction for "memory device" and, as such, the ALJ finds that Respondents and Staff have shown by clear and convincing evidence that NextBus discloses this limitation.

(4) ***"the memory device being configured to defer sampling data that corresponds to the first write command until a strobe signal is detected, delaying for a first time period after issuing a write command" ('353, Cl. 11)***

The evidence further shows that NextBus discloses this limitation. Specifically, the NextBus Spec discloses a system whereby two different strobe signals–DRQ* and DSTB* (discussed *supra*)–are used to write data to memory. Both signals are depicted in Figure 4-11:

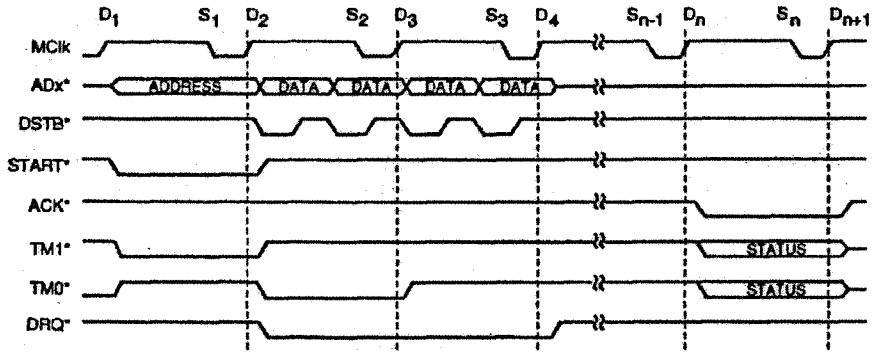


Figure 4-11. NextBus Burst Write Transaction

(RX-4265.0049; RX-5429C at Q&A 294, 297.) As shown above, after the combination of signals constituting the write command is issued at time D1, at time D2, the "master" sending data issues a "Data Request" strobe signal "DRQ*" "to indicate that it is supplying two words of data in the current major cycle." (*See* RX-4265.0026; *see also* RX-4265.0045 ("During a burst write operation, the master uses the DRQ* signal to indicate when the source is ready to transfer data.").) This corresponds to the "strobe signal" disclosed in the Barth Patents. (RX-4540 at 8:61.) Given that DRQ* is issued to indicate that it is supplying two words of data in the current major cycle, DRQ* is data transfer start information, just like the strobe signal of the Barth Patents. (RX-5429C at Q296.)

NextBus also discloses a data strobe (DSTB*) that initiates the sampling of data by a memory device:

> **Data Strobe (DSTB*)**
> During burst transfers, the board sending data (the master during writes, and the slave during reads) generates the DSTB* signal by gating BUSCLK. The data sender asserts DSTB* at the same time that it places data on the bus. The receiver then captures data at the rising edge of DSTB*.

(RX-4265.0025 (emphasis in original); RX-5429C, Jacobs Direct Q&A 296, 306; *see also* Przybylski, Tr. 2648:21-2649:24, 2652:17-2653:16.) As shown in Figure 4-11, the master asserts the write command at time D1, but delays until after time D2 to assert the strobe signals DRQ* and DSTB*.Thus, DSTB* is used to sample the data (rather than a clock signal) in order to "minimiz[e] skew between the data and its clock." (*See* RX-4256.0071.) Thus, as Jacob testified, DSTB* is the same type of signal and has the same purpose as DQS in the JEDEC DDR SDRAM specification Rambus alleges is covered by the asserted Barth claims. (RX-5429C at Q296.)

In addition, Rambus's own expert Dr. Przybylski admitted the relationship between the DSTB* signal and sampling in this regard:

> Q: Please tell His Honor yes or no, does this disclose using the strobe signal to sample data off the data bus? Yes or no, sir.
>
> A: The receiver captures the data on the rising edge of DSTB. That's what it says.
>
> Q: And that's sampling, isn't it?
>
> A: That's sampling . . .

(Przybylski, Tr. 2651:17-23; 2653:13-16 (similar testimony).) Rambus does dispute that the DSTB* signal represents a data strobe signal that initiates the sampling of data. (CRB at 37-40; Przybylski ,Tr. at 2651:17-21 (arguing that the DRQ* signal is not the claimed "strobe signal," but not disputing that DSTB* reads on the "strobe signal" from the asserted Barth claims). As set forth *supra*, the ALJ declines to adopt Rambus's proposed narrow construction for "memory

device" and, as such, the ALJ finds that Respondents and Staff have shown by clear and convincing evidence also shows that NextBus discloses this limitation.

> **(5)** ***"issuing a strobe signal to the memory device to initiate sampling of a first portion of the data by the memory device" ('353 Patent Claim 11)/"providing a signal to the memory device, wherein the signal indicates when the memory device is to begin sampling write data/the transfer operation/the write operation, wherein the write data is stored in the memory core during the write operation" ('109 Patent claims 1, 20, 24)***

The NextBus Spec discloses the use of two strobe signals that "initiate sampling of a first portion of the data by the memory device" and indicate "when the memory device is to begin sampling write data," that satisfies the "strobe signal"/"signal" elements of the '353 and '109 Patents, respectively. In the NextBus Spec, write operations take place between the CPU and the attached "slaves" (*e.g.*, "memories") controlled by the CPU. In the context of a burst write transaction (*i.e.*, a write transaction involving multiple pieces of data), the NextBus Spec discloses a system whereby two different strobe signals–DRQ* and DSTB* (discussed *supra*)–are used to write data to memory. Both signals are depicted in Figure 4-11:

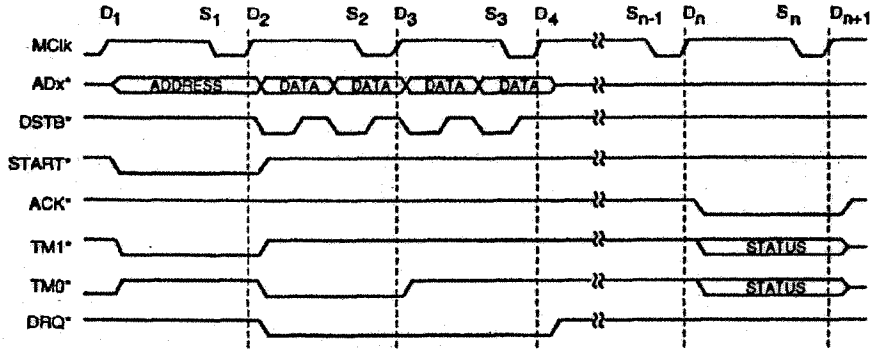


Figure 4-11. NextBus Burst Write Transaction

(RX-4265.0049.) First, as shown in Figure 4-11, after the combination of signals constituting the write command is issued at time D1, at time D2, the "master" sending data issues a "Data Request" strobe signal "DRQ*" "to indicate that it is supplying two words of data in the current

major cycle." (*See* RX-4265.0026; *see also* RX-4265.0045 ("During a burst write operation, the master uses the DRQ* signal to indicate when the source is ready to transfer data.").) This corresponds to the "strobe signal" disclosed in the Barth Patents. (RX-4540 at 8:61.) Given that DRQ* is issued to indicate that it is supplying two words of data in the current major cycle, DRQ* is data transfer start information, just like the strobe signal of the Barth Patents. (RX-5429C at Q296.)

The second separate "Data Strobe" signal "DSTB*" whereby the "data sender asserts DSTB* at the same time it places data on the bus" was already discussed *supra*. Therefore, the ALJ finds that Respondents and Staff have shown by clear and convincing evidence that the strobe signal DSTB* in NextBus is issued by a memory controller to a memory device to initiate sampling as claimed.

(6) *Providing / Transferring Two Portions of Data to the Memory Device and Sampling During Odd and Even Phases of a Common Clock Cycle ('353, Cl. 12-13; '109, Cl. 1, 20,24)*

The evidence shows that NextBus discloses providing two portions of data and sampling that data during an odd and even phase of an external clock signal. (RX-5429C at Q298.) Specifically, a "synchronous (12.5 MHz), multiplexed, multimaster bus" where "a basic cycle rate of 12.5 MHz, and a mechanism that allows data burst transfers to occur at a rate of 25 MHz." (*See* RX-4265.0013.) The NextBus Spec states that it "[t]ransfers two words per burst cycle." (*See* RX-4265.0014.) Moreover, Figure 4-11 shows that DSTB* is used to sample the first portion of data in an odd phase of a clock cycle of MCLK* and a second portion of data in an even phase of the same cycle of MCLK*:

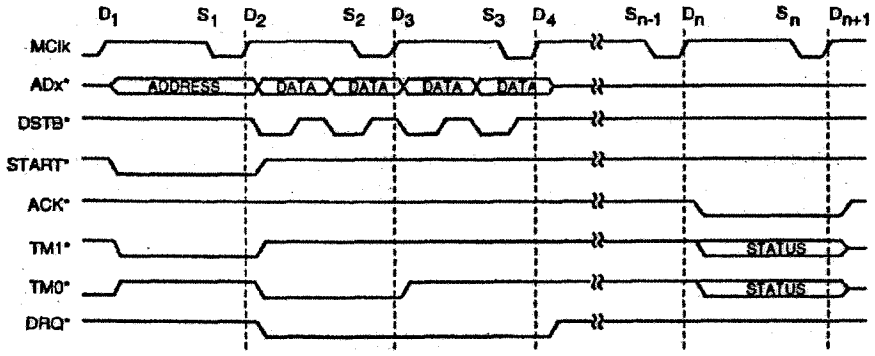


Figure 4-11. NextBus Burst Write Transaction

(*See* RX-4265.0049.)

MCLK* is one of one of three clock signals disclosed in the NextBus Spec (*i.e.*, BUSCLK, MCLKSEL*, and MCLK*), and is a 12.5 MHz internal clock with a 75% duty cycle. (RX-4265.0018-19.) MCLK* is generated from two external clocks–BUSCLK (Busclock) and MCLKSEL* (Major Clock Select). (*Id.*) The relationship between BUSCLK, MCLKSEL*, and MCLK* is shown in Figure 1-5 of the NextBus Spec. (RX-4265.0018.) As seen in Figure 1-5, BUSCLK and MCLKSEL* are used to create MCLK*. Specifically, MCLK* is the logical "OR" of BUSCLK and MCLKSEL* (*i.e.*, MCLK is in a high position when either BUSCLK or MCLKSEL* is high):

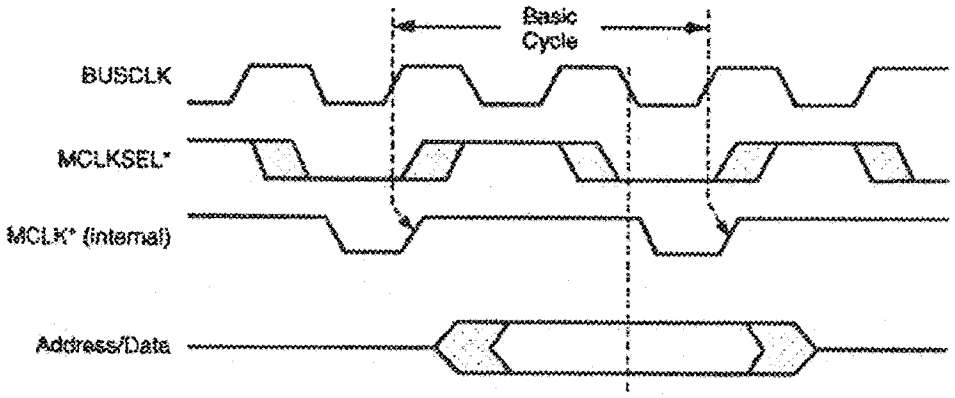
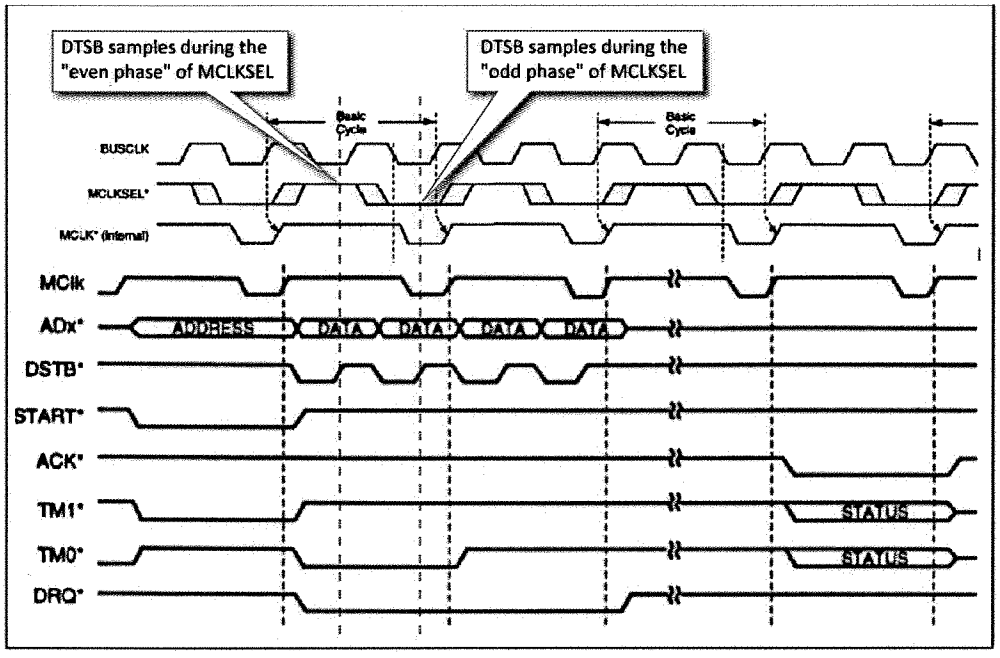


Figure 1-5. NextBus Basic Timing Signals

(RX-4265, Figure 1-5.) The reason why MCLK* has a long phase and a short phase is because it has a 75% duty cycle.

The evidence shows that a first portion of data is sampled during an even phase of the MCLKSEL* signal and a second portion of data is sampled during an odd phase of the MCLKSEL* signal, with the even and odd phases occurring during a common cycle of the MCLKSEL* signal:



(RDX-0419; (overlaying the timing diagram of the clock signals (Figure 1-5) on the timing diagram of the other signals (Figure 4-11)); RX-5429C at 303-304.) As shown, during burst write transactions, the first piece of data is sampled by the rising edge of DSTB* during the odd phase of the external clock MCLKSEL* and the second piece of data is sampled by the rising edge of DSTB* during the of even phase of external clock MCLKSEL*. (RX-5429C at 304.) As a result, both portions of data are issued during a common clock cycle of MCLKSEL*. (RX-5429C at Q298-304.) The evidence shows that one of ordinary skill in the relevant art would view this disclosure in NextBus as satisfying the double data rate limitations recited in the Barth Patent claims.

Rambus argues MCLKSEL* does not constitute a "clock signal" as required in the asserted claims. (CRB at 40; CX-10765C at Q255.) The evidence shows, however, that MCLKSEL* is described as a clock, even containing the abbreviation "CLK" in its label. Moreover, MCLKSEL* is a free-running, periodic signal–characteristics that are indicative of a clock. As described above, MCLKSEL* is "OR"ed with another clock, BUSCLK, to form a third clock, MCLK*. (RX-5429C at Q299-301, RDX-0418.) The evidence further shows that even if MCLKSEL* were not a clock, it would make no sense to think you could "OR" a clock like BUSCLK with a non-clock signal (MCLKSEL*) and have the result still be a clock (MCLK*). (RX-5429C at Q311.) Therefore, the ALJ finds that Respondents and Staff have shown by clear and convincing evidence that NextBus discloses these limitations.

d) Hayes

Respondents argue that Hayes anticipates claim 11 of the '353 Patent. (RIB at 67-70.) Hayes is assigned to Digital Equipment Corporation was filed September 4, 1987, 1991 and issued June 8, 1993. (*See* RX-4268.001.) Hayes is prior art under 35 U.S.C. §102(b). (*See id.*)

Staff agrees. (SIB at 62-72.)

Rambus argues that Hayes fails to disclose a "memory device" as claimed in the Barth Patents and fails to disclose a "strobe signal" that "initiates sampling" as required by the Barth Patents. (CRB at 42-43.)

(1) *"A method of controlling a memory device that includes a plurality of memory cells"*

The evidence shows that Hayes describes a "memory configuration system" wherein the "local bus 17 interfaces the processor chip 10 with local memory and on-board logic and supports direct memory access (DMA) transfers to and from local memory and the system bus." (*See* RX-4268.0013 at 6:4-8.) Hayes also discloses a "single board computer module 9" connected to a number of "memory array boards" via a "memory array bus" as depicted in the portion of Figure 1 of the Hayes patent. (*See* RX-4268 at 3:45-58; 5:4-8.) Each memory array board includes a RAM Control Logic and 256Kbit Dynamic Ram Chips (DRAM), which is a "memory device" as that term is used in the asserted claims of the Barth Patents. (RX-5429C.0123.) This Examiner in the '353 Reexamination reached the same conclusion finding claim 11 of the '353 Patent invalid as anticipated by Hayes. (*See* RX-4246 at 7-8.) Furthermore, the evidence shows that the DRAM chips each have a plurality of memory cells as required by the asserted claims. (RX-5429C.0123.)

Rambus argues that Hayes fails to disclose the claimed "memory device." Rambus again argues that a "memory device" cannot include memory boards that house multiple DRAM chips and an on-board controller. (CRB at 42; CX-10765C at Q358.) As the ALJ set forth *supra* in Section VI.B.1.c, the ALJ declined to adopt such a narrow reading of "memory device." In addition, the Examiner in the '353 Reexam found that the RAM Control Logic and 256Kbit Dynamic Ram Chips (DRAM) (as shown in Fig. 7 of Hayes) to be a "memory device," as was

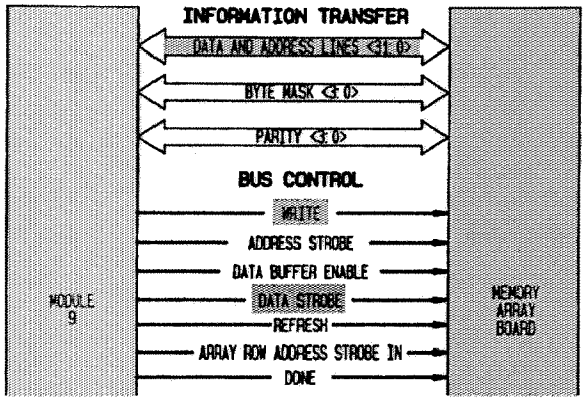
the entire memory array board. (*See* RX-4246 at 7-8.)

Therefore, the ALJ finds that Respondents have shown by clear and convincing evidence that Hayes discloses the preamble of claim 11.

(2) *"issuing a first write command to the memory device"*

The evidence shows that Hayes discloses sending the claimed write command to a memory device. (RX-5429C.0123-25.) Figure 5 depicts the various signals used to write data from "module 9" (shown in Figure 1) to the memory array boards containing the memory devices (annotated):

FIG. 5



Hayes states:

> Write line (WR) specifies the direction of a data transfer on DAL[31:0]. If the bus master asserts WR, then it will drive data onto DAL[31:0]. If the bus master does not assert WR, then the slave device will drive data onto DAL[31:0].

(RX-4268.0014 at 7:41-45; *see also* 19:57-59.) Rambus does not dispute that Hayes discloses this limitation. (CRB at 42-43.) Therefore, the ALJ finds that Respondent have shown by clear and convincing evidence that Hayes discloses this limitation.

(3) *"the memory device being configured to defer sampling data that corresponds to the first write command until a strobe signal is detected, delaying for a first time period after issuing a write command"*

The evidence shows that there is some delay period after the module 9 sends a write command to the memory device by asserting WR, "then [module 9] will drive data onto DAL [31:0]." (RX-4268 at 7:42-43; 9:58; *see also* 19:57-59 ("The byte mask, ***write***, address strobe and data strobe signals perform the same functions on the memory array bus 21 as they did on the local bus 17.") (emphasis added); RX-5429C.0125-26.) Rambus does not dispute that Hayes discloses this limitation. (CRB at 42-43.) Therefore, the ALJ finds that Respondents have shown by clear and convincing evidence that Hayes discloses this limitation.

(4) *"after delaying for the first time period, issuing the strobe signal to the memory device to initiate sampling of a first portion of the data by the memory device"*

The evidence shows that a Data Strobe ("DS") is sent to the memory device to indicate that the data on the signals lines is valid and that the memory device can initiate sampling data. (RX-5429C at Q358.) Hayes teaches that a "Data Strobe line (DS) provides timing information for data transfers . . . . During a write cycle, the bus master [memory controller] asserts DS to indicate that [the data bus] contains valid write data." (*Id.* at 7:56-65; 19:57-59 ("The byte mask, write, address strobe and ***data strobe*** signals perform the same functions on the memory array bus 21 as they did on the local bus 17.") (emphasis added).). This was further corroborated during reexaminations of the '405 Patent and the '353 Patent reexamination, which found that the "DS signal let[s] the memory know when to start to read/write data" and initiate sampling. (RX-4246.0010-12; RX-5357.0014)

Rambus argues that the data strobe (DS) disclosed in Hayes is not the claimed "strobe signal" because it merely identifies the type of information on the bus and does not initiate sampling of data by the memory device. (CRB at 42-43.) The evidence shows that Hayes discloses a bus master that "asserts DS, ***indicating that the data is valid*** on DAL [31:0]." (RX-

4268.0014 at 7:61-64 (emphasis added).) Rambus relied on a similar disclosure for its infringement analysis, namely that the DQS signal "is the signal that is used to tell the receiver that ***data is valid on the bus***, so not you can clock those data into . . . its registers." (CX-9543C at 246-47 (emphasis added).) Rambus cannot construe "strobe signal" in two different ways to prove infringement and avoid invalidity. *See, e.g.*, *Amazon.com, Inc. v. Barnesandnoble.com, Inc.*, 239 F.3d 1343, 1351 (Fed. Cir. 2001) ("'A patent may not, like a "nose of wax," be twisted one way to avoid anticipation and another to find infringement.'") (quoting *Sterner Lighting, Inc. v. Allied Elec. Supply, Inc.*, 431 F.2d 539, 544 (5th Cir. 1970) (citing *White v. Dunbar*, 119 U.S. 47 (1886))). Therefore, the ALJ finds that Respondents have shown by clear and convincing evidence that Hayes discloses this limitation.

e) Farmwald

Respondents argue that Farmwald anticipates claims 1, 2, 4, 5, 12, 13, 20, 21, and 24 of the '109 Patent. (See RX-4269; RX-5429C at Q366-384.) Farmwald '037 claims priority back to U.S. Application No. 07/510,898, which was filed on April 18, 1990. (See RX-4269.0001.) Therefore, Farmwald '037 is prior art under § 102(e). It is important to note that the only elements of claims 1, 2, 4, 5, 12, 13, 20, 21, and 24 of the '109 patent that Przybylski argues are not disclosed in Farmwald '037 are the elements concerning the signal (or code) that indicates when the memory is to begin sampling. (Tr. at 2717:10-2719:7; CX-10765C at Q379, 397-99.)

As Staff correctly noted, Respondents' arguments as to the Farmwald '037 are substantially the same as arguments made by nVidia in the prior 661 Investigation. The October 2011 hearing in this investigation did not introduce any significant, new evidence related to Farmwald '037 that would lead to a different outcome in this evidentiary hearing. (Jacobs, Tr. 1063:01-1066:09; CX-10765C, Przybylski Rebuttal Q&A 371-402.) Therefore, for the same

reasons the ALJ found that the Farmwald reference in the 661 Investigation failed to anticipate the Barth Patents, he similarly finds that the Farmwald '037 fails to anticipate. Specifically, the evidence shows that AccessType [0] does not provide the "control information" or "operation codes" because it cannot be considered separate and apart from AccessType [1:3] bits. (CX-10765C.0084-85; *see also* 661 ID at 54-55.) Second, storing a delay value in an access register is not the claimed providing a signal that "indicates when the memory device is to begin sampling write data." (HTr. 1063:1-1065:6; CX-10765C.0085, 87, 89-90; *see also* 661 ID at 53-55.) The Barth Patent specification specifically distinguishes the claimed invention from prior art systems where the timing of data transfer is dictated by the timing of the request for the data transfer based on a value stored in a register. (JX-3 at 10:21-33.) The specification also identifies the use of a delay value as an alternative embodiment from the claimed signal embodiment, explaining that the alternative, unclaimed "value" embodiment does not use a strobe signal. (JX-5 at 10:52-56; CX-10765C.0087-88; *see also* 661 ID at 55-56.) Third, the evidence shows that claim 1 of the '109 Patent does require specific order. (JX-5 at 8:67-9:2; CX-10765C.0086-87.) Farmwald '037 transmits its value *before* what Respondents allege meets the providing a "code which specifies that a write operation be initiated." (CX-10765C.0086-87; RX-4269.0022 at 6:46-48.) Claim 1 recites the opposite order. (CX-10765C.0086-87.)

Therefore, the ALJ finds that Respondents have failed to show by clear and convincing evidence that Farmwald '037 anticipates the '109 Patent.

f) SyncLink

Respondents argue that SyncLink anticipates claims 11-13 of the '353 Patent and claims 1, 20 and 24 of the '109 Patent. (RIB at 75-77.)

The ALJ finds that SyncLink fails to anticipate for the same reasons Farmwald '037 fails to anticipate. SyncLink discloses a packet-based communications system that is similar in many respects to that of the Farmwald '037 patent discussed above and the Farmwald '755 patent previously asserted in the 661 Investigation:

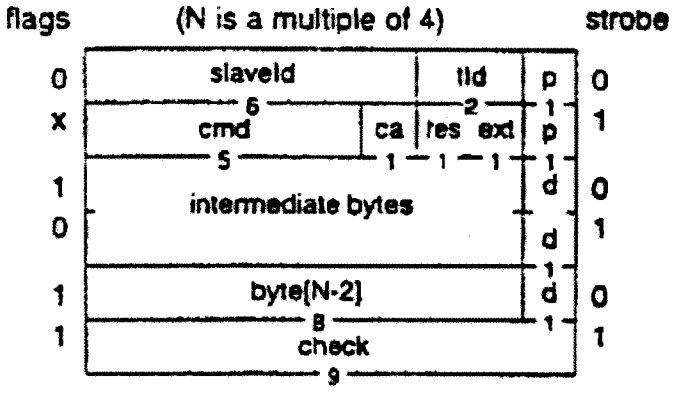


Figure 19—Packet framing

(RX-4270C.0043; *see also* CX-10765C, Przybylski Q/A 412.) The ALJ finds that the the "flags" signal in SyncLink that Respondents contend fails to corresponds to the strobe signal/signal limitation of the asserted Barth patent claims. The evidence shows that the "flags" signal in SyncLink merely indicates "intermediary bytes," such as address information, and thus fails to initiate sampling in the manner called for in the asserted claims. (CX-10765C, Przybylski Q&A 417) Therefore, the ALJ finds that Respondents have failed to show by clear and convincing evidence fails to show anticipation by the SynchLink. (*See id.* at Q&A 403-426; *see also* Jacobs, Tr. 1071-1081.)

The Dally Patents[14]

g) Effective Prior Art Date

The Respondents in their pre-hearing brief and post-hearing reply brief dispute the decision of the U.S. Patent & Trademark Office to grant Dr. Dally the benefit of a pre-filing conception/reduction to practice date. (*See* RPB at 222-224; RRB at 63-64.) However, the failure by Respondents to raise the issue in their initial post-hearing brief means that they have waived the issue. Moreover, the ALJ finds that even considering Respondents' half-hearted efforts to raise this issue in their reply brief simply do not show why it is even necessary to decide the issue. As the Staff points out, the Respondents failed to put forward any invalidity arguments where the priority date question plays any dispositive role. But even if it was relevant the ALJ agrees with Staff that the evidence fails to support the Respondents' position on priority. Accordingly, the ALJ declines Respondents' invitation to upset the U.S.P.T.O.'s decision to award the Dally patents their priority date.

h) Level of Skill in the Art

Rambus contends that a person having ordinary skill in the art during the relevant time frame of the Dally patents would have at least a bachelor's degree in Electrical Engineering or a related field and approximately three years post-baccalaureate experience working on high-speed signaling interfaces. (CX-10764C.0006.) Respondents assert that this person would have at least a Bachelor's degree in Electrical Engineering (EE) plus seven years of industry experience in the EE field, at least a Master's degree in EE plus three years of industry experience in the EE field, particularly in the field of integrated circuits, digital transmission, and communication systems. (RX-5431C at Q/A 13-14.) The ALJ does not detect a huge difference between the

[14] *Prima facie* obviousness arguments and motivations to combine for the references considered in the anticipation section are included with those references in this section rather than as a separate section. The secondary consideration analysis will take place in the obviousness section proper *infra.*

parties' proposed definitions of a person of ordinary skill. Indeed, this dispute does not appear to be definitive in the parties' invalidity analysis in any way.

Rambus's proposed definition would have a person with fewer years of experience, but that experience would be much more focused than Respondents' propose. The ALJ believes that the level of skill in the art likely lies between the two proposals, but closer to Rambus's proposed definition. The ALJ agrees with Respondents that a person of ordinary skill would likely have a bit more experience than under Rambus's proposal, but the ALJ believes that Rambus is correct that the person's area of skill would be relatively focused. As such, the ALJ finds that the level of skill in the art would have at least a bachelor's degree in Electrical Engineering or a related field and approximately four years post-baccalaureate experience working on high-speed signaling interfaces.

i) Overview

The Respondents allege that the Dally patents are anticipated or obvious in view of eight primary references: Widmer Article (RX-4109); Odysseus (RX-4299C); LSI Logic SeriaLink CWSL500 Technology; DP83840 (RX-2360C); Lau (RX-4106); Wurster (RX-4112); Widmer Patent (RX-2870), and Nakamura (RX-4114).

The Respondents further group these eight references into the following main groups: (1) The Widmer Art (Widmer Article, Widmer Patent, Odysseus, and Ewen Article); (2) LSI SeriaLink CWSL500 Technology (SL 500 Art); (3) National Semiconductor Technology (DP83840 and Lau); and (4) Nakamura.

Respondents contend that DP83840, Lau, Wurster, Widmer Patent, and Nakamura anticipate and/or render obvious the asserted Dally claims. As an initial issue, Rambus and Staff argue that Respondents have waived a number of these references under Ground Rules 8(f) and

8(h) by treating the references in such a cursory manner. Rambus and Staff also argue that Respondents violated the instruction in Order No. 51 that "the parties [are to] set forth their contentions with sufficient detail so as to adequately inform the other parties of their positions on the issues for hearing" without trying to "circumvent the page limits by including contentions or arguments as exhibits to their pre-hearing statements." Rambus and Staff argue that in light of this waiver, the ALJ need not consider Respondents' arguments related to the DP83840 device, Lau, Wurster, the Widmer Patent, and Nakamura. The ALJ finds the clearest case of waiver to be the Wurster patent. It is raised only in the briefest passing in Respondents' Initial Post-Hearing Brief (RIB at 200) and in a footnote in Respondents' Reply Brief (RRB at 72 n.45). This is completely inadequate. Accordingly, all arguments regarding Wurster are waived. As for the other references, the ALJ finds the case for a complete waiver to be less clear and will deal with those references in the individual discussion below.

j) The Widmer Art

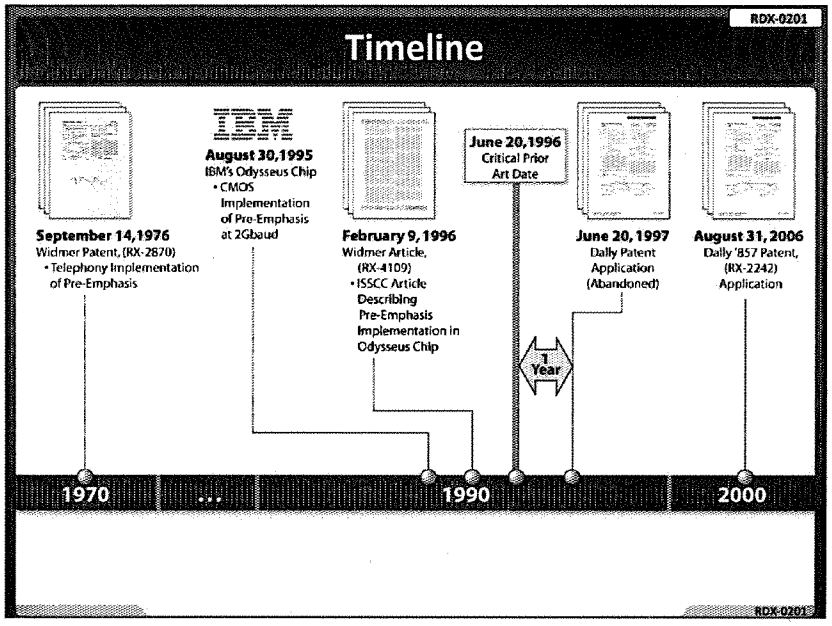
The Respondents' first group of allegedly anticipatory art is referred to herein as the "Widmer Art," and includes the following four exhibits:

Reference	Abbreviated Name	RX Number
Single-Chip 4x500 Mbaud CMOS Transceiver (Feb. 9, 1996) (including the article and separate slides thereon)	Widmer Article	RX-4109

Reference	Abbreviated Name	RX Number
Odysseus Quad-SerDes Functional and Electrical Specification (Aug. 30, 1995)	Odysseus	RX-4299C
U.S. Patent No. 3,980,826	Widmer Patent	RX-2870
Single-Chip 1062Mbaud CMOS Transceiver for Serial Data Communication (Feb. 1995)	Ewen	RX-4125

(1) *Background*

The "Widmer Art" generally relates to the work of Mr. Albert Widmer of IBM from the mid-1970s to the mid-1990s. Demonstrative RDX-0201 provides an overview of the relevant timeframe according to the Respondents:



The first reference, chronologically, in this group, *i.e.*, U.S. Patent No. 3,980,826 (RX-2870) (the "Widmer Patent"), issued on September 14, 1976 and the ALJ finds that this qualifies as prior art to the Dally patents under 35 U.S.C. § 102(b).[15] As Staff explained, this patent is an early example of an equalization mechanism that compensates for high frequency signal attenuation as similarly described and claimed in the Dally patents. (*See* RX-5431C at Q/A 279; CX-10764 at Q/A 223-224.)

Mr. Widmer called his technique predistortion, rather than pre-emphasis, though both were treated synonymously in the field. Predistortion, or pre-emphasis, had become so well known that by as early as 1992, the New IEEE Standard Dictionary of Electrical and Electronics Terms included definitions for these terms:

> **predistortion (pre-emphasis) (system) (transmitter performance).** A process that is designed to emphasize or de-emphasize the magnitude of some frequency components with respect to the magnitude of others. See: **pre-emphasis.**

[15] While the Widmer Patent qualifies as prior art and will be considered as evidence in the record of this case as to whether other references are enabled, the Respondents have not raised, in any detail, any invalidity arguments based on the Widmer Patent. This cursory treatment is inadequate. Accordingly, the ALJ finds any specific invalidity arguments based on the Widmer Patent to be waived.

> **pre-emphasis (pre-equalization).** (1) (General). A process in a system designed to emphasize the magnitude of some frequency components with respect to the magnitude of others, to reduce the adverse affects, such as noise, to subsequent parts of the system, de-emphasis may be applied to restore the original signal with a minimum loss of signal-to-noise ratio.

(IEEE Dictionary, RX-4429 at 999 (emphasis in original).)

As illustrated in RDX-0201 above, Mr. Widmer's work in this field continued after issuance of his patent in 1976 and resulted in an article, *i.e.*, the Widmer Article (RX-4109), that he presented at a conference in February 1996. Specifically, in the 1990s, Widmer and a team at IBM invented a chip, codenamed Odysseus that implemented the pre-distortion technique disclosed in the Widmer Patent in a semiconductor chip that was designed, built, and tested in the U.S. one year prior to the June 10, 1997 priority date. The IBM Odysseus Quad-SerDes Functional and Electrical Specification (August 30, 1995), describes the Odysseus chip. ("Odysseus Specification," RX-4299C at IBM00003.)

The same IBM employees listed on the Odysseus Specification authored a paper describing the Odysseus chip, titled *Single-Chip 4x500Mbaud CMOS Transceiver* (the "Widmer Article"). The Widmer Article was publically presented at the 1996 IEEE International Solid State Circuits Conference ("ISSCC") in San Francisco, demonstrating the operation of the Odysseus chip. (*Compare* RX-4299C at IBM000002 *with* the "Widmer Article," RX4109 at 126.) The conference took place from February 8-10, 1996.

The ALJ finds that the Widmer Article was published in February 1996 at page 126 of Volume 39 of the IEEE's 1996 Digest of Technical papers. The Widmer Article was the seventh paper presented at the seventh session of the 1996 ISSCC, as indicated by the Paper FA7.7 at the top of the first page. (RX-4109 at 120; RX-5431C at Q/A 120.) The Widmer Article was distributed to attendees of the 1996 ISSCC at the conference on February 8-10, 1996 in a bound Digest of Technical Papers.

Based on the associated publication and public dissemination discussed above of the Widmer Article in February 1996, the ALJ finds that the article qualifies as prior art to the Dally patents under 35 U.S.C. § 102(b).

Respondents seek to further supplement the Widmer Article with slides that Respondents contend were presented as part of the article at the IEEE conference in whose proceedings the article was included. Respondents also rely on a set of slides describing this work that Respondents contend were presented at the conference, on February 9, 1996. Respondents argue that the slides used that day, February 9, 1996, which they contend Widmer was the primary drafter, were also published in February 1996 at pages 94-95 of the "Slide Supplement 1996" to the Digest of Technical Papers, Vol. 39 and are included in RX-4109. The ALJ finds that, while this is a close case, Respondents have presented clear and convincing evidence that the slides are a printed publication within the meaning of § 102 in part because Mr. Widmer, who was to verify that the slides were presented and publicly disseminated, failed to provide such testimony at the evidentiary hearing. *In re Klopfenstein*, 380 F.3d 1345, 1349 n.4 (Fed. Cir. 2004).

The ALJ finds that as described above the Widmer Article describes a chip with four transmitter circuits, each of which includes an equalization mechanism for high frequency signal attenuation. (*See* RX-5431C at Q/A 127.) In many respects, the Widmer Article is similar to the Widmer Patent in that both disclose equalization mechanisms, but the Widmer Article reflects various shifts in technology from the 1970s timeframe of the Widmer Patent to the 1990s timeframe of the Widmer Article, including a growing interest in implementing circuitry on integrated semiconductor chips rather than as discrete components. (*See* RX-5431C at Q/A 286; Tr. 2414:13-2416:09 (Dr. Singer).)

The ALJ finds that evidence shows that in order to submit and present the Widmer Article at the February 1996 conference, the article had to have been based on a working chip. (*See* RX-5431C at Q/A 205; Tr. 1551:01-07.) The ALJ finds that in the case of the Widmer Article, the working chip was "Odysseus," an IBM product described in "Odysseus Quad-SerDes Functional and Electrical Specification" (RX-4299C; Tr. 1551:08-1552:19; RX-5431C at Q/A 205-206, 208.)

(2) *Enablement of Widmer Article*

As an initial matter, Rambus argues that the Widmer Article cannot anticipate because it is not enabled. The ALJ agrees with Respondents and Staff and finds that the Widmer Article is enabled. *See Am. Calcar, Inc. v. Am. Honda Motor Co.*, 651 F.3d 1318, 1341 (Fed. Cir. 2011) ("To be anticipatory, a reference must describe, either expressly or inherently, each and every claim limitation and enable one of skill in the art to practice an embodiment of the claimed invention without undue experimentation."). The operative question is whether "one of ordinary skill in the art could practice the invention without undue experimentation." *Novo Nordisk Pharms., Inc. v. Bio-Tech. Gen. Corp.*, 424 F.3d 1347, 1355 (Fed. Cir. 2005).

The Widmer Article includes as Figure 1 a block diagram of a "Quartet-transceiver":

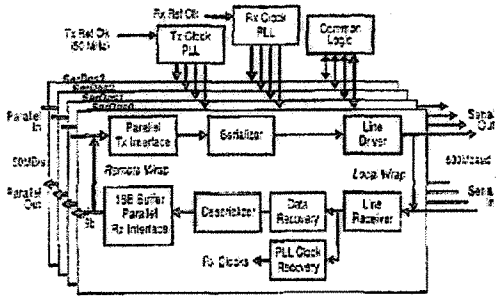


Figure 1: Quartet-transceiver block diagram.

(RX-4109.0002; *see also* Tr. 1534:04-14; RX-5431C at Q/A 127.) The "Quartet" part reflects the fact that there are four separate circuits therein, each circuit having a "Line Driver" and a "Line Receiver" connected to a serial output and a serial input respectively.

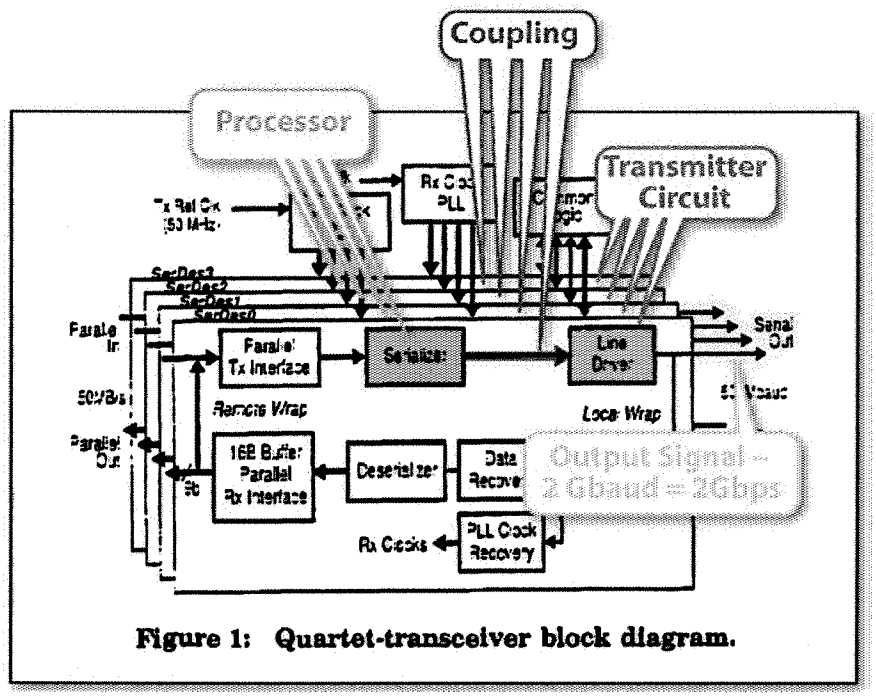


Figure 1: Quartet-transceiver block diagram.

Additional detail regarding the Line Driver and Line Receiver is provided in Figure 4:

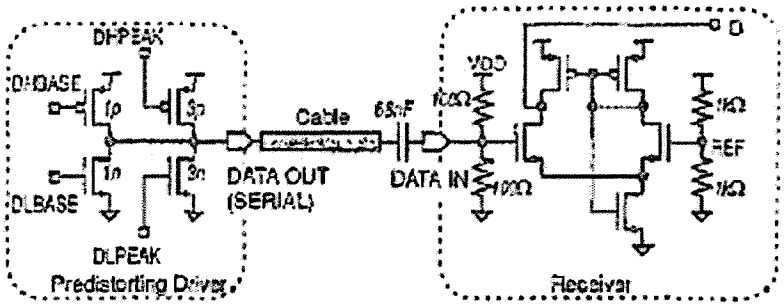


Figure 4: Serial driver and receiver circuits.

(RX.4109.0002, Figure 4; *see also* Tr. 1488:15-19, 1535:15-1538:12; RX-5431C at Q/A 127.) Notably, the label "Predistorting Driver" appears in Figure 4 in reference to the Line Driver shown to the left. (Tr. 1488:20-24, 1535:20-25.) This Predistorting Driver is described in the Widmer Article as follows:

> The links have frequency-dependent attenuation (worst case 9dB at 500MHz) and discontinuities that cause significant signal distortion. The path can include 65cm of card trace and 3.5m of 25AWG, 50Ω coax, along with 50mil-pitch microstrip card-to-card connectors, and dense 4-row 100mil-pitch shielded cable connectors. In the serial driver, a digital predistortion technique boosts high-frequency content, improving the eye opening of the received signal [2]. The low level and high level are each peaked by 50% for a 1-baud interval immediately following any transition. A circuit diagram of the predistorting driver is shown in Figure 4. Control inputs DHBASE and DLBASE set the base driver levels, and DHPEAK and DLPEAK turn on the extra drive required for peaking. The high and low levels are programmable to 1 of 4 levels. Dc-freecoding of serial data permits ac coupling to the receiver, reducing S/N degradation caused by ground shifts.

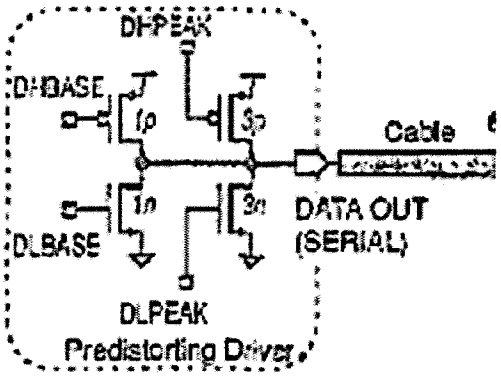
(RX-4109.0001; *see also* Tr. 1488:25-1489:14.) The "References" section of the Widmer Article explains that "[2]" in the paragraph above is a citation to the Widmer Patent previously discussed, *i.e.*, U.S. Patent No. 3,980,826. (*See* RX-4109.0002; *see also* Tr. 1543:06-25.)

The ALJ finds that the evidence shows that the Widmer Article expressly and explicitly refers to the Widmer Patent (RX-2870) in the very paragraph discussing the "Predistorting Driver" of Figure 4. (*See* RX-4109.0002; Tr. 1543:06-25.) Thus, the Widmer Patent would have been an obvious addition to the disclosure of the Widmer Article. For at least this reason, the ALJ finds that the evidence shows that a person of ordinary skill in the relevant art would have found the Widmer Article to contain an enabling disclosure, with the Widmer Patent being exemplary of how equalization can be done using the circuits disclosed and described in the Widmer Article. (*See* RX-5431C at Q/A 134.)

In a related argument, Rambus's expert, Dr. Singer, attempts to distinguish the Widmer Article as requiring the use of off-chip circuitry not disclosed in the reference. (*See* CX-10764C,

at Q/A 82-83.) According to Dr. Signer, the required use of undisclosed, off-chip circuitry confirms his view that the Widmer Article is not enabled. (*See id.* at Q/A 84.) In addition, Dr. Signer contends that the *off*-chip circuitry required by the Widmer Article means it cannot be an anticipatory reference even assuming that it contains an enabling disclosure because the asserted claims all require that the transmitter circuitry be *on*-chip. (*See id.* at Q/A 85.) The ALJ finds that evidence fails to support this purported distinction.

Dr. Singer's argument relates to the DHPEAK and DLPEAK references in Figure 4, a portion of which is reproduced below:



(RX-4109.0002.) Dr. Singer infers that DHPEAK and DLPEAK are necessarily provided from off-chip circuitry because the paragraph describing Figure 4 refers to these two signals as "control inputs." (*See* CX-10764C at Q/A 82-83.) However, the ALJ finds that the evidence shows that to the contrary, a person of ordinary skill in the relevant art would interpret the "input" language as referring to the signals being input *into the Predistorting Driver* portion of the chip as explicitly shown in Figure 4. (*See* RX-5431C at Q/A 133; Tr. 1489:15-1492:16, 1539:05-140:16.) The Widmer Article confirms this interpretation in stating that external (*i.e.*, off-chip) components are *not* required:

> The 9.7x9mm^2 chip has 100k transistors and is fabricated in 0.5μm . . . CMOS with 4 global wiring levels (Figure 6). No external components are required.

(RX-4109.0001; *see also* Tr. 1539:18-1540:02.) As outlined during questioning of Dr. Hassoun, the Widmer Article as a whole thus provides sufficient disclosure to allow one of ordinary skill in the art to implement the Widmer chip without undue experimentation:

JUDGE ESSEX:	Let me interrupt here since this is getting long. Doctor, are you familiar enough with patents to know what a person of ordinary skill in the art is?
THE WITNESS:	Absolutely.
JUDGE ESSEX:	If you looked at [the disclosure in Widmer] and I gave this to a person of ordinary skill in the art, could they come up with the circuit?
THE WITNESS:	Your Honor, a sophomore, junior in electrical engineering would be able to look at that logic and build that simple logic circuit.
JUDGE ESSEX:	Are they somewhere below the ordinary skill?
THE WITNESS:	Way below the ordinary skill.
JUDGE ESSEX:	Let's move on then.
MR. STACH:	Thank you, Your Honor.

(Tr. 1491:25-1492:16; RX-5431C at Q/A 134.) In addition, the evidence shows that it would at least have been obvious to implement the equalization mechanism described in the Widmer Article without the use of off-chip components. (Tr. 1540:17-1541:06.)

Moreover, the ALJ finds that the fact that the inputs to the DHPEAK and DLPEAK transistors are called "inputs" does not support Rambus' assertion that they must come from off-chip. First, the terms "input" and "output" are used throughout the Widmer Article to describe on-chip signals, including those in the Serializer of Figures 1 and 2, which Rambus does not dispute are generated on-chip:

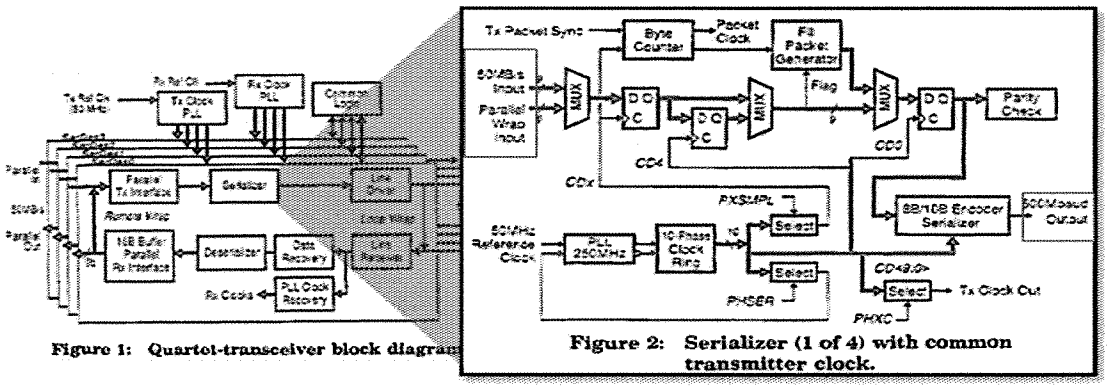


Figure 1: Quartet-transceiver block diagram

Figure 2: Serializer (1 of 4) with common transmitter clock.

(RX-4109 at 127.) Second, Figure 1 shows that signals received and transmitted ***off-chip*** are labeled "in" and "out," not "input" and "output." Rambus surmises that 181 pins are used "as inputs for other functions, such as providing clock signals or the 'common logic' signals shown in Figure 1." (CIB at 219.) The Widmer Article discloses that these clock signals and common logic signals are made available "so output timing is controlled more precisely." (RX-4109 at 126.) However, the ALJ finds that these signals are not related to DHPEAK and DLPEAK and are optional:

> The reference input for the PLL ***can be selected among an external receiver clock, the transmitter reference clock, or the clock recovered from Link#0*** . . . . The PLL includes ***a dummy off-chip driver (OCD) and receiver (OCR)*** to compensate for I/O circuit delay variations so output timing is controlled more precisely.

(*Id.* (emphasis added)) Thus, consistent with the Widmer Article's disclosure that "[n]o external components are required," a user can choose to use or not use these external clock and common logic signals.

Rambus suggests that the Staff improperly relies upon the Widmer Patent as supporting the disclosure of the Widmer Article. (*See* CIB at 217-218.) The ALJ finds this argument unpersuasive. As discussed herein, the Widmer Article is fully enabled and the Widmer Patent is merely an example of how equalization can be performed. Moreover, the record is replete with evidence justifying combining the Widmer Patent with the Widmer Article. (*See* Tr. 1543:06-

1550:04.) Accordingly, any reference to and reliance upon the Widmer Patent is entirely proper and supported by the evidence of record.

For at least these reasons, the ALJ finds that the Widmer Article contains an enabling disclosure of an equalization mechanism as claimed in the Dally patents.

(3) *Odysseus Prior Art*

As part of the Widmer Art, Respondents rely on a document titled "IBM Odysseus Quad-SerDes Functional and Electrical Specifications" to describe an IBM project code-named "Odysseus." (RX-4299C). Each page of this document is labeled "**IBM CONFIDENTIAL.**" (*Id.*) The cover page of the document further emphasizes that this is not a public document, stating:

> This document contains **IBM CONFIDENTIAL** information. All information contained herein shall be kept in confidence. The information should not be divulged to persons other than IBM employees authorized by the nature of their duties to receive such information or individuals and organizations authorized by the IBM Corporation in accordance with existing policy regarding release of company information.

(RX-4299C.0001.) Because it is not a public document, the ALJ finds that Respondents cannot rely on it as prior art.

To the extent Respondents rely on an alleged Odysseus *device* as prior art (as opposed to the Odysseus Functional and Electrical Specifications *document*), they must show, for example, that before the relevant date, the device was made in the United States, sold or offered for sale in the United States, and/or in public use in the United States. 35 U.S.C §§ 102(a), (b), and (g). As Rambus correctly points out, there is no record evidence that the device described in the Odysseus document was ever created in the United States, let alone sold or used in the United States. Instead, Dr. Hassoun speculates that because the Widmer Article and the Odysseus

document list the same authors, the Odysseus device "was the working chip that permitted the Widmer Article to be accepted and presented at ISSCC 1996." (RX-5431C.0187.) However, besides Dr. Hassoun's speculation, Respondents provide no hard evidence to support this conclusion.

As Dr. Singer testified, there are differences in functionality between the chip described in the Widmer Article and the device described in the Odysseus document. (Tr. 2338:22-9.) For example, the Widmer Article and the Odysseus document describe differing levels of emphasis. (*Id.*) Thus, while the technology of the Widmer Article and Odysseus may have been similar in many ways, the evidence demonstrates that Odysseus was not necessarily the chip disclosed in the Widmer Article. Lacking any actual evidence that an Odysseus device was made in the United States, the ALJ finds that Respondents cannot carry their burden by clear and convincing evidence. As for prior invention, the ALJ finds the one document, standing alone, is insufficient to meet the clear and convincing standard of proof. *See Cooper v. Goldfarb*, 154 F.3d 1321, 1330 (Fed. Cir. 1998)

(4) *Invalidity of U.S. Patent Nos. 7,602,857 and 7,715,494 Over the Widmer Article*

The ALJ now turns to a comparison of the Widmer Article to the asserted '857 and '494 Patent claims. The ALJ finds that clear and convincing evidence shows that the Widmer Art (*e.g.*, the Widmer Article) anticipates claims 1, 4-6, 9-10, 24-28, 35-36, 39-44, 47, 53 of the '857 Patent and renders obvious claims 2, 11-13, 31-34, 49-52 of the '857 Patent, either alone or in combination with other art.

(a) Element-by-Element Analysis of Claim 1

The ALJ also finds view, clear and convincing evidence shows that the Widmer Art (*e.g.*, the Widmer Article) anticipates claims 1, 2, 6, and 8 of the '494 Patent and renders obvious claims 3, 25, 26, 30, 39, 40, and 42. Indeed, the majority of the contested limitations in the '494 Patent are substantially identical in scope to corresponding limitations in the '857 Patent, and the private parties rely on the same analyses in their respective pre-trial briefs. Accordingly, the ALJ deals with the two asserted Dally patents together.

A Component Comprising A Semiconductor Chip

Clear and convincing evidence shows that the Widmer Article discloses a component comprising a semiconductor chip. (*See* RX-5431C at Q/A 131.) A micrograph of the chip disclosed in the Widmer Article appears as Figure 6:

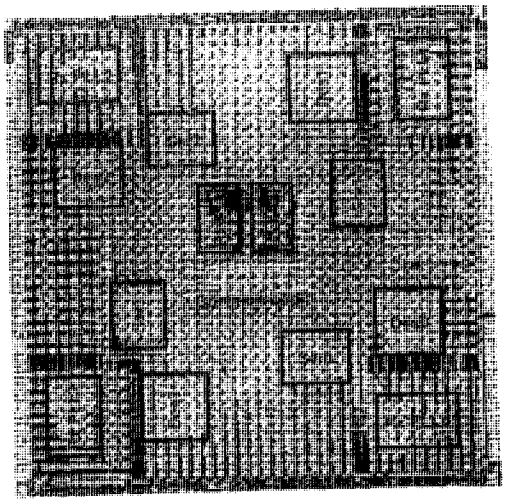


Figure 6: Chip micrograph.

(RX-4109.0003, Figure 6; *see also* Tr. 1550:09-1552:19.)

A Processor Within The Chip

The evidence also shows that the Widmer Article discloses a processor within the chip. (*See* RX-5431C at Q/A 131; Tr. 1534:15-1534:11.) For example, Figure 2 depicts an "8b/10b Encoder Serializer" that processes data for a 500Mbaud Output:

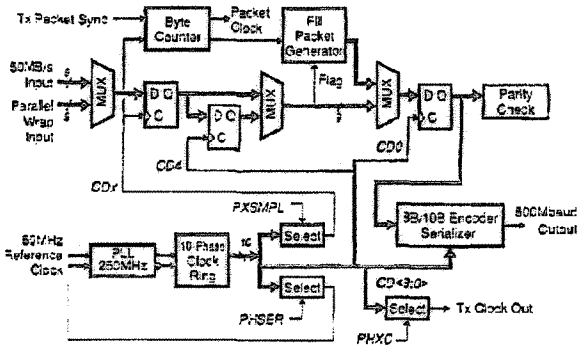
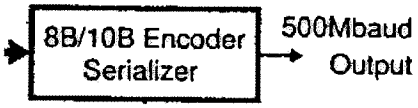


Figure 2: Serializer (1 of 4) with common transmitter clock.

(RX-4109.0002, Figure 2; *see also* Tr. 1534:23-1535:11.) An 8b/10b encoder qualifies as the claimed processor for reasons previously discussed with respect to infringement. (Tr. 1535:09-11.) This is enlarged below:



(RX-4109 at 126-27.)

A Transmitter Within The Chip And Coupled To The Processor To Accept A Digital Input Signal Including A Plurality Of Digital Values From The Processor

The evidence also shows that the Widmer Article discloses a transmitter within the chip and coupled to the processor. (*See* RX-5431C at Q/A 131.) For example, Figure 1 discloses a Line Driver within the chip and coupled to the Serializer (which includes the 8b/10b encoder):

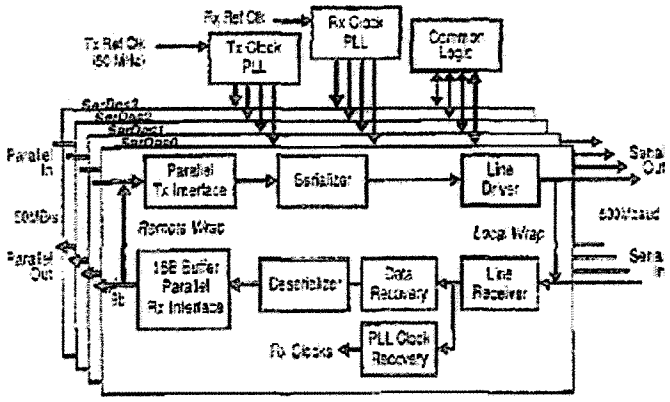


Figure 1: Quartet-transceiver block diagram.

(RX-4109.0002, Figure 1; *see also* Tr. 1535:12-1538:12.) Further, the evidence shows that the "500Mbaud Output" accepted by the Line Driver from the Serializer (*e.g.*, as shown in Figure 2) is a digital input signal including a plurality of digital values. (*See* RX-5431C at Q/A 131.) This is blown up below:

The Widmer Article discloses that the transmitter circuit (*i.e.* line driver) is coupled to the "processor" (*i.e.* the four 8B/10B encoders in the serializer). (RX-4109 at 127.) The line driver is configured to accept a 10B data from the processor (*i.e.* a digital input signal including a plurality of digital values from the processor.)

According to Rambus, the Widmer Article is distinguishable because its transmitter circuit requires off-chip components whereas the asserted Dally patent claims purportedly require that this circuitry wholly reside "within a semiconductor chip or an integrated circuit." (CIB at 218.) Yet, as Staff clearly explains, Rambus's expert Dr. Singer repeatedly waffled on this point during questioning by the Staff. At his deposition, Dr. Singer claimed that components of a transmitter circuit *could* reside off-chip and still fall within the scope of the asserted Dally patent claims:

> Q: Is it your opinion that components of a transmitter circuit could reside off chip and still satisfy the transmitter limitation of the asserted Dally patent claims?
>
> A: It would depend on what you mean by components of. If by components of, we mean critical components to the functionality of? Then, no, I don't believe they could be off chip and still satisfy the claims. On the other hand, if it were the power supply, or some decoupling capacitor or something that wasn't part of the functionality, I guess in that context, I wouldn't call that the transmitter.

(Tr. 2570:21-2571:10.) However, at trial Dr. Singer was resolute in saying that a transmitter circuit with off-chip components could *not* fall within the scope of the asserted Dally patent

claims:

> Q. With respect to your off-chip/on-chip distinction, are the asserted Dally patent claims broad enough to encompass a transmitter circuit with a portion that resides off-chip?
>
> A. No.

(Tr. 2569:10-14.)

On a related point, at his deposition Dr. Singer testified that a person of ordinary skill in the relevant art could *not* tell what constitutes a "critical component" that must reside on-chip (and thus fall within the scope of the transmitter circuit limitation) without looking at an accused product or prior art reference:

> Q: Could a person of ordinary skill in the art tell what a critical component is solely by looking at the asserted Dally patent claims?
>
> A: Without looking at the transmitter in question?
>
> Q: Yes.
>
> A: No. I think one of ordinary skill would have to look at the specific transmitter to know.

(Tr. 2572:09-18.) However, at trial Dr. Singer flipped again in saying that such a person *could* make such a determination without looking at an accused product or prior art reference:

> Q: Can a person of ordinary skill in the relevant art determine the scope of the transmitter circuit limitation in the Dally patent claims without looking at an accused product or prior art reference?
>
> A: Yes.

(Tr. 2571:24-2572:04.)

The ALJ finds that Dr. Singer's inconsistency on this point carries over to his analysis of infringement versus validity. In instances where an Accused Dally Product or an embodiment of the Dally patents requires an associated off-chip component to transmit signals properly, Dr. Singer interprets that component as irrelevant to the analysis. (*See* Tr. 2544:02-2546:22,

2547:21-2552:01, 2553:06-2555:04; *see also* RX-5430C at Q/A 40-47.) The ALJ notes that in contrast, where a prior art product requires an analogous off-chip component, Dr. Signer interprets that component as critical to the analysis. (*See, e.g.* Tr. 2539:15-2544:01, 2546:24-2547:20; CX-10764C at Q/A 83-85.) In the ALJ's view, Dr. Singer's inability to maintain a consistent position on his purported off-chip/on-chip distinction and the corresponding scope of the "transmitter circuit" limitation reflects serious credibility problems that taint his entire analysis.

Moreover, as for the Widmer Article in particular, Dr. Singer's position conflicts with how a person of ordinary skill in the relevant art would have interpreted the article. For example, Dr. Hassoun noted that article explicitly refers to its circuitry as being wholly on-chip:

> Q. Doctor, do you see the DH peak and DL peak at the top and bottom [of RX-4109.0002, Figure 2] which I believe you testified about?
>
> A. Yes, I do.
>
> Q. Are those generated on chip or off chip?
>
> A. On chip.
>
> Q. Why do you say that?
>
> A. Well, the title of the paper is a single chip, but also if you look at column 2 on the bottom, it says specifically, no external components are required. There is no doubt that it is on chip.
>
> Q. Let's see if we can get that paragraph for you. Can I get the first page of the Widmer article [RX-4109.0001] and the last full paragraph. It starts with the "9.7." Is this the paragraph you are referring to?
>
> A. That is.
>
> Q. And what portion of this paragraph were you referring to?
>
> A. If you look at the second sentence, it says, "no external components are required."
>
> Q. Despite this sentence here, do you have an opinion as to whether external components are nonetheless required to generate the DH peak and DL

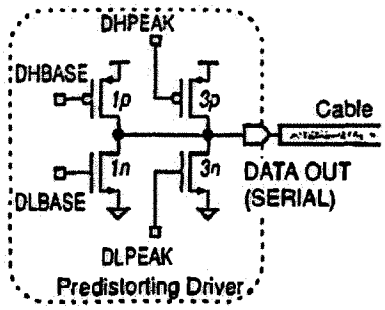
peak signals off chip?

A. It would be a ridiculous thing to do, because at that point, you have signals that are operating -- the current bit and the previous bit are operating at 500 [meg]abit per second, which is a very, very high speed. So for you to take those off chip, build a circuit that has to handle that kind of high speed, and then bring those signals back on chip, that would be a very costly endeavor and it makes no sense whatsoever.

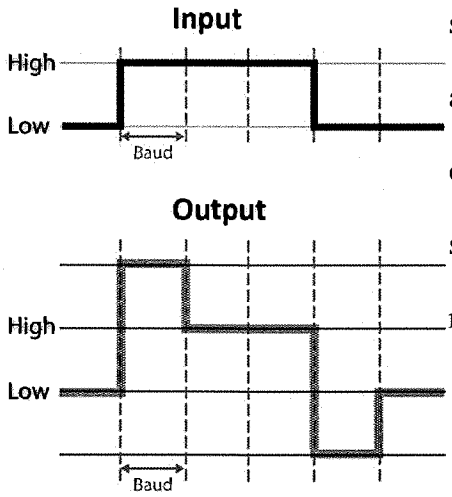
(Tr. 1539:05-1540:16.) In light of Dr. Hassoun's testimony and other evidence of record, the ALJ finds that a person of ordinary skill in the relevant art would have viewed the Widmer Article's circuitry as being *on-chip*.

The Transmitter Circuit Being Operable To Send An Output Signal (With Pre-Emphasis/Pre-Distortion)

Finally, the ALJ finds that the evidence shows that the Widmer Article anticipates or renders obvious a transmitter circuit with an equalization mechanism as claimed (*i.e.*, pre-emphasis/pre-distortion circuitry). (RX-5431C at Q/A 132, 135; Tr. 1535:12-1538:12, 1539:05-1541:06, 1543:06-1550:04.)



The remaining limitations require a transmitter circuit that is operable to "emphasize high frequency components of the output signal relative to low frequency components of the output signal so that (i) an output bit signal of the output



signal . . . has one signal level when the bit value is the same as a bit value represented by a predetermined preceding output bit signal; and (ii) the output bit signal . . . has another signal level when the bit value is different from the bit value represented by the predetermined preceding output bit signal.

The Widmer Article discloses a transmitter circuit using a "predistortion technique [that] boosts high-frequency content, improving the eye opening of the received signal." (*Id.* at 126.) "The low level and high level are each peaked by 50% for a 1-baud interval immediately following any transition." (*Id.*) The Widmer Article also discloses the predistortion circuit that implements pre-emphasis, as shown here. The Widmer Article discloses that "no external components are required" (*i.e.*, the predistortion circuit, as well as all the circuitry required to perform pre-emphasis are found on-chip). (*Id.*) Thus, the ALJ finds that the Widmer Article discloses the remaining limitations of claim 1 by boosting higher components such that there is one signal level after repeated bits (non-peaked signal level) and another signal level after transition bits (50% peaked signal level). (Tr. at 1536:7 to 1540:16.)

Accordingly, the ALJ finds that Widmer anticipates claim 1 of the '857 Patent.

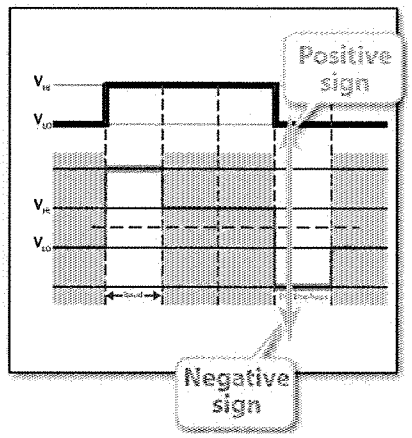
(b) The Remaining Independent Claims of the '857 Patent

The remaining independent claims of the '857 Patent generally capture the same functionality and therefore, are disclosed by the same prior art. For example, claims 24, 35 and 39 require a "component circuit" rather than a processor. A "component circuit" includes a "processor"; thus, the Widmer Article's four 8B/10B encoders of meet this limitation. Claims 24

and 35 require "the transmitter circuit is operable to select each signal level as a function of the digital value represented by that signal level and of the digital values represented by one or more preceding signal levels." The Widmer Article discloses determining the output based on the present digital value and immediately preceding digital value. Moreover, Rambus does not raise any independent arguments against these particular claims. Accordingly, the ALJ finds that the Widmer Article anticipates the remaining independent claims of the '857 Patent.

(c) Independent Claims 1, 25, and 39 of the '494 Patent

The ALJ finds that the independent claims of the '494 Patent are either anticipated or rendered obvious by the same evidence considered above with regards to the other independent claims or rendered obvious by the Ewan article. The independent claims require a transmitter circuit (claims 1 and 25) or a transmitter (claim 39) within a semiconductor chip. (RX-5431C at Q/A 186.) Claim 1 of the '494 Patent requires "the transmitter circuit generating a sign which depends upon the value of the bit represented by such output bit signal and generating a magnitude which is a function of the value of the bit represented by such output bit signal and the values of the bits represented by one or more preceding output bit signals, each output bit signal having sign and magnitude determined by the generated sign and generated magnitude." The Widmer Article discloses generating a sign (DHBASE and DLBASE) and a magnitude (DHPEAK and DHPEAK). (*Id.*) As shown in the pre-emphasized output signal to the left, each output bit has a sign and magnitude determined by DHBASE, DLBASE, DHPEAK, and DLPEAK. (RX-5431C at Q/A 186.)



Accordingly, the ALJ finds that this together with the analysis discussed above for Claim 1 of the '857 Patent, the Widmer Article anticipates claim 1 of the '494 Patent.

(d) Claims 25 and 39 of the '494 Patent

Independent claims 25 and 39 of the '494 Patent include a requirement not found in other asserted claims that the output signal be a *differential* output signal. Claim 25 is representative, and reads in pertinent part:

> a transmitter circuit within the chip, the transmitter circuit being operable to accept a digital input signal including a plurality of bits and send a *differential output signal* including a series of output bit signals, each bit of the digital input signal being represented by a single output bit signal

(JX-121 at 10:42-47 (emphasis added).)

"a differential output signal"

As discussed above, Claims 25 and 39 of the '494 Patent require the additional feature of transmitter with a differential output signal. The Widmer Article cites to the Ewen Article, which explicitly discloses differential signaling.[16] The Widmer Article points the reader to the Ewen Article, stating that the "serializer/deserializer (SerDes) design adopts techniques use previously" in the Ewen Article. (RX-4109 at 126, n.1.) The Ewen Article discloses a 1.062 Gbps high-speed transmitter including a serial driver with differential outputs. (RX-4125 at 32.)

Respondents contend that the Ewan Article is incorporated by reference into the Widmer Article and therefore, they should be considered together for anticipatory purposes. However, as the Federal Circuit has explained, "in order for one document to incorporate another document by reference, the incorporating document must identify the incorporated document with detailed

[16] The Ewen Article, "Single-Chip 1062Mbaud CMOS Transceiver for Serial Data Communication" (February 1995), is authored by many of the same authors as the Widmer Article. (RX-4125 at 32.) The Widmer Article references the Ewen Article in the first footnote and (RX-4125.) The Widmer Article specifically states that it "adopts techniques used previously" in the Ewen Article. (RX-4109 at 127.)

particularity, clearly indicating the specific material for incorporation." *Kyocera Wireless Corp. v. Int'l Trade Comm'n*, 545 F.3d 1340, 1352 (Fed. Cir. 2008). A mere cross-reference to another document, like the Widmer Article's reference to Ewen, is not sufficient. *Id.* ("[V]ague referencing practice is hardly sufficient to meet this court's legal requirements for incorporation"). Thus, the Widmer Article/Ewen Article combination cannot be used for purposes of anticipation.

However, while the combination cannot be used for anticipation, the ALJ finds that it would have obvious to one of ordinary skill to implement differential outputs. The ALJ finds that a person of ordinary skill would understand that an output signal can either be single-ended or differential. (RX-5431C at Q/A 194.) In differential signaling, the signal consists of two wires that carry complementary signals (*e.g.*, if one signal is "high," the other is "low"). (Tr. 1486:20-22.) A single-ended signal consists of a single wire that carries one of the differential signals, but not the complement. (Tr. 1487:5-7.) To switch from a differential to single-ended output, one could simply ignore the complementary signal. Similarly, to switch to a differential signal, one merely needs to generate the complement of the single-ended signal.

The ALJ finds that clear and convincing evidence also shows that it would have been obvious to modify the system disclosed in the Widmer Article to implement differential signaling as called for in claims 25 and 39. Specifically, while the Widmer Article discloses single-ended signaling, it explicitly references the Ewen article which used differential signaling instead. (Tr. 1486:01-1488:14.) The ALJ finds that the evidence shows that it would have been obvious to a person of ordinary skill in the relevant art to implement well known differential signaling techniques such as Ewen with the system of the Widmer Article where increased speed

and noise tolerance were bigger concerns than reduced pincount. (*See* RX-5431C at Q/A 194; Tr. 1552:20-1553:23.)

Rambus alleges "the Widmer Article teaches away from differential signaling due to the increased wire count required to implement differential signaling." (CIB at 227.) But "[a] known or obvious composition does not become patentable simply because it has been described as somewhat inferior to some other product for the same use." *In re Gurley*, 27 F.3d 551, 553 (Fed. Cir. 1994).

But the ALJ finds that the Widmer Article teaches that a single-ended output can be used to reduce wire count. One of ordinary skill would have been well aware of this and other benefits and drawbacks of single-ended versus differential signaling. (RX-5431C at Q/A 194.)

Moreover, the ALJ finds that a person of ordinary skill would understand the well benefits of using one type of signaling versus the other. (RX-5431C at Q/A 194.) For example, the Widmer Article discloses using single-ended outputs to reduce wire count. (RX-4109 at 126.) A person of ordinary skill in the art would understand the benefits of using differential signaling. For example, Dally discloses using differential signaling in part because it has better "noise immunity" than "any single-ended approach." ('RX-2239.0198.) The Dally Patents do not expressly teach single-ended signaling, but the independent Asserted Claims cover singled-ended, as well as, differential signaling. Similarly, the Widmer Article discloses using differential outputs signals to one of ordinary skill in the art.

This conclusion is further supported by Dr. Hassoun's testimony at trial where he explained at trial that engineers routinely switch between single-ended signaling versus differential signaling depending on the particular constraints they are facing when designing a given system:

Q. Would a person of ordinary skill in the art choose to implement single-ended signaling versus differential signaling in some contexts?

A. Yes, absolutely.

Q. Why?

A. Well, it depends on your constraints. For example -- or what problems are you going to solve? For example, if you look at the Widmer article, they made a choice to implement single-ended because they had wiring constraint. They were designing the chip for a particular application that had that particular constraint. If you didn't have that constraint, you might choose to implement differential signaling in there, to make, for example, your receiver design a little bit easier. It doesn't have to work so hard at figuring out the high and the low. It can use differential signaling. So there is -- those are examples of considerations you would have, whether you would use differential or single-ended.

(Tr. 1552:25-1553:23.) Thus, the ALJ finds that while the chip discussed in the Widmer Article may have been designed with single-ended signaling for a pin-count sensitive application, it would have been obvious to a person of ordinary skill in the relevant art to modify that chip to use differential signaling in other applications in which pin-count was *not* a significant concern. Stated another way, system constraints define whether single-ended or differential signaling is used rather than vice versa. Accordingly, the ALJ finds that independent claims 25 and 39 are invalid for obviousness.

(e) Claims 2, 31, and 49 of the '857 Patent, Claim 3 of the '494 Patent

Unlike claim 1 of the '857 Patent and claim 1 of the '494 Patent, the ALJ finds that clear and convincing evidence fails to show that the Widmer Article anticipates claims 2, 31, and 49 of the '857 Patent and claim 3 of the '494 Patent. However, clear and convincing evidence does

show that claim 2 would have been obvious in view of the Widmer Article alone or in combination with other art.[17] This claim reads:

> 2. The component as claimed in claim 1 wherein the transmitter circuit is operable to send the output signal with an output frequency of at least 1 GHz and a bandwidth greater than 100 MHz.

(JX-120 at 8:64-67.) With respect to claim 2, there appear to be different interpretations of the claim that materially impact the validity analysis. Rambus is of the view that claim 2 specifies a 1 Gbps output data rate "for a single channel NRZ waveform over one line" – *i.e.*, a single, serial channel. (*See* Tr. 2326:04-08.) By contrast, the Respondents are of the view that claim 2 is broad enough to read on a system where a 1 Gbps output data rate is split over multiple channels, as allegedly recited in dependent claim 5. (RX-5431C at Q/A 155-157; Tr. 1564:15-1567:06.) The ALJ finds that the evidence supports Rambus's interpretation of the claims *in part*.

More specifically, the claims must be viewed collectively to fully understand the nature of the output data rate called for in claim 2. Starting with claim 1, this claim broadly recites a processor coupled to a transmitter circuit that sends an output signal – *i.e.*, one processor, one transmitter circuit, and one output signal. (*See* JX-120 at 8:45-63.) Dependent claim 5 adds a requirement that the transmitter circuit of claim 1 be coupled to one or more I/O connections. (*See* JX-120 at 8:45-63.) In this system, the I/O connections are redundant such that the same "output signal" is duplicated on however many I/O connections are utilized, with the output data rate being merely that of a single transmitter circuit. (Tr. 2322:01-2323:13.) This fact is verified by contrasting claim 5 with claims 11 and 12. Namely, claim 11 requires the processor of claim 1 be coupled to at least one "additional" transmitter circuit which sends an "additional" output

[17] Claims 31 and 49 of the '857 Patent and claim 3 of the '494 Patent include an identical limitation of "the output signal with an output frequency of at least 1 GHz and a bandwidth greater than 100 MHz," so this analysis is equally applicable to them as well.

signal – *i.e.*, one processor, multiple transmitters, and a corresponding number of output signals. (*See* JX-120 at 9:26-31.) Claim 12, which depends from claim 11, adds the requirement that the multiple transmitter circuits be coupled to a plurality of I/O connections. (*See id.* at 9:32-35.) Thus, claim 12 envisions a system different from claim 5 in which the I/O connections are *not* redundant. Namely, in claim 12 there are multiple transmitter circuits coupled to a common processor, each transmitter circuit providing an output signal on an I/O connection, the aggregate data rate of the multiple output signals collectively representing the total data rate for the overall system. (*See* Tr. 2326:20-2327:07.) It bears noting, however, that both claim 5 *and* claim 12 specify the "output signal" in terms of a given transmitter circuit. This supports Rambus's view that the "output signal" term recited in other claims, such as dependent claim 2, likewise refers to that of a given transmitter circuit rather than that of a combination of transmitter circuits as proposed by the Respondents.

Applying this understanding to the Widmer Article, the individual transceivers disclosed therein have an output data rate of 500 Mbaud – *i.e.*, one half the 1 Gbps output data rate required under a proper interpretation of this claim. (*See* RX-4109.0002, Figure 1.) Moreover, the ALJ finds that one cannot consider the data rates of all four of the transceivers as a collective (*i.e.*, 4 x 500 Mbaud = 2 Gbaud) because: (1) such a configuration no longer satisfies the requirement of claim 1 that *the* transmitter circuit (*e.g.*, the Line Driver in the Widmer Article) be coupled to *the* processor (*e.g.*, the 8b/10b Serializer in the Widmer Article); and (2) the data rate recited in claim 2 is specified in terms of "the output signal" of a given transmitter circuit rather than multiple output signals from multiple transmitter circuits. Thus, the ALJ finds that clear and convincing evidence fails to show anticipation of claim 2 by the Widmer Article.

However, the ALJ finds that clear and convincing evidence does show obviousness in view of the Widmer Article either alone or in combination with other art. For example, the Widmer Article refers to a secondary reference (Ewan, RX-4125) that its design "adopts techniques" from:

> The serializer/deserializer (SerDes) design adopts techniques used previously but includes functions to support transparent operation and relax timing constraints at the system interface[1].

(RX-4109.0001; *see also* RX-4109.0002 ("[1] Ewen, J.F. et al. 'Single-Chip 1062MBaud CMOS Transceiver for Serial Data Communication,' ISSCC Digest of Technical Papers, pp. 32-33, Feb., 1995").) Ewen discloses a chip with a serial output at 1062 Mbaud:

> This work implements the media independent functions specified in the emerging ANSI fibre channel standard at 1062.5Mbaud. Integrated onto a single CMOS chip are: two phase-locked loops (PLL)for clock generation and clock recovery, a selectable 1B or 2B parallel interface with corresponding multiplexer and demultiplexer for parallel-to-serial and serial-to-parallel conversion, word alignment logic for byte synchronization, 8B/10B coder and decoder, and high-speed differential CMOS PECL drivers and receivers for the serial I/0.

(RX-4125.0001; *see also* RX-5431C at Q/A 160; Tr. 1497:17-1498:05.) The evidence shows that it would have been obvious to modify the system disclosed in the Widmer Article to achieve an output data rate of 1.062 Gbps as disclosed in Ewen, particularly in light of the need for increasingly fast data transmission techniques in certain implementations. (Tr. 1498:06-13, 1501:08-15.)

The ALJ has already found the independent claims that claims 31 and 49 of the '857 Patent and claim 3 of the '494 Patent depend on invalid as anticipated by the Widmer Article. There is no material difference between these independent claims and claim 1 of the '857 Patent depends on. Rambus also raises no unique arguments for claims 31 and 49 of the '857 Patent and claim 3 of the '494 Patent. Accordingly, the ALJ finds that the analysis above for claim 2 of

the '857 Patent applies with equal force to claims 31 and 49 of the '857 Patent and claim 3 of the '494 Patent.

Accordingly, the ALJ finds that claims 2, 31, and 49 of the '857 Patent invalid as obvious in light of the combination of the Widmer Article and Ewan Article.

(f) Dependent Claims 30 and 42 of the '494 Patent

Dependent claims 30 and 42 of the '494 Patent recite a similar, but slightly different variation of this limitation. Exemplary claim 30 reads:

> 30. The circuit of claim 25, where the series of output signals is transmitted by the transmitter onto a signal path at a rate of at least 400 megahertz.

(JX-122 at 10:65-67.) While parties treat the "rate" aspect of '494 Patent claims 30 and 42 the same as the "output frequency" aspect of '494 Patent claim 3 and '857 Patent claims 2, 31, and 49, claims 30 and 42 of the '494 Patent requires a transmitter circuit that outputs at a rate of "400 megahertz," which is *slower* than the "1 GHz" required to meet the latter set of claims. This distinction is relevant to the Widmer Article, which discloses a transmitter circuit that outputs at 500 MHz, which is less than 1 GHz but more than 400 MHz.

More specifically, the Widmer Article discloses a Quartet transceiver in which each transceiver has an output data rate of 500 MBaud. (*See* RX-4109.0002, Figure 1.) Because 500 MBaud is less than the "1 GHz" required to satisfy the output frequency limitation under both of the proposed constructions for that limitation, the ALJ has determined that the Widmer Article does not anticipate claim 3 of the '494 Patent and claims 2, 31, and 49 of the '857 Patent. Because 500 MBaud is *greater* than the "400 megahertz" required to satisfy the rate limitation of these claims as construed by the ALJ, the ALJ finds that the Widmer Article teaches this limitation. The ALJ has already determined that independent claims 25 and 39 are obvious in light of the combination of Widmer and Ewan. Rambus appears to agree as it only disputes

anticipation of those claims under its flawed interpretation of "output frequency" and "rate."(*See* CIB at 222.) Accordingly, the ALJ finds that claims 30 and 42 are also rendered obvious for the reasons stated above and for the reasons stated above with respect to independent claims 25 and 39.

(g) Claims 11, 32, and 50 of the '857 Patent

The ALJ finds that clear and convincing evidence fails to show that the Widmer Article anticipates claim 11, 32, and 50 of the '857 Patent. However, the ALJ finds that clear and convincing evidence does show that the additional limitations of these claims would have been obvious in view of the Widmer Article alone or in combination with other art.

More specifically, claim 11 (which is representative of claims 11, 32, and 50) requires "at least one additional transmitter circuit within the chip" that is also "coupled to the processor" of claim 1. (*See* JX-120 at 9:26-32.) According to the Respondents, the four individual transceivers correspond to the "additional transmitter circuit" of claim 11. (*See* RIB at 153-154.) However, as discussed in detail with respect to claim 2, the Respondents have not identified a common processor coupled to the four individual transceivers as claimed. (*See* RX-5431C at Q/A 174-175; Tr. 1492:20-1494:15.) Rather, the Respondents appear to be relying on the 8b/10b Encoder Serializer within a given transceiver as the claimed "processor" even though that particular component is not coupled to multiple transmitter circuits as claimed. (*See* RX-5431C at Q/A 174-175; Tr. 1492:20-1494:15.)

Nonetheless, the ALJ finds that clear and convincing evidence shows that it would have been obvious to implement the system disclosed in the Widmer Article in a configuration with multiple transmitter circuits coupled to a common processor, particularly given the Widmer Article's disclosure of a Quartet-transceiver system that could be used with an upstream

processor.[18] (*See* Tr. 1542:05-1543:05.) Moreover, Rambus does not appear to raise any validity arguments specific to the additional limitations added in claim 11. (*See* CIB at 218-228.)

(h) Claim 8 of the '494 Patent

The ALJ finds that clear and convincing evidence shows that the Widmer Article discloses the "reprogrammable" limitation added by way of dependent claim 8 of the '494 Patent. For example, the Widmer Article explains that "[t]he high and low levels are programmable to 1 of 4 levels." (RX-4109.0001; *see also* RX-5431C at Q/A 192-193.) Rambus does not contest this limitation.

(i) Additional Dependent Claims of the '857 and '494 Patent

Clear and convincing evidence also shows that the Widmer Article discloses the limitations added by way of the remaining claims. (RX-5431C at Q/A 136-154, 169-173, 176, 177, 179, 180, 182-185. 187-191, 195, 196, 198-200.) In fact, Rambus does not appear to raise any validity arguments specific to these limitations added by way of these claims. (*See* CIB at 218-228.) Accordingly, the ALJ finds that clear and convincing evidence shows that the remaining dependent claims of the '857 Patent and the '494 Patent are rendered invalid by the Widmer Article.

The remaining claim limitations are discussed below:

(j) Pre-emphasis: claims 4, 9, 10, 26, 41, 42, 47 and 53 ('857 Patent) and 2 and 6 ('494 Patent)

This group of dependent claims includes limitations requiring specific forms of pre-emphasis. These claims are anticipated or rendered obvious based on the same evidence shown

[18] This analysis also applies as to dependent claims 32 and 50, which similarly call for multiple transmitter circuits coupled to a common component circuit (*e.g.*, a processor).

for claim 1 of the '857 Patent. Claims 4 and 26 of the '857 Patent and claim 2 of the '494 Patent recite emphasizing signal levels after transition bits related to repeated bits. Claims 9, 10 and 47 of the '857 Patent recite the each input bit is represented by one of the signal levels in the output signal. Claims 41, 42 and 53 of the '857 Patent and claim 6 of the '494 Patent recite selecting the signal level as a function of the present bit and one or more preceding or the immediately preceding bits. All of these limitations are disclosed by the Widmer Article, which teaches a transmitter circuit that emphasizes the output signal after transition bits relative to repeated bits by comparing the present bit value the immediately preceding bit value. (*See* RX-5431C at Q/A 137, 139, 140, 143, 149, 150, 152, 153, 154, 188-190.) Accordingly, for these reasons, and for the reasons stated above with respect to the independent claims on which these claims depend, the ALJ finds that the Widmer Article anticipates claims 4, 9, 10, 26, 41, 42, 47 and 53 ('857 Patent) and 2 and 6 ('494 Patent).

(k) I/O connections: claims 5, 12, 27, 33, 43 and 51 ('857 Patent)

The "I/O connections" claims (claims 5, 12, 27, 33, 43 and 51) of the '857 Patent require that the chip have "I/O connections and the transmitter circuit is coupled to one or more of the I/O connections to send the output signal through the one or more I/O connections." As shown above in relation to claim 1 of the '857 Patent, the Widmer Article discloses that the chip has I/O connections and the transmitter circuit is coupled to a cable through an I/O connection. (RX-4109 at 127; *see also id.* at 95 ("22 signal I/Os").) Therefore, the Widmer Article discloses the I/O connections limitation. (*See, e.g.*, RX-5431C at Q/A 138, 144, 151.) Rambus does not appear to dispute that this limitation is present in the Widmer Article.

The ALJ has already determined that independent claims 1, 24, and 39 of the '857 Patent are anticipated by the Widmer Article. As discussed above, the I/O connection limitation is also

disclosed in the Widmer Article. Claims 5, 27, and 43 depend on claims 1, 24 and 39 respectively and add only the I/O connection limitation. Accordingly, the ALJ finds that claims 5, 27, and 43 are anticipated as well.

As for claims 12, 33, and 51, they depend on claims 11, 32, and 50 respectively. The ALJ has found claims 11, 32, and 50 invalid as obvious in light of the Widmer Article. Claims 12, 33, and 50 only recite one additional limitation over the claims that have already been found invalid. That limitation is the I/O connection limitation discussed above. Because the I/O limitation is found in Widmer Article, claims 12, 33, and 51 are also obvious in light of Widmer for the reasons discussed with respect to claims 11, 32, and 50. Accordingly, the ALJ finds that claims 12, 33, and 51 are obvious.

(l) "nonmodulated": claims 6, 28 and 44 ('857 Patent)

This group of claims require sending the output signal in nonmodulated form. As shown in relation to claim 1 of the '857 Patent, the Widmer Article discloses an output signal that is in nonmodulated form. (*See also* RX-4109 at Fig. 7.) Further, there is no description in the Widmer Article of a modulated output (*e.g.*, using the output signal of the transmitter to modulate a carrier signal). Therefore, the Widmer Article discloses the nonmodulated claims. (*See, e.g.*, RX-5431C at Q169.)

Claims 6, 28, and 44 are dependent claims. They depend on claims 5, 27, and 43 respectively. Claims 5, 27, and 43 have been found to be anticipated (*See* "I/O Connection Claims" discussion above). The only limitation that claims 6, 28, and 44 add is the non-modulated limitation, which is present in the Widmer Article. Accordingly, claims 6, 28, and 44 are also found anticipated by the Widmer Article.

(m) multiple transmitters/parallel stream of data/parallel bus: claims 13, 34, and 52 ('857 Patent) and 26 and 40 ('494 Patent)

Claims 13, 34 and 52 of the '857 Patent recite output signals representing a parallel stream of data from the processor. Claims 26 and 40 of the '494 Patent recite sending output bit signals on lines of a parallel bus. All of these claims are disclosed by the four 500 Mbps transmitters of the Widmer Article, which can be configured to receive a parallel stream of data from the 8B/10B encoders and output bit signals on a parallel bus. (RX-4109 at 126-27.) Thus, the Widmer Article discloses the additional limitations of these claims. (*See*, *also*, RX-5431C at Q/A 175-76, 195, 198.) Rambus does not dispute the presence of these particular limitations.

Claims 13, 34, and 52 depend on claims 11, 32, and 50 respectively. The ALJ has found claims 11, 32, and 50 invalid as obvious in light of the Widmer Article. Claims 13, 34, and 52 only recite one additional limitation over the claims that have already been found invalid. That limitation is the parallel data stream from the processor limitation discussed above. Because the parallel data stream from the processor is found in Widmer Article, claims 13, 34, and 52 are also obvious in light of Widmer for the reasons discussed with respect to claims 11, 32, and 50. Accordingly, the ALJ finds that claims 13, 34, and 52 are obvious.

(n) processor: claims 25, 36 and 40 ('857 Patent)

The claims recite that the "component circuit" be a processor. As discussed above in relation to claim 1 of the '857 Patent, the Widmer Article discloses four 8B/10B encoders that make up the processor. Thus, the Widmer Article discloses the processor limitation. (*See*, *e.g.*, RX-5431C at Q/A 142.) Claims 25, 36, and 40 are dependent claims. They depend on claims 24, 35, and 39 respectively. The ALJ has found that claims 24, 35, and 39 are anticipated by the Widmer Article. The only additional limitation that claims 25, 36, and 40 have over claims 24,

35, and 39 is the processor limitation. Accordingly, because the Widmer Article discloses all of the limitations of claims 25, 36, and 40, they are anticipated by the Widmer Article.

k) The SL500 Art

In addition to the Widmer Art described above, the Respondents also rely on several invalidity theories stemming from a chip called the "SerialLink SL500" (which incorporates the "CWSL500 Technology" or "CWSL500 core") that was allegedly "conceived, reduced to practice, used, and offered for sale well before the applicable bar dates associated with the Dally patents." (RIB at 165-166.) The parties dispute whether the SL500 art even qualifies as prior art. The ALJ will turn to that issue first.

Respondents contend that the SL500 Art is prior art under §§ 102(b) and (g). However, Rambus contests whether the SL500 Art is available as prior art. (*See* CIB at 232-233; 240-241). The Staff agrees with Respondents that, at the very least, the SL500 Art qualifies as prior art under § 102(b).

(1) *Availability of the SL500 Art as Prior Art*

The ALJ finds that the evidence shows that the SL500 Art indeed constitutes prior art to the Dally patents under 35 U.S.C. § 102(b) and/or § 102(g). More specifically, the ALJ finds that the SL500 Art to qualifies as prior art based on LSI having offered to sell the SL500 Art to customers Seagate and Cabletron in 1995 and based on LSI having conceived and reduced to practice the claimed invention (as implemented in the SL500 Art) prior to the June 1996 critical date of the asserted Dally patents. As discussed below, the ALJ finds that the evidence in this case shows that LSI manufactured the first SL500 chips in [redacted] and provided prototype SL500 chips to Seagate no later than [redacted], both occurring prior to the June 1996 critical date of the asserted Dally patents. Thus, LSI was the first to reduce to practice the claimed

invention. The evidence also shows that LSI conceived of the claimed invention (*e.g.*, as to be implemented in a CWSL500 core) at least by [redacted], and was diligent in reducing to practice the invention as part of ultimately developing and producing the prototype chips provided to Seagate and Cabletron no later than [redacted]. For at least these reasons, the SL500 Art also qualifies as a prior invention of the Dally patents by LSI under 35 U.S.C. § 102(g)(2). Moreover, the ALJ finds that the evidence shows that LSI also offered the device for sale to both Seagate and Cabletron more than one year before Dally filed for his patent. Thus, it also qualifies as prior art under § 102(b).

(a) Prior Invention Under 102(g)

As discussed below, the evidence in this case shows that LSI manufactured the first SL500 chips in [redacted] and provided prototype SL500 chips to Seagate no later than [redacted], both occurring prior to the June 1996 critical date of the asserted Dally patents. Thus, LSI was the first to reduce to practice the claimed invention. The evidence also shows that LSI conceived of the claimed invention (*e.g.*, as to be implemented in a CWSL500 core) at least by [redacted], and was diligent in reducing to practice the invention as part of ultimately developing and producing the prototype chips provided to Seagate and Cabletron no later than [redacted]. For at least these reasons, the SL500 Art also qualifies as a prior invention of the Dally patents by LSI under 35 U.S.C. § 102(g)(2).

Legal Standard

A patent claim also is invalid if before the patentee's invention, "the invention was made in this country by another inventor who had not abandoned, suppressed, or concealed it. In determining priority of invention under [102(g)], there shall be considered not only the respective dates of conception and reduction to practice of the invention, but also the reasonable

diligence of one who was the first to conceive and last to reduce to practice, from a time prior to conception by the other." 35 U.S.C. § 102(g)(2). "[A] challenger [to a patent's validity] such as [LSI] has two ways to prove that it was the prior inventor: (1) it reduced its invention to practice first . . . , or (2) it was the first party to conceive of the invention and then exercised reasonable diligence in reducing that invention to practice." *Mycogen Plant Sci., Inc. v. Monsanto Co.*, 243 F.3d 1316, 1332 (Fed. Cir. 2001). Claims of prior invention must be corroborated. *See Finnigan Corp. v. ITC*, 180 F.3d 1354 (Fed. Cir. 1999). Whether corroborating evidence is sufficient when considering all of the pertinent evidence is evaluated under the "rule of reason." *Loral Fairchild Corp. v. Matsushita Elec. Indus. Co.*, 266 F.3d 1358, 1363 (Fed. Cir. 2001). Under a "rule of reason" analysis, "it is not necessary to produce an actual over-the-shoulder observer. Rather, sufficient circumstantial evidence of an independent nature can satisfy the corroboration requirement." *Cooper v. Goldfarb*, 154 F.3d 1321, 1330 (Fed. Cir. 1998) (finding reduction to practice proven by the inventor's testimony corroborated by testimony of his co-workers that he had told them of his reduction to practice, and that they had seen him obtain materials of the type necessary to practice the invention.); *see also Lacotte v. Thomas*, 758 F.2d 611, 613 (Fed. Cir. 1985 (affirming finding of reduction to practice, stating "[t]he testimony of Thomas, the inventor, and the written evidence of his reduction to practice in his notebook, are corroborated by independent circumstantial evidence of his withdrawal of supplies to practice the invention, as well as independent corroborating testimony of his associate, Lee.").

The date of conception "defines the legally operative moment of invention." *Invitrogen Corp. v. Clontech Labs., Inc.*, 429 F.3d 1052, 1063 (Fed. Cir. 2005). Conception requires an actual recognition of that which constitutes the inventive subject matter. *See id.*

The earliest possible filing date of the parent application to which the Dally patents claim

priority is June 20, 1997. Dally alleges a conception date of [redacted] in his invention disclosure (RX-4147C; RX-4148C), this disclosure form does not demonstrate conception of all the claims of the Dally Patents although Rambus does not press the point in its briefs. Absent proof to the contrary, Dally's conception date is the filing date of the parent application to which the Dally Patents claim priority, June 20, 1997. However, it is irrelevant because LSI has alleged a conception date well before Rambus's alleged conception date, so if LSI can establish conception and reduction to practice, the SL 500 art will be prior art regardless of Rambus's date of invention. *See Mahurkar v. C.R. Bard, Inc.*, 79 F.3d 1572, 1577 (Fed. Cir. 1996) ("Stated otherwise, priority of invention goes to the first party to reduce an invention to practice unless the other party can show that it was the first to conceive the invention and that it exercised reasonable diligence in later reducing that invention to practice." (quotation marks omitted)).

LSI's Conception of SL 500 Art

The ALJ finds that LSI Logic had conceived of the SL 500 Art as early as [redacted] when it was informing its customers that the CWSL500 technology included the emphasis functionality. (RX-4173C.0030-31.) The ALJ finds that at this time, LSI Logic also had defined the basic characteristics of the CWSL500 technology and was offering the CWSL500 for sale to its customers as discussed in greater detail below. (RX-4150; RX-4128; and RX-4156C.0015.) The ALJ also finds that by [redacted], LSI Logic had developed documentation and product manuals detailing the functionality and characteristics of the CWSL500. (*See e.g.*, RX-4116C.0002-0014; RX-4130.0007-60.) These documents illustrate that LSI Logic recognized the inventive subject matter [redacted] and appreciated that which they had invented. By [redacted], LSI Logic engineers had completed SPICE

configuration files and transistor level schematics. (RX-4116C.0044-191; RX-4143C and RX-4144C [redacted] RX-4520C; *see also*, RX-5430C at Q/A 379-381, 486-490, 498-505.) LSI Logic also had performed simulations on the CWSL500 circuitry that depicted the emphasis functionality. (RX-4092C; (RDX-350); RX-4094C; *see also* RX-5430C at Q/A 379-391.) Accordingly, the ALJ finds LSI Logic conceived of the invention by [redacted] at the latest. However, as previously described, LSI Logic's conception occurred much earlier, and in any case, earlier than Dally.

LSI's Reduction to Practice of the SL 500 Art

The ALJ finds LSI Logic reduced its invention of the CWSL500 technology to practice prior to Dally. Establishing an actual reduction to practice requires that (1) an inventor constructed an embodiment or performed a process that met all the limitations of the claims, (2) the inventor determined that the prior invention worked for its intended purposes, and (3) that the inventor engaged in sufficient testing to demonstrate reduction to practice in instances where testing is required to demonstrate that the invention worked for its intended purpose. *See z4 Techs., Inc. v. Microsoft Corp.*, 507 F.3d 1340, 1352 (Fed. Cir. 2007) (*citing Cooper v. Goldfarb*, 154 F.3d 1321, 1327 (Fed. Cir. 1998)).

Independent third-party evidence corroborates LSI Logic's reduction to practice of the SL500 chip. For example, the SL500 is alluded to in a [redacted] email correspondence between [redacted]. (RX-4176C.) [redacted]

[redacted] Accordingly, the CWSL500 was reduced to practice in the SL500 chip as early as [redacted] and no later than [redacted].

LSI Logic also published a paper in February 1997 related to the CWSL500 and its emphasis functionality. (RX-4107.) Because publication in the ISSCC requires that the author have manufactured a working chip, LSI Logic unquestionably had developed a functional SL500 chip that included emphasis. (Tr. 1675:16-1680:13.) In fact, for publication in February 1997, LSI Logic would have had to submit its paper in September 1996. (*Id.* at 1608:11-22.) Indeed, the design of the CWSL500 had been completed for almost a year and the first SL500 chips had been fabricated well before Dally presented his research. [redacted]

[redacted]

(RX-2772C.0103.) Accordingly, as is further corroborated by Drs. Dally and Poulton, LSI Logic. (*See also* RX-5422C at Q/A 80-86.; RX-2772C.0077-78; RX-2772C.0102-103.)

The ALJ also finds that LSI Logic also reduced the CWSL500 technology to practice in the Shemp chip in [redacted]. (RX-4142.0002, Schedule Table.) In particular, the ALJ finds that LSI Logic worked on layout and tape out of the Shemp chip from [redacted] and sent the first prototype chips to Cabletron in [redacted]. (*Id.*) As set forth above, the ALJ

finds that the Shemp chips incorporated four CWSL500 cores and anticipated each and every claim of the Dally Patents. (RX-4128.0002.) Rambus argues that the Shemp chip did not include the emphasis functionality. In support of this assertion, Rambus cites to a document that [redacted]. (RX-4511C.) However, as testified by Dr. Hajimiri, however, the [redacted] is not indicative of anything. Indeed, this document reflects [redacted]. (Tr. at 1625:24-1626:24.)

LSI's Diligence in Reducing SL 500 to Practice

LSI was diligent in reducing the SL500 Technology to practice as demonstrated by the following evidence:

- LSI Logic began offering the CWSL500 technology for sale to its customers as early as [redacted] and continued offering the CWSL500 technology to its customers throughout [redacted]. (*See* RX-4156C.0015; RX-4128; RX-4142C.)

- LSI Logic regularly met with its customers to inform them of the CWSL500 technology and provided information regarding the CWSL500's functionality. (*See, e.g.*, RX-4173C.0010, 23, 30-31, 48-49, and 65-67.) LSI Logic also provided its customers with product literature. (RX-4150; RX-4149.)

- From [redacted], LSI Logic engineers were diligently running simulations to verify the CWSL500 circuitry and design of the SL500 chip. (RX-4092C (RDX-350); RX-4094C; RX-4520C.)

- In [redacted], LSI Logic prepared CWSL500 product manuals and additional documentation. (RX-4116C.0002-14; RX-4130.0007-60.)

- From [redacted], LSI Logic engineers were diligently designing and developing the Shemp chip for Cabletron that incorporated the CWSL500. (*See* RX-4136; RX-4137C; RX-4138; RX-4519C.)

- In January 1996, LSI Logic informed the general public that it had received SL500 chips back from fabrication as is evidenced by its [redacted]. (RX-4176C.)

[redacted]

- In [redacted], LSI Logic worked on layout and tape out of the Shemp chip. (RX-4142C; RX-4138; RX-4519C.)

- In [redacted], LSI Logic delivered the first prototype Shemp chips to Cabletron. (RX-4142C.)

- July and September 1996, LSI Logic began publishing articles regarding the CWSL500 technology. (RX-4123; and RX-4107 (while this article was published in February 1997, testimony supports that it would have had to be submitted in September 1996 for inclusion in the publication (Tr. 1608:11-22.).)

Therefore, because LSI Logic (1) conceived of the invention disclosed in the Dally Patents (*i.e.*, the CWSL500 technology); (2) diligently reduced the invention to practice; and (3) did not abandon, suppress, or conceal its invention of the CWSL500 technology, each and every asserted claim of the Dally Patents is invalid under § 102(g).

Rambus's Arguments in Response

In response to this evidence, Rambus argues that this section of the Patent Act does not apply because "neither the SL500 nor the Shemp chip met all the limitations of the asserted Dally claims" and because the equalization circuitry "was not functional" in these chips. (*See* CIB at. 241.) According to Rambus, these deficiencies preclude a finding that LSI (and/or its personnel) qualifies as having previously invented the subject matter of the asserted Dally patent claims under 35 U.S.C. § 102(g). Neither argument is persuasive.

The first argument is really whether the claims anticipate. The ALJ perceives the proper inquiry as whether the SL 500 prior art has the features LSI claims it does. If LSI can prove the SL 500 has the particular features it claims it does, then those features will be entitled to the priority date that LSI claims. The ALJ will then undertake the second step below of determining whether LSI's SL 500 Art anticipates or not.

Turning next to whether the equalization circuitry in the SL500 Art worked as intended, Rambus relies on the testimony of its expert Dr. Singer to establish [redacted] (CIB at 234 (citing CX-10764C at Q/A 363-367; Tr. 2584:09-2586:12).) A similar argument is made by Rambus as to [redacted] (*See* CIB at 236 (citing Tr. 2587:04-2589:14).) [redacted] (*See* CIB at 235 (citing RX-5430C.0018-19; RX-4171C.0006-7).) Rambus surmises that LSI never actually produced a version of the SL500 Art with working equalization circuitry, and certainly did not provide such a chip to Seagate or

Cabletron. (*See* CIB at 236-237.) The ALJ finds that Rambus's arguments are contrary to the weight of the evidence.

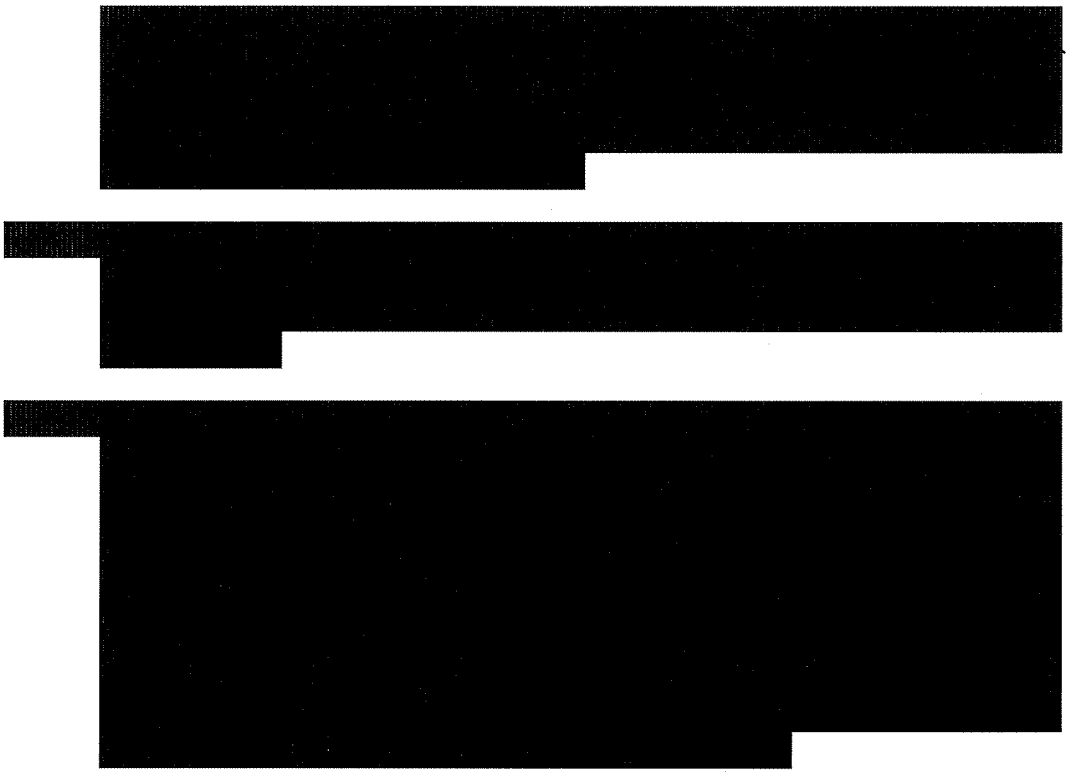
First, the ALJ finds that clear and convincing evidence confirms that LSI conceived of using equalization circuitry within the SL500 Art in the [redacted]. For example, [redacted]:

(RX-4116C.0007.) Similarly, a "SeriaLink™ SL500 Document Set," also from the [redacted] timeframe, describes this same set of inputs:

RX-4130.0047. [redacted]. (*See* RX-4173C.0048; Tr. 2517:15-2518:13, 2520:10-19 (discussing RX-4173C.0048).) LSI further confirmed that this equalization circuitry would, in fact, perform pre-emphasis/de-emphasis as claimed in the Dally patents by performing simulations on the conceived design:

(RX-4094C; *see also* RX-5430C at Q/A 388-390 [redacted] While the particular circuit diagrams/layouts of the equalization circuitry that LSI ultimately chose to implement within the SL500 Art may not be of record, such circuitry was well known in the prior art as exemplified by the Widmer Article, the Widmer Patent, and other art of record. Thus, the ALJ finds that clear and convincing evidence shows that LSI conceived of using equalization circuitry within the SL500 Art in the [redacted] timeframe.

To the extent that Rambus disputes whether the simulations show *working* versions of equalization circuitry, Rambus's arguments are premised on the flawed reasoning of its expert Dr. Singer. As Respondent LSI's expert Dr. Hajimiri testified at trial, [redacted]



(CX-5430C at Q/A 495-496.) Dr. Hajimiri's testimony is corroborated by an article from 1997, in which a version of the SL500 Art with equalization circuitry therein was described in considerable detail. (*See* RX-4017 (article entitled "A 1.0625 Gbps Transceiver with 2x-Oversampling and Transmit Signal Pre-Emphasis" and including reference to "The GigaBlaze(TM) SerialLink^{TM} CWSL500 transceiver core.").) As Dr. Hajimiri explained, the IEEE conference at which this article was presented required that there be a working version of the chip, thus confirming his view that working equalization circuitry was indeed ultimately produced by LSI. (*See* Tr. 1675:10-1680:13.)

Lastly, Rambus correctly observes that some of the documents on which LSI relies [redacted] (*See* CIB. 235-236 (citing RX-5430C.0018-19; RX-4171C.0006-0007).) However, the ALJ finds that this observation is not relevant. Much like the equalization circuitry in certain of the Accused Dally Products, the SL500 Art as conceived by LSI contained [redacted]

[redacted]. (*See* RX-5430C at Q/A 466.) This fact is verified [redacted] Proof that the SL500 Art discloses working equalization circuitry that *could* be enabled invalidates even the asserted method claims because, unlike an infringement analysis under Section 271, an invalidity analysis under Section 102 does not require evidence of a prior art product actually being used in the claimed manner. *See* Manual of Patent Examining Procedure, § 2112.02 (Process Claims) (8th Ed. With July 2008 Revisions) (citing *In re King*, 801 F.2d 1324, 1326-1327 (Fed. Cir. 1986)).

Accordingly, Rambus's arguments against finding that the SL 500 Art is prior art under § 102(g) are rejected.

(b) Public Sale

Legal Standards

With respect to the offers for sale alleged to be prior art, "the § 102(b) on-sale bar applies when two conditions are met before the critical date: (1) the product is the subject of a commercial offer for sale, and (2) the invention is ready for patenting." *August Tech. Corp. v. Camtek, Ltd.*, 655 F.3d 1278, 1289 (Fed. Cir. 2011) (citing *Pfaff v. Wells Elecs., Inc.*, 525 U.S. 55, 67 (1998)). "An invention can be found to be 'ready for patenting' in at least the following ways: by proof that it was reduced to practice, or by proof that the inventor had prepared drawings or other descriptions of the invention that were sufficiently specific to enable a person skilled in the art to practice the invention." *Cargill, Inc. v. Canbra Foods, Ltd.*, 476 F.3d 1359, 1368 (Fed. Cir. 2007). In addition, in certain circumstances an invention may qualify as prior art even if it is not ready for patenting at the time the offer is made. *See August Tech.*, 655 F.3d at 1289 ("The issue presented in this case is whether the invention must be ready for patenting at

the time the alleged offer is made. We conclude that it does not."). So long as an "offer for sale is extended and remains open, a subsequent conception will cause it to become an offer for sale of the invention as of the conception date." *Id.* at 1289.

As discussed below, the ALJ finds that the evidence in this case shows that LSI offered to sell the SL500 Art to both Seagate and Cabletron [redacted], that the SL500 Art was ready for patenting prior to the June 20, 1996 critical date of the asserted Dally patents, and that the offers to sell remained open at that time. Thus, the SL500 Art qualifies as on-sale bar prior art to the Dally patents under 35 U.S.C. § 102(b).

Background Regarding SL 500 Sales

The ALJ finds the following background facts regarding the sales of the SL 500. The "CWSL500 core" refers to the "core ware" of the SL500 Art. (Tr. 1607:01-18.) A "core" constitutes a design that can subsequently be instantiated in an actual chip as discussed previously with respect to infringement. LSI personnel developed equalization circuitry within a CWSL500 core sometime in the [redacted], and reduced to practice a corresponding SL500 chip with a CWSL500 core instantiated therein sometime [redacted] (RX-5430C at Q/A 519; Tr. 1607:19-25.) LSI also produced a BDSL500 evaluation board that contained an SL500 chip in this general timeframe. (Tr. 1608:01-04.) Thus, the three critical aspects of the SL500 Art consist of: (1) CWSL500 cores; (2) SL500 chips; and (3) BDSL500 evaluation boards. That a working SL500 chip (with associated cores and evaluation boards) was indeed ultimately produced by LSI is verified by a February 1997 article presented at the International Solid-State Circuits Conference on the SL500 chip, which required a working chip for presentation of an article. (*See* RX-4107.) The particular article here (RX-4107) refers

to a SL500 chip with programmable pre-emphasis functionality, thus confirming that a working SL500 chip was produced in the [redacted] timeframe. (RX-4107; Tr. 1675:10-1680:13.)

The Cabletron Prior Art Issues

Turning to the Cabletron issues in particular, evidence of record as to the commercial offer for sale includes a [redacted]. (RX-4128.0002; RX-5430C.0293 at Q/A 23-25; RX-4137C.0001; RX-4138.0004; Tr. 1685:18-1686:09, 1687:19-1688:09.) [redacted] (RX-4142C.0001 (Business Table).) The chip was eventually shipped to Cabletron roughly one year later:

[redacted]

(Tr. 1683:04-09.)

The record includes considerable detail as to the development schedule for the chip sold to Cabletron. For example, the record includes a [redacted] Thus, the evidence supports the Respondents' argument that LSI offered to sell an SL500 chip to Cabletron that was "ready for patenting" before the priority date of the asserted

Dally patents. (RX-5430C.0294 at ¶ 30; Tr. 1611:25-1613:05; 1619:08-1620:09, 1620:25-1624:17, 1681:15-1682:03, 1683:04-09.)

The Cabletron Offer

Turning to the Cabletron offer, [redacted] (*See* CIB at 234 (citing RX-4128.001; Tr. 1620:25-1622:09).) According to Rambus, [redacted] that this offer to Cabletron cannot be a qualifying offer for sale under 35 U.S.C. § 102(b) because [redacted] (CIB at 234.) Again, whether an offer was accepted is irrelevant as the Patent Act only requires that a qualifying offer be made – *not* that it further be accepted. *See* 35 U.S.C. § 102(b). Here, the ALJ finds that clear and convincing evidence shows an offer for sale that qualifies under Section 102(b) based on conception (and ultimately reduction to practice) of the invention as embodied by the Shemp chip having occurred while the offer to Cabletron remained open. For example, the evidence includes [redacted]

[redacted]. (RX-4142C.0002, Schedule Table.)

For at least these reasons, Rambus's arguments that LSI did not make a qualifying offer to sell Shemp to Cabletron should be rejected.

The Seagate Prior Art Issues

Turning to Seagate, evidence of record as to the commercial offer for sale to Seagate includes a [redacted]

(RX-4156C.0011; *see also* RX-5430C.0290, at ¶¶1-4.) [redacted]

[redacted]

(RX-4149.0011.) That an actual SL500 chip was indeed ultimately provided to Seagate is demonstrated by [redacted] Thus, the ALJ finds that the evidence supports the Respondents' argument that an SL500 chip circuitry was offered for sale to Seagate and "ready for patenting" (*e.g.*, used by Seagate (during testing)) before the priority date of the asserted Dally patents. (RX-5430C.0292 to 0293, ¶¶ 21-22; Tr. 1611:25-1613:05; 1615:19-1616:01.)

Rambus argues that [redacted] on which the Respondents rely include nothing more than [redacted] and thus cannot constitute an offer for sale under 35 U.S.C. §102(b). (CIB at 233.) However, the ALJ agrees with Staff that even assuming that Rambus's characterization of the [redacted] is accurate, additional evidence of record is more specific to the

SL500 Art in particular. [redacted]

(RX-4149.0004.) Indeed, the ALJ notes that [redacted]

Given the above, the ALJ finds that the evidence as a whole demonstrates that in [redacted] LSI indeed offered to sell an SL500 chip to Seagate that included equalization circuitry.

Rambus's argument regarding the relevance of the offer for sale is based on a misleading cite to only a portion of the *August Tech.* opinion, wherein the Federal Circuit explained that "there is no offer for sale until such time as the invention is conceived." CIB at 233. (quoting *August Tech. Corp. v. CamTek, Ltd.*, 655 F.3d 1278, 1289 (Fed. Cir. 2011)). The larger

paragraph from which this quote was taken explains that subsequent conception will cause a prior offer to qualify as an offer for sale under 35 U.S.C. § 102(b):

> [W]e conclude that an invention cannot be offered for sale until its conception date. Hence, if an offer for sale is made and retracted prior to conception, there has been no offer for sale of the invention. In contrast, if an offer for sale is extended and remains open, a subsequent conception will cause it to become an offer for sale of the invention as of the conception date. In such a case, the seller is offering to sell the invention once he has conceived of it. Before that time, he was merely offering to sell an idea for a product.

August Tech., 655 F.3d at 1289. Such a series of events occurred here. Namely, as discussed above clear and convincing evidence shows an offer for sale [redacted] followed shortly thereafter by conception (and ultimately reduction to practice) of an SL500 chip that embodies the invention claimed in the Dally patents. That the conception occurred while the offer for sale remained open is demonstrated by [redacted] who ultimately tested an SL500 chip provided by LSI, which would not have taken place had LSI retracted its prior offer. (*See* RX-4175C.0065 to .0074.)

Ready For Patenting

While LSI Logic was offering the CWSL500 technology to Seagate and Cabletron, the CWSL500 technology also was ready for patenting. First, [redacted]

[redacted] RX-4094C; RX-4092C (RDX-350); *see also* RX-5430C at Q/A 379-391.)

LSI Logic engineers diligently ran hundreds of simulations [redacted] while finalizing the CWSL500 circuitry and laying out the SL500 chip. (RX-4520C.) [redacted] (RX-4520C.)

As discussed above, the CWSL500 technology was reduced to practice no later than [redacted] in the SL500 chip. (RX-4176C.) The SL500 was a silicon implementation of the CWSL500. (RX-4130.0020.) As is standard practice in the industry, LSI Logic would have tested the SL500 chips to ensure they operated properly prior to distributing them to customers. (Tr. at 1644:5-1645:18.) [redacted] Accordingly, the ALJ finds that the CWSL500 was ready for patenting in [redacted], and no later than [redacted] based on the reduction to practice of the CWSL500 circuitry in the SL500 chip. As such, the ALJ finds that the CWSL500 was ready for patenting while LSI Logic was offering to sell the CWSL500 technology to Seagate and Cabletron.

Rambus's Arguments

Rambus argues that Respondents cannot show that there was an offer to sell the CWSL500 technology to Seagate that would constitute an on-sale bar to the asserted Dally Patents. (CIB at 233.) The ALJ finds that despite Rambus's assertions to the contrary, the [redacted]

[redacted] Additional documentation and the testimony of Dr. Hajimiri further confirm that these [redacted] reflect an offer to sell the CWSL500. (*See e.g.*, RX-5430C.0290-92; RX-4150; RX-4149.) Accordingly, LSI Logic began offering the CWSL500 technology to Seagate as early as [redacted]

Rambus also argues that there is no evidence that an offer to Seagate remained open through the time the CWSL500 technology became ready for patenting. (CIB at 233.) However, [redacted] Thus, the evidence shows that LSI Logic continued to offer to sell the CWSL500 technology to Seagate while the technology was ready for patenting.

Rambus also argues that Respondents cannot show that there was an offer to sell the CWSL500 technology to Cabletron that would constitute an on-sale bar to the Dally Patents. (CIB at 234.) The ALJ finds that this argument ignores evidence showing [redacted] (RX-4142C.001-2; Tr. 1680:24-1683:9; *see also* RX-4136, RX-

4138.) The ALJ finds that not only did the offer not expire, it resulted in a final contract and LSI shipping the Shemp chips that incorporated the CWSL500 cores. Accordingly, the ALJ finds that there can therefore be no dispute as to whether LSI Logic's offer to sell the CWSL500 technology to Cabletron satisfies the requirements of § 102(b).

(2) *Invalidity Of U.S. Patent No. 7,602,857 and Over The SL500 Art*

The ALJ finds that clear and convincing evidence shows that the SL500 Art discloses each and every limitation of asserted claims 1, 2, 3, 4-6, 9, 10, 24-28, 31, 35, 36, 39, 41-44, 47, 49 and 53 of the '857 patent, and also renders obvious asserted claims 11-13, 32-34, and 50-52. The invalidity analysis set forth in this section is based largely on the following documents, all of which describe the SL500 chip and/or the CWSL500 core instantiated within that chip, and collectively provide sufficient detail to show that the chip/core was "ready for patenting" prior to the critical date of the asserted Dally patents:

Exhibit Number	Document Description
RX-4520C	[redacted]
RX-4176C	[redacted]

Exhibit Number	Document Description
RX-4175	[redacted] RX-4175C.0065-73; RX-4175C.0076-77 (excerpts included as RDX-4031 and RDX-4074) [redacted]. RX-4173C.0159-160 (excerpts included as RDX-4032).
RX-4130C	[redacted]
RX-4116C	[redacted]
RX-4094C	[redacted]. RDX-350 (excerpt provided in RDX-4076) [redacted]

Exhibit Number	Document Description
RX-4092C	[redacted]

(*See also* RX-5430C at Q/A 376-392.) Additional supporting documentation is identified by Dr. Hajimiri in his direct witness statement. (*See id.* at Q/A 51.)

(a) Element-by-Element Analysis of Claim 1 of the '857 Patent

A Component Comprising A Semiconductor Chip

Clear and convincing evidence shows that the SL500 Art discloses a component comprising a semiconductor chip. (RX-5430C at Q/A 394.) More specifically, a CWSL500 core was instantiated within sample SL500 chips, and provided on BDSL500 evaluation boards to various customers. *Id.* at Q/A 374-375, 392-393. [redacted]

(RX-4130.0021.)

Moreover, the CWSL500 itself was a high-speed serial interface core that consisted of fully defined, optimized and reusable circuits. (RX-4130.0015.) LSI Logic designed the CWSL500 core for integration and implementation on semiconductor chips. (RX-4130.0021,

Fig. 1.3.) [redacted]. (RX-4130.0020.) [redacted]. (RX-4128 [redacted] RX-4156C.0015 [redacted].) In these customer-specific ASICs, [redacted] (RX-4130.0015-16.) Thus, the ALJ finds that there can be no doubt that the CWSL500 technology, and LSI Logic's interactions involving the CWSL500, necessarily were directed towards implementing the CWSL500 on semiconductor chips and the SL 500 technology meets this limitation.

A Processor Within The Chip

Clear and convincing evidence also shows that the SL500 Art discloses (and/or renders obvious) a processor within the chip. (*See* RX-5430C at Q/A 395-396.) [redacted] (*See* RX-4130C.0020 [redacted]; *see also* RX-4130.0018 [redacted] For example, the SL500 chip included [redacted]. (*See e.g.*, RX-4130.0020 [redacted]

[redacted]

(RX-4128.0002, Table 1.)

A Transmitter Within The Chip And Coupled To The Processor To Accept A Digital Input Signal Including A Plurality Of Digital Values From The Processor

The ALJ finds that clear and convincing evidence also shows that the SL500 Art discloses (and/or renders obvious) a transmitter within the chip and coupled to the processor. (*See* RX-5430C at Q/A 397-398.) Moreover, this is discussed at least at RX-4130C.0017:

[redacted] In addition, a transmitter is shown in Figure 2.1 below:

(RX-4130C.0028.) The evidence further shows that the transmitter circuit in the SL500 Art accepts a digital input signal including a plurality of digital values from the processor. (*See* RX-5430C at Q/A 398.) For example, [redacted]

In particular, Rambus is of the view that the SL500 Art required the use of "[redacted] (as illustrated below):

(RX-4116.0060.) The ALJ finds that the evidence fails to support this purported distinction. For example, the named inventor Dr. Dally took a contrary view during prosecution in relying on his reduction to practice of a chip that [redacted]. (*See* RX-2014 at ¶¶ 6-7; RX-5430C at Q/A 40-43; *see also* Tr. 1761:16-1764:13 (Poulton); Tr. 1763:14-1764:6 (Dally); RPX-0002C.) In addition, Dr. Hajimiri testified at trial that [redacted] (*See* Tr. 1627:14-1628:01.) Accordingly, the ALJ finds that Rambus is incorrect and the SL 500 prior art does disclose a transmitter.

The Transmitter Circuit Being Operable To Send An Output Signal (With Pre-Emphasis/Pre-Distortion)

Finally, the ALJ finds that clear and convincing evidence shows that the SL500 Art anticipates a transmitter circuit with an equalization mechanism as claimed (*i.e.*, pre-emphasis/pre-distortion circuitry). (RX-5430C at Q/A 399-401.) [redacted]

[redacted] (CIB at 234-237.) [redacted] (CIB at 234.) However the ALJ finds that the evidence instead shows that the equalization circuitry in the SL500 Art was indeed complete and operational with respect to the equalization circuitry therein. (*See* RX-5430C at Q/A 491-496.)

The CWSL500's transmitter circuit was operable [redacted] (*See* RX-4130.0047 [redacted] RX-4116C.0006 ([redacted]; RX-4116C.0007 [redacted] (*See e.g.*, RX-4116C.0060, 62, 72, 80.) Further, the CWSL500 technology's emphasis functionality was operable such that "(i) an output bit signal of the output signal representing a particular bit value has one signal level when the bit value is the same as a bit value represented by a predetermined preceding output bit signal; and (ii) the output bit signal representing the particular bit value has another signal level when the bit value is different from the bit value represented by the predetermined preceding output bit signal." (*See id.*) [redacted]

((RDX-348 (RX-4094C); *see also* RDX-347 [redacted] (RX-5430C at Q/A 388-90.) [redacted]. (RX-5430C at Q/A 382-84.)

(RDX-4076 (excerpt from RDX-350), RX-4092C.)

Dr. Singer asserts that the emphasis [redacted] (CX-10764C at Q/A 363-66.) However, the ALJ finds that the evidence shows that there is no [redacted] (*Id.*) [redacted] (*Id.*) [redacted] (*Id.*)

Rambus also argues that because the CWSL500's emphasis functionality was [redacted] (RX-4130.0047; RIB at 167-72), either the CWSL500's transmitter did not have emphasis or that its emphasis functionality was inoperable. However, the evidence shows that [redacted] (Tr. 1615:10-1616:1.)

In addition, the ALJ finds that as was discussed with respect to infringement, the fact that [redacted] in the SL500FCT product does not constitute the absence of emphasis functionality. (*Compare* Tr. 790:22-791:5.) Under the same rationale as Rambus's

infringement theory, [redacted].

Accordingly, as set forth above, the CWSL500 technology anticipates each and every limitation of asserted claim 1 of the '857 Patent. (*See also,* RX-5430C at Q/A 394-401.)

(b) Independent Claims 24 and 35 of the '857 Patent:

Claims 24 and 35 of the '857 Patent are independent claims that are similar in scope to claim 1 of the '857 Patent except that claims 24 and 35 recite a "component circuit," instead of a "processor," and describe the emphasis functionality in a slightly different manner. Notwithstanding, the ALJ finds that claims 24 and 35 are disclosed by the CWSL500 technology for many of the same reasons cited above in relation to claim 1. (*See, e.g.*, RX-5430C at Q411-419, 428-436.) First, the ALJ finds that [redacted] used in conjunction with the SL500 and Shemp chips were component circuits. (RX-4130.0017, Fig. 1.1, 20-21; RX-4128.0002.) Also, the ALJ finds that as set forth in relation to claim 1, the CWSL500 included the emphasis functionality. The CWSL500 simulations further show that each digital value was represented by one of the signal levels of the output signal.19 (RX-4092C (RDX-350); RDX-347; RX-4094C, hereinafter collectively referred to as "Simulation Waveforms".)

With respect to claim 24, the ALJ finds that the simulations show that the output bit signal from the CWSL500's transmitter had one signal level when a digital bit value of the input signal was the same as a digital bit value represented by a predetermined preceding output bit signal, and one signal level when a digital bit value of the input signal was different from a digital bit value represented by a predetermined preceding output bit signal. (*Id.*; *see also* RX-5430C at Q419.)

[19] If you compare the input bits with the number of signal levels in the output waveform, there is a one-to-one correspondence between the input bits and the output signal levels.

With respect to claim 35, the ALJ finds that the simulations show that transmitter circuit was operable to select each signal level as a function of the digital value represented by that signal level and the digital value represented by the immediately preceding signal level. (Waveform Simulations; *See also* RX-5430C at 436.)

Accordingly, the ALJ finds that the SL 500 art anticipates independent claims 24 and 35.

(c) Independent Claim 39 of the '857 Patent:

Claim 39 of the '857 Patent is an independent claim that is similar in scope to claims 1 and 24 of the '857 Patent except claim 39 describes the transmitter circuit within the chip in a slightly different manner. Notwithstanding, the ALJ finds that claim 39 of the '857 Patent is disclosed by the CWSL500 technology for many of the same reasons cited above in relation to claims 1 and 24 of the '857 Patent. (*See, e.g.*, RX-5430C at Q438-443.) Additionally, the ALJ finds that the CWSL500's transmitter circuit was coupled to the component circuit [redacted], such that the transmitter accepted a digital input signal including a plurality of bit values from the component circuit. (RX-4130C.0018, 20.) The ALJ finds that the CWSL500's transmitter circuit also was operable to send an output signal including a series of signal levels representing the digital values. (RX-4130C.0018.)

Accordingly, as with all of the other asserted independent claims of the '857 Patent, the ALJ finds that the SL 500 art anticipates Claim 39.

(d) Dependent Claims 2, 31, and 49 of the '857 Patent

Turning to the dependent claims, the ALJ finds that clear and convincing evidence shows that the SL500 Art outputs data at a rate of 1.0625 Gbps and thus discloses the additional limitations (as construed by the ALJ) added by way of claims 2, 31, and 49. (*See* RX-5430C at Q/A 402; RX-5430C.0291, Hajimiri Direct at ¶ 11; Tr. 1628:09-13, 1683:18-1684:08; Tr.

2423:19-2427:13.) Indeed, Rambus only appears to contest this aspect of claim 2 under its proposed construction of "output frequency," which has been rejected. (*See* CIB at 239-240.)

(e) Dependent Claims 11-13, 32-34, and 50-52 of the '857 Patent

The ALJ finds that clear and convincing evidence does not show that the SL500 Art anticipates claims 11, 32, and 50. But, the ALJ finds that clear and convincing evidence does show that the additional limitations of these claims would have been obvious in view of the SL500 Art alone or in combination with other art. Specifically, claim 11 requires "at least one additional transmitter circuit within the chip" that is also "coupled to the processor" of claim 1. (*See* JX-120 at 9:26-32.) According to the Respondents, [redacted] The Respondents further argue that multiple cores were included within a version called "Shemp" that LSI purportedly offered to sell in [redacted] However, even if true, the ALJ finds that the Respondents have failed to identify a [redacted] Thus, the ALJ finds that the evidence fails to show anticipation for at least this reason.

Nonetheless, the ALJ finds that clear and convincing evidence shows that it would have been obvious to implement the system disclosed in the SL500 Art in a configuration with multiple transmitter circuits coupled to a processor as claimed. Thus, the additional limitations of claim 11 (and claims 32 and 50) would have been obvious variations to one of ordinary skill in the relevant art.

For example, the evidence shows that the SL 500 art was explicitly designed to be scalable. (RX-4130C.0025 [redacted]

Accordingly, the SL500 could have been designed to implement multiple CWSL500 transmitters, and it would have been obvious to do so. (See RX-5430C at Q/A 408.) The analogous art strongly suggests that a person of ordinary skill would be motivated to include multiple transmitters. For example, as discussed above the Widmer article teaches a system including multiple transmitters that could be used with an upstream processor. (*See* Tr. 1542:05-1543:05.) Moreover, Rambus has not contested this limitation. The ALJ finds that the evidence clearly establishes that it would have been obvious to a person of ordinary skill given the SL 500 art to modify the art to have multiple transmitters couple to a single chip. *Perfect Web Tech., Inc. v. INfoUSA, Inc.*, 587 F.3d 1324, 1331 (Fed. Cir. 2008). As discussed below, the "secondary considerations" that Rambus raises are insufficient to overcome the strong case for modifying the SL 500 art. Accordingly, the ALJ finds that clear and convincing evidence shows that it would have been obvious to implement the system disclosed in the SL 500 art in a configuration with multiple transmitter circuits coupled to a common processor, particularly given the explicit disclosure of that the SL 500 art was designed to be scalable.[20]

(f) Claims 12, 33, and 51 ('857 Patent)

Rambus does not dispute that the SL 500 art discloses the additional limitations of Claims 12, 33, and 51. The only limitation missing is the multiple transmitter limitation of the claims that claims 12, 33, and 51 depend on (namely, claims 11, 32, and 50). For the reasons discussed above with respect to claims 11, 32, and 50, the multiple transmitter limitation would have been obvious to a person of skill in the art. The remaining limitation as shown below:

[20] This analysis also applies as to dependent claims 32 and 50, which similarly call for multiple transmitter circuits coupled to a common component circuit (*e.g.*, a processor).

Dependent Claim Analysis		
Dependent Claim	Additional Claim Limitation	CWSL500 Technology Reference
'857 Claim 12, '857 Claim 33, '857 Claim 51	"the chip has I/O connections and the transmitter circuit is coupled to one or more of the I/O connections to send the output signal through the one or more I/O connections" (certain claims require a plurality)	The SL500 chip had I/O connections, and the CWSL500's transmitter circuit was coupled to one or more of these I/O connections to send the output signal through the one or more I/O connections. (RX-4130C.0021 (Fig 1.3), RX-4130C.0023 (Fig 1.5); RX-4116C.0006-08; RX-5430C at Q/A 404.) Similar to chips with a single transmitter, multiple transmitter chips were, and would have been, coupled to a plurality of I/O connections and operable to send the output signals through the I/O connections. (*Id.*; *see also, e.g.*, RX-5430C at Q409.)

(g) Dependent Claims 13, 34, and 52 ('857 Patent)

Rambus does not dispute that the SL 500 art discloses the additional limitations of Claims 13, 34, and 52. The only limitation missing is the multiple transmitter limitation of the claims that claims 13, 34, and 52 depend on (namely, claims 11, 32, and 50). For the reasons discussed above with respect to claims 11, 32, and 50, the multiple transmitter limitation would have been obvious to a person of skill in the art. The remaining limitation as shown below:

Dependent Claim Analysis		
Dependent Claim	Additional Claim Limitation	CWSL500 Technology Anticipation Reference
'857 Claim 13, '857 Claim 34, '857 Claim 52	"operable to provide output signals representing a parallel stream of data from the processor"	Similar to implementation of a single transmitter, a chip with multiple CWSL500 transmitter circuits was operable to provide output signals representing a parallel stream of data from the processor. (RX-4130C.0020-21 [redacted]; RX-5430C at Q/A 410.) As discussed in relation to claim 1 of the '857 Patent, the CWSL500's transmitter accepts this parallel data and sends a corresponding output signal. (RX-4130C.0018 [redacted].)

(h) Additional Dependent Claims of The '857 Patent

Finally, clear and convincing evidence shows that the LSI art discloses the limitations added by way of the remaining dependent claims. In fact, Rambus does not appear to raise any validity arguments specific to the limitations added by way of these claims. Accordingly, as detailed in the chart below, the ALJ finds those claims invalid as well.

Dependent Claim Anticipation Analysis		
Dependent Claim	Additional Claim Limitation	CWSL500 Technology Anticipation Reference
'857 Claim 4, '857 Claim 26	"operable to emphasize signal levels representing values following transitions between values relative to signal levels representing repeated values"	The CWSL500 simulations show that when two consecutive digital input bits are the same, the output signal from the CWSL500 transmitter has one level. (Simulation Waveforms.) When two consecutive digital input bits are different, the output signal from the CWSL500 transmitter has another level. (RX-5430C at Q/A 403,)
'857 Claim 5, '857 Claim 27, '857 Claim 43	"the chip has I/O connections and the transmitter circuit is coupled to one or more of the I/O connections to send the output signal through the one or more I/O connections" (certain claims require a plurality)	The SL500 chip had I/O connections, and the CWSL500's transmitter circuit was coupled to one or more of these I/O connections to send the output signal through the one or more I/O connections. (RX-4130C.0021 (Fig 1.3), RX-4130C.0023 (Fig 1.5); RX-4116C.0006-08; RX-5430C at Q/A 404.) Similar to chips with a single transmitter, multiple transmitter chips were, and would have been, coupled to a plurality of I/O connections and operable to send the output signals through the I/O connections. (RX-5430C at Q/A 404; RX-5430C at Q409.)

Dependent Claim Anticipation Analysis		
Dependent Claim	Additional Claim Limitation	CWSL500 Technology Anticipation Reference
'857 Claim 6, '857 Claim 28, '857 Claim 44	"operable to send the output signal in nonmodulated form"	If the CWSL500 were to send modulated signals, a modulator block would have been included in RX-4116C at Fig. 2 (RX-4116C.0006). The CWSL500's transmitter block diagram does not include a modulator block, nor does it receive a carrier wave, which would be necessary for modulation of the output signal. (RX-5430C at Q/A 405.) Therefore, the signal is sent in nonmodulated form. (RX-5430C at Q/A 405.)
'857 Claim 9, '857 Claim 47	"(each digital value/each bit value in the digital input signal) is represented by one of the signal levels in the output signal"	The CWSL500 simulation waveforms wherein each digital value is represented by one of the signal levels of the output signal. RX-4092C (RDX-350); RDX-347; RX-4094C (hereinafter collectively referred to as "Simulation Waveforms"); RX-5430C at Q/A 406.)
'857 Claim 10	"the digital input signal includes a plurality of bits and each bit of the digital input signal is represented by one of the signal levels in the output signal"	The CWSL500's transmitter accepted a digital input signal, which included a plurality of bits. (RX-4130C.0018, Fig. 1.2.) The CWSL500 simulation waveforms show that each bit of the digital input bit is represented by one of the signal levels in the output signal. (Simulation

Dependent Claim Anticipation Analysis		
Dependent Claim	Additional Claim Limitation	CWSL500 Technology Anticipation Reference
		Waveforms.; RX-5430C at Q/A 407.)
'857 Claim 25, '857 Claim 36, '857 Claim 40	"wherein the component circuit is a processor"	As discussed in relation to claim 1 of the '857 Patent, the CWSL500 technology discloses a component circuit, *i.e.*, an [redacted] that was a processor. (*See also, e.g.*, RX-5430C at Q/A 420.)
'857 Claim 41	"operable to select each signal level as a function of the bit value represented by that signal level and of the bit values represented by one or more preceding signal levels"	The CWSL500 simulations show that when two consecutive digital input bits are the same, the output signal from the CWSL500 transmitter has one level, and when two consecutive digital input bits are different, the output signal from the CWSL500 transmitter has another level. (Simulation Waveforms; *see also, e.g.*, RX-5430C at Q/A 445.)
'857 Claim 42	"operable to select each signal level as a function of the bit value represented by that signal level and the bit value represented by the immediately preceding signal level"	The CWSL500 simulations show that when two consecutive digital input bits are the same, the output signal from the CWSL500 transmitter has one level, and when two consecutive digital input bits are different, the output signal from the CWSL500 transmitter has another level. (Simulation Waveforms; *see also, e.g.*, RX-

Dependent Claim Anticipation Analysis		
Dependent Claim	Additional Claim Limitation	CWSL500 Technology Anticipation Reference
'857 Claim 53	"operable to select each signal level as a function of only the bit value represented by that signal level and the bit value represented by the immediately preceding signal level"	5430C at Q/A 446.)

(3) *Invalidity Of U.S. Patent No. 7,715,494 Over The SL500 Art*

The ALJ finds that clear and convincing evidence shows that the SL500 art anticipates claims 1, 2, 3, 6, 8, 25, 30, 39, and 42 of the '494 patent and renders obvious claims 26 and 40 for similar reasons to those discussed above with respect to the '857 patent. Indeed, Rambus does not appear to raise any validity arguments specific to the '494 patent claims. (*See* CPB at 404-406.)

(a) Independent Claim 1 of the '494 Patent:

Claim 1 of the '494 Patent is an independent claim that is disclosed by the CWSL500 technology. (*See* RX-5430C at Q/A 455-462.) As discussed in relation to claim 1 of the '857 Patent, the CWSL500 technology discloses "a circuit comprising a semiconductor chip" and "a transmitter circuit within the chip." The ALJ finds that the CWSL500 technology also discloses a "transmitter circuit being operable to accept a digital input signal including a plurality of bits." In particular, the CWSL500's transmitter circuit is coupled to a component circuit [redacted], such that the transmitter accepts a digital input signal including a plurality of bits. (RX-4130C.0018, 20.)

The CWSL500 technology also discloses a transmitter circuit that is operable to "send an output signal including a series of output bit signals." (*See* RX-4130C.0018.) The CWSL500 simulation waveforms further show "each bit of the digital input signal being represented by a single output bit signal." (*See* Simulation Waveforms.) The simulation waveforms also show that the CWSL500's transmitter circuit generated a sign which depended upon the value of the bit represented by such output bit signal and generating a magnitude which is a function of the value of the bit represented by such output bit signal and the values of the bits represented by one or more preceding output bit signals, each output bit signal having sign and magnitude determined by the generated sign and generated magnitude. (Simulation Waveforms.)

(b) Independent Claims 25 and 39 of the '494 Patent:

Claim 25 of the '494 Patent is an independent claim that is similar in scope to claim 1 of the '494 Patent except that claim 25 requires the transmitter's output signal to be a differential signal and also describes the emphasis functionality in a slightly different manner. Notwithstanding, the ALJ finds that claim 25 of the '494 Patent is disclosed by the CWSL500 technology for many of the same reasons cited above in relation to claim 1 of the '494 Patent. (*See* RX-5430C at Q/A 467-474, 477-483.) Additionally, the CWSL500 technology discloses a transmitter circuit with a differential output signal. (RX-4130C.0018 [redacted] The ALJ finds that CWSL500 simulation waveforms also show that the CWSL500's transmitter circuit drives the series of output bit signals to have sign an represented by logic level of a first bit that is to be transmitted, and magnitude represented by whether the first bit represents a common logic level relative to an immediately previous bit, the magnitude being driven to be relatively smaller when the first bit

has a common logic level with the immediately previous bit, and to be relatively larger when the first bit does not have the common logic level. (Simulation Waveforms; RX-5430C at Q/A 474.)

Claim 39 of the '494 Patent is a method claim that is otherwise equivalent to claim 25 of the '494 Patent. Accordingly, the CWSL500 technology discloses the limitations of claim 39 of the '494 Patent for at least the same reasons cited above in relation to claim 25 of the '494 Patent. (*See* RX-5430C at Q/A 477-483.)

As is shown above, the implementation of the CWSL500 technology in semiconductor chips anticipated each and every limitation of the Asserted Claims of the Dally Patents. (*See also* RX-5430C.0213-294.) Rambus has not provided any credible evidence to the contrary.

(c) Dependent Claims 26 and 40 of The '494 Patent

The ALJ finds that clear and convincing evidence does show that the SL500 Art anticipates claims 26 and 40. In addition, the ALJ finds that clear and convincing evidence also shows that the additional limitations of these claims would have been obvious in view of the SL500 Art alone or in combination with other art. Specifically, claims 26 and 40 requires that the chip "include[] plural of said transmitter circuits." Unlike claims 11, 32, and 50, there is no requirement that the multiple transmitter circuits be also "coupled to the processor" (as discussed *supra* at 152-154). Thus, the ALJ finds that respondents are correct that the evidence shows that the core of the SL500 was designed to be scalable and thus "can include at least one additional transmitter circuit within the chip." (*See* RX-5430C at Q/A 408.) The Respondents further argue that multiple cores were included within a version called "Shemp" that LSI purportedly offered to sell in [redacted] Thus, the ALJ finds that the evidence show anticipation for at least this reason.

Moreover, the ALJ finds that even if this disclosure is lacking clear and convincing evidence shows that it would have been obvious to implement the system disclosed in the SL500 Art in a configuration with multiple transmitter circuits as claimed. Thus, the additional limitations of claim 26 and 40 would have been obvious variations to one of ordinary skill in the relevant art.

For example, the evidence shows that the SL 500 art was explicitly designed to be scalable. (RX-4130C.0025 [redacted] Accordingly, the SL500 could have been designed to implement multiple CWSL500 transmitters, and it would have been obvious to do so. (See RX-5430C at Q/A 408.) The analogous art strongly suggests that a person of ordinary skill would be motivated to include multiple transmitters. For example, as discussed above the Widmer article teaches a system including multiple transmitters. (*See* Tr. 1542:05-1543:05.) Moreover, Rambus has not contested this limitation. The ALJ finds that the evidence clearly establishes that it would have been obvious to a person of ordinary skill given the SL 500 art to modify the art to have multiple transmitters couple to a single chip. *Perfect Web Tech., Inc. v. INfoUSA, Inc.*, 587 F.3d 1324, 1331 (Fed. Cir. 2008). As discussed below, the "secondary considerations" that Rambus raises are insufficient to overcome the strong case for modifying the SL 500 art. Accordingly, the ALJ finds that clear and convincing evidence shows that it would have been obvious to implement the system disclosed in the SL 500 art in a configuration with multiple transmitter circuits, particularly given the explicit disclosure of that the SL 500 art was designed to be scalable.

(d) Other Dependent Claims

Rambus does not raise any other arguments with respect to the other dependent claims. Accordingly, the ALJ finds that Respondents have shown by clear and convincing evidence that

they are anticipated. The evidence with respect to each of the remaining independent claims is listed in the chart below:

Dependent Claim Anticipation Analysis		
Dependent Claim	Additional Claim Limitation	CWSL500 Technology Anticipation Reference
'494 Claim 3 '494 Claim 30, '494 Claim 42	"operable to (send/provide) the output signal with an output frequency of at least 1 GHz and a bandwidth greater than 100 MHz" "the series of output signals is transmitted by the transmitter onto a signal path at a rate of at least 400 megahertz"	Under Respondents' construction of the term "output frequency", the CWSL500 technology satisfies this limitation.21 (RX-4130.0021 [redacted] RX-4130.0024 [redacted]; RX-5430C at Q/A 402.)
'494 Claim 2	"the function is such that an output bit signal is representing a bit having a value different from the value of the bits represented in the one or more preceding output bit signals has a greater magnitude than an output bit signal representing a bit having the same value as the bits represented by the one or more preceding output bit signals"	The CWSL500 simulations show that the CWSL500's transmitter performed the emphasis function such that an output bit signal representing a bit having a value different from the value of the bits represented in the one or more preceding output bit signals had a greater magnitude than an output bit signal representing a bit having the same value as the bits represented by the one or more preceding output bit signals. (Simulation Waveforms; RX-5430C at Q/A 463.)

[21] Rambus' dispute with respect to this limitation is not what is disclosed by the CWSL500 technology; rather, Rambus' dispute is with the meaning of the term "output frequency."

Dependent Claim Anticipation Analysis		
Dependent Claim	Additional Claim Limitation	CWSL500 Technology Anticipation Reference
'494 Claim 6	"operable to select the magnitude of each output bit signal based only on the value of the bit represented by that output bit signal and the value of the bit represented by the immediately preceding output bit signal"	The CWSL500 simulations show that the CWSL500's transmitter circuit was operable to select the magnitude of each output bit signal based only on the value of the bit represented by that output bit signal and the value of the bit represented by the immediately preceding output bit signal. (Simulation Waveforms; RX-5430C at Q/A 465.)
'494 Claim 8	"wherein the function is reprogrammable"	The CWSL500's transmitter was operable such that the relationship between the strength of the output bit signals and the number of bits since the last transition (0 or 1) is reprogrammable. (RX-4116C.0004 [redacted] RX-4116C.0010 (Fig. 4); RX-4116C.0060, 62, 72 and 80; RX-5430C at Q/A 66.)

C. Obviousness

Included within the presumption of validity is a presumption of non-obviousness. *Structural Rubber Prods. Co. v. Park Rubber Co.*, 749 F.2d 707, 714 (Fed. Cir. 1984). Obviousness is grounded in 35 U.S.C. § 103, which provide, *inter alia*, that:

> A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negative by the manner in which the invention was made.

35 U.S.C. § 103(a). Under 35 U.S.C. § 103(a), a patent is valid unless "the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains." 35 U.S.C. § 103(a). The ultimate question of obviousness is a question of law, but "it is well understood that there are factual issues underlying the ultimate obviousness decision." *Richardson-Vicks Inc.*, 122 F.3d at 1479; *Wang Lab., Inc. v. Toshiba Corp.*, 993 F.2d 858, 863 (Fed. Cir. 1993).

Once claims have been properly construed, "[t]he second step in an obviousness inquiry is to determine whether the claimed invention would have been obvious as a legal matter, based on underlying factual inquiries including: (1) the scope and content of the prior art, (2) the level of ordinary skill in the art, (3) the differences between the claimed invention and the prior art; and (4) secondary considerations of non-obviousness" (also known as "objective evidence"). *Smiths Indus. Med. Sys., Inc. v. Vital Signs, Inc.*, 183 F.3d 1347, 1354 (Fed. Cir. 1999), citing *Graham v. John Deere Co.*, 383 U.S. 1, 17 (1966). The ultimate determination of whether an invention would have been obvious is a legal conclusion based on underlying findings of fact. *In re Dembiczak*, 175 F.3d 994, 998 (Fed. Cir. 1999).

Obviousness may be based on any of the alleged prior art references or a combination of the same, and what a person of ordinary skill in the art would understand based on his knowledge and said references. If all of the elements of an invention are found, then:

> a proper analysis under § 103 requires, inter alia, consideration of two factors: (1) whether the prior art would have suggested to those of ordinary skill in the art that they should make the claimed composition or device, or carry out the claimed process; and (2) whether the prior art would also have revealed that in so making or carrying out, those of ordinary skill would have a reasonable expectation of success. *Both the suggestion and the reasonable expectation of success must be founded in the prior art, not in the applicant's disclosure.*

Velander v. Garner, 348 F.3d 1359, 1363 (Fed. Cir. 2003) (emphasis added) (internal citations omitted).

The critical inquiry in determining the differences between the claimed invention and the prior art is whether there is a reason to combine the prior art references. *See C.R. Bard v. M3 Sys.*, 157 F.3d 1340, 1352 (Fed. Cir. 1998). For example:

> *[A] patent composed of several elements is not proved obvious merely by demonstrating that each of its elements was, independently, known in the prior art.* Although common sense directs one to look with care at a patent application that claims as innovation the combination of two known devices according to their established functions, *it can be important to identify a reason that would have prompted a person of ordinary skill in the relevant field to combine the elements in the way the claimed new invention does. This is so because inventions in most, if not all, instances rely upon building blocks long since uncovered*, and claimed discoveries almost of necessity will be combinations of what, in some sense, is already known.

KSR Int'l Co. v. Teleflex, Inc., 550 U.S. 398, 418-19 (2007) (emphasis added). The Federal Circuit case law previously required that, in order to prove obviousness, the patent challenger must demonstrate, by clear and convincing evidence, that there is a "teaching, suggestion, or motivation to combine. The Supreme Court has rejected this "rigid approach" employed by the Federal Circuit in *KSR Int'l Co. v. Teleflex Inc.*, 500 U.S. 398 (2007), 127 S.Ct. 1727, 1739. The Supreme Court stated:

> When a work is available in one field of endeavor, design incentives and other market forces can prompt variations of it, either in the same field or a different one. If a person of ordinary skill can implement a predictable variation, § 103 likely bars its patentability. For the same reason, if a technique has been used to improve one device, and a person of ordinary skill in the art would recognize that it would improve similar devices in the same way, using the technique is obvious unless its actual application is beyond his or her skill. Sakraida and Anderson's-Black Rock are illustrative–a court must ask whether the improvement is more than the predictable use of prior art elements according to their established function.

> Following these principles may be more difficult in other cases than it is here because the claimed subject matter may involve more than the simple substitution of one known element for another or the mere application of a known technique to a piece of prior art ready for the improvement. Often, it will be necessary for a court to look to interrelated teachings of multiple patents; the effects of demands known to the design community or present in the marketplace; and the background knowledge possessed by a person having ordinary skill in the art, all in order to determine whether there was an apparent reason to combine the known elements in the fashion claimed by the patent at issue. To facilitate review, this analysis should be made explicitly. See *In re Kahn*, 441 F.3d 977, 988 (CA Fed. 2006) ("[R]ejections on obviousness grounds cannot be sustained by mere conclusory statements; instead, there must be some articulated reasoning with some rational underpinning to support the legal conclusions of obviousness"). As our precedents make clear, however, the analysis need not seek out precise teachings directed to the specific subject matter of the challenged claim, for a court can take account of the inferences and creative steps that a person of ordinary skill in the art would employ.
>
> [. . .]
>
> The obviousness analysis cannot be confined by a formalistic conception of the words teaching, suggestion, and motivation, or by overemphasis on the importance of published articles and the explicit content of issued patents. The diversity of inventive pursuits and of modern technology counsels against limiting the analysis in this way. In many fields it may be that there is little discussion of obvious techniques or combinations, and it often may be the case that market demand, rather than scientific literature, will drive design trends. Granting patent protection to advance that would occur in the ordinary course without real innovation retards progress and may, in the case of patents combining previously known elements, deprive prior inventions of their value or utility.

KSR, 550 U.S. at 417-419; 127 S.Ct. at 1740-41. The Federal Circuit has harmonized the KSR opinion with many prior circuit court opinions by holding that when a patent challenger contends that a patent is invalid for obviousness based on a combination of prior art references, "the burden falls on the patent challenger to show by clear and convincing evidence that a person of ordinary skill in the art would have had reason to attempt to make the composition or device, or carry out the claimed process, and would have had a reasonable expectation of success in doing so. *PharmaStem Therapeutics, Inc. v. ViaCell, Inc.*, 491 F.3d 1342, 1360 (Fed. Cir. 2007)(citing *Medichem S.A. v. Rolabo S.L.*, 437 F.3d 1175, 1164 (Fed. Cir. 2006)); *Noelle v. Lederman*, 355

F.3d 1343, 1351-52 (Fed. Cir. 2004); *Brown & Williamson Tobacco Corp. v. Philip Morris, Inc.*, 229 F.3d 1120, 1121 (Fed .Cir. 2000) and *KSR*, 127 S.Ct. at 1740 ("a combination of elements 'must do more than yield a predictable result'; combining elements that work together 'in an unexpected and fruitful manner' would not have been obvious"). Further, a suggestion to combine need not be express and may come from the prior art, as filtered through the knowledge of one skilled in the art. *See Certain Lens-Fitted Film Pkgs.*, Inv. No. 337-TA-406, Order No. 141 at 6 (May 24, 2005).

"Secondary considerations," also referred to as "objective evidence of non-obviousness," must be considered in evaluating the obviousness of a claimed invention, but the existence of such evidence does not control the obviousness determination. *Graham*, 383 U.S. at 17-18. A court must consider all of the evidence under the *Graham* factors before reaching a decision on obviousness. *Richardson-Vicks Inc.*, 122 F.3d at 1483-84. Objective evidence of non-obviousness may include evidence of the commercial success of the invention, long felt but unsolved needs, failure of others, copying by others, teaching away, and professional acclaim. *See Perkin-Elmer Corp. v. Computervision Corp.*, 732 F.2d 888, 894 (Fed. Cir. 1984), *cert. denied*, 469 U.S. 857 (1984); *Avia Group Int'l, Inc. v. L.A. Gear California*, 853 F.2d 1557, 1564 (Fed. Cir. 1988); *In re Hedges*, 783 F.2d 1038, 1041 (Fed. Cir. 1986); *Kloster Speedsteel AB v. Crucible Inc.*, 793 F.2d 1565 (Fed. Cir. 1986), *cert. denied*, 479 U.S. 1034 (1987). The burden of showing secondary considerations is on the patentee and, in order to accord objective evidence substantial weight, a patentee must establish a nexus between the evidence and the merits of the claimed invention; a *prima facie* case is generally set forth "when the patentee shows both that there is commercial success, and that the thing (product or method) that is commercially successful is the invention disclosed and claimed in the patent." *In re GPAC Inc.*,

57 F.3d 1573, 1580 (Fed. Cir. 1995); *Demaco Corp. v. F. Von Langsdorff Licensing Ltd.*, 851 F.2d 1387, 1392 (Fed. Cir. 1988), cert. denied, 488 U.S. 956 (1988); *Certain Crystalline Cefadroxil Monohydrate*, Inv. No. 337-TA-293, Comm'n Op. (March 15, 1990). Once a patentee establishes nexus, the burden shifts back to the challenger to show that, *e.g.*, commercial success was caused by "extraneous factors other than the patented invention, such as advertising, superior workmanship, etc." *(Id.)* at 1393.

Generally, a prior art reference that teaches away from the claimed invention does not create *prima facie* case of obviousness. *In re Gurley*, 27 551, 553 (Fed. Cir. 1994); *see also Andersen Corp. v. Pella Corp.*, No. 2007-1536, 2008 U.S. App. LEXIS 24087, *13-18 (Fed. Cir. Nov. 19, 2008); *Certain Rubber Antidegradants*, Inv. No. 337-TA-533 (Remand), Final ID (Dec. 3, 2008) (stating, "*KSR* reaffirms that obviousness is negated when the prior art teaches away from the invention.")). However, the nature of the teaching is highly relevant. *Id.* "A reference may be said to *teach away when* a person of ordinary skill, upon reading the reference, would be *discouraged from following the path set out in the reference, or would be led in a direction divergent from the path that was taken by the applicant.*" *Id.* (emphasis added). For example, "a reference will teach away if it suggests that the line of development flowing from the reference's disclosure is unlikely to be productive of the result sought by the applicant." *Id.*

The Barth Patents

Respondents argue that the Barth Patents are invalid in light of the following twelve (12) prior art combination:

Asserted Claims Rendered Obvious by Prior Art			
Prior Art Combination (1-12)	'353 Patent	'405 Patent	'109 Patent
1. Yano / Farmwald '037	11, 12, 13	11, 12, 13, 15, 18	1, 2, 4, 5, 12, 13, 20, 21, 24
2. Yano / SCI and Release 4	11, 12, 13	11, 12, 13, 15, 18	1, 2, 4, 5, 12, 13, 20, 21, 24
3. Dan / Farmwald '037	11, 12, 13	11, 12, 13, 15, 18	1, 2, 4, 5, 12, 13, 20, 21, 24

4. Dan / SCI and Release 4	11, 12, 13	11, 12, 13, 15, 18	1, 2, 4, 5, 12, 13, 20, 21, 24
5. Farmwald '037 / Yano	11, 12, 13	11, 12, 13, 15, 18	1, 2, 4, 5, 12, 13, 20, 21, 24
6. Farmwald '037 / Dan	11, 12, 13	11, 12, 13, 15, 18	1, 2, 4, 5, 12, 13, 20, 21, 24
7. NeXTBus / Farmwald '037	----	11, 12, 13, 15, 18	1, 2, 4, 5, 12, 13, 20, 21, 24
8. NeXTBus / Release 4	----	11, 12, 13, 15, 18	1, 2, 4, 5, 12, 13, 20, 21, 24
9. Harriman / Farmwald '037	----	11, 12, 13, 15, 18	1, 2, 4, 5, 12, 13, 20, 21, 24
10. Harriman / Release 4	----	11, 12, 13, 15, 18	1, 2, 4, 5, 12, 13, 20, 21, 24
11. Farmwald '037 / NeXTBus	----	11, 12, 13, 15, 18	1, 2, 4, 5, 12, 13, 20, 21, 24
12. Farmwald '037 / Harriman	----	11, 12, 13, 15, 18	1, 2, 4, 5, 12, 13, 20, 21, 24

(RIB at 78.) Respondents perform an analysis of the various different groups of combinations, explaining why one of ordinary skill in the art would have been motivated to combine the references and which elements from each reference would be combined that would render the missing elements obvious. (RIB at 78-96.) The Respondents' obviousness arguments appear to be largely directed at four limitations that may not be disclosed in Yano, Dan, NeXTBus and/or Harriman and involve features well known in the prior art, including: (1) double data rate functionality (claims 12 and 13 of the '353 and '405 patents); (2) autoprecharge functionality (claim 11 of the '405 patent, claims 2, 5, and 13 of the '109 patent); (3) multiple memory banks (claims 4, 5, 12, and 13 of the '109 patent); and (4) sense amplifiers (claim 18 of the '405 patent, claims 2 and 21 of the '109 patent). The evidence shows that the identified features were well known in the prior art and would have been obvious additions to the references discussed in the prior section on anticipation. Staff agrees. (SIB at 76-81.)

a) Combining Asynchronous/Synchronous Memory Systems

Before addressing the specific elements set forth *supra*, the ALJ finds it necessary to address Rambus's argument that certain prior art references cannot disclose each and every element of the asserted claims because they are asynchronous and that certain combinations should be rejected as improper because they combine features from asynchronous systems with features from synchronous systems. (CRB at 28-29; 44.) The evidence shows that the proposed

asynchronous/synchronous combinations would have been obvious to a person of ordinary skill in the art. As the Board of Patent Appeals recently explained during the '405 Reexamination:

> Respondent [Rambus] and the Examiner also do not rebut Mr. Paris's testimony describing how known asynchronous functions were being combined routinely with, and integrated into, synchronous DRAM systems by skilled artisans.

(SX-0008, September 1, 2011 Board Decision at 12; *see also id.* at 15 (finding asserted claims 11, 15, and 18 of the '405 patent invalid as obvious in view of the prior art); Przybylski, Tr. 2704:15-2710:01, 2711:03-2712:10, 2713:17-2714:08 (disagreeing with the Board's decision as to whether it would have been obvious to combine aspects of asynchronous and synchronous art).) The evidence shows that it would indeed have been obvious to combine aspects of asynchronous and synchronous art so as to achieve the inventions claimed in the Barth I patents. (RX-5429C, Jacobs Direct Q&A 105, 129, 492-496.)

b) Yano or Dan in combination with Farmwald or SCI and Release 4

As set forth *supra* in Section VI.B.1, the ALJ found that that Yano and Dan each render claim 11 of the '353 Patent invalid as anticipated under § 102. Furthermore, certain elements of claim 11 of the '353 Patent are similar to certain elements in the asserted claims of the '405 and '109 Patents, *e.g.*, "strobe signal"/"signal". Thus, to the extent that the elements of claim 11 of the '353 Patent are disclosed in Yano and Dan, the analysis for those elements applies equally to like elements found in the asserted claims of the '405 and '109 Patents.

To the extent that Yano and/or Dan fail to disclose certain elements of the asserted claims of the Barth Patents, the ALJ finds it would have been obvious to one of ordinary skill in the art to combine that element from another prior art references with Yano or Dan. (*Id.* at Q466.) Specifically, it would have been obvious to one of ordinary skill in the art to combine Yano or Dan with the teachings of either (1) Farmwald '037 or (2) SCI with Release 4. (RX-5429C at

Q467, 476.)

(1) *Double Data Rate ("DDR") Claim Elements*

The double data rate, or "DDR," elements of the asserted Barth claims may not be disclosed in Yano or Dan, but can be found in the disclosure of the Farmwald '037 and in the disclosure of SCI. (RX-5429C at Q468-469.) As set forth *supra* in Section VI.B.1.e, Farmwald '037 discloses the DDR elements. (*See* RX-4269 at 8:42-48; 27:58-63 (Claim 33).) Similarly, Figure 6 of SCI similarly illustrates first and second portions of data being sampled during a single clock cycle. (*See* RX-4278C.0004, Figure 6.)

The evidence shows that it would have been obvious to one of ordinary skill in the art as of the priority date of the Barth Patents to combine the DDR disclosure from Farmwald '037 or SCI with the write operations disclosed in Yano and Dan, respectively in order to improve the efficiency and speed of data access operations. (*See* RX-5357 at 28.) Yano, Dan, Farmwald '037, and SCI each sought to address the well-known need in the industry for faster data access operations, and creating faster data speeds without increasing the number of input/output pins by sampling two pieces of data during a single cycle of a clock or other periodic signal would be a desirable result. (RX-5429C at Q470.)

The evidence further shows that DDR was a well-known method in the art and that this method performs the same established function in the asserted Barth claims, namely capturing two pieces of data from the bus during a single period of a clock or other periodic timing signal. (RX-5429C at Q469-470.) Indeed, double data rate techniques were widely available and known in the art as an effective way to increase speed without significantly increasing circuit complexity, pincount, *etc.* (RX-5429C, Jacobs Direct Q&A 202-207.) As such, combining the DDR elements from either Farmwald '037 or from SCI with the known write operation method

described in both Yano and Dan does no more than yield predictable results, and, therefore, such combinations would have been obvious to one of ordinary skill in the art. *See KSR Int'l Co. v. Teleflex Inc.*, 550 U.S. 398, 417 (2007).

(2) *Precharge Claim Elements*

The precharge elements of the asserted Barth claims also may not be disclosed in Yano or Dan, but are found in both Farmwald '037 and Release 4, which disclose the precharge elements of the asserted Barth claims. (RX-5429C at Q 471-472.) As set forth *supra* in Section VI.B.1.e, Farmwald '037 the precharge elements in a number of locations. (*See* RX-4269 at 10:62-11:2; 11:60; 28:5-20.) Similarly, Table 3.11.5-1 of JEDEC Release 4—the SDRAM Function Truth Table—identifies "WRITE with AUTO Precharge" as a command option. (*See* RX-2108C.0111 at Table 3.11.5-1.)[22] The evidence shows that it would have been obvious to a person of ordinary skill in the art to implement precharge functionality in systems that lacked such functionality, particularly as synchronous systems (and the associated autoprecharge capabilities used therewith) began overtaking asynchronous systems prior to the October 1995 filing date of the Barth I patents. (RX-5429C, Jacobs Direct Q&A 208-212.)

The evidence shows that it would have been obvious to one of ordinary skill in the art as of the priority date of the Barth Patents to combine the precharge command from either Farmwald '037 or from JEDEC Release 4 with the write operations disclosed in Yano and Dan, respectively, to improve the efficiency and speed of data access operations. (RX-5429C at Q473.) The evidence shows that Yano, Dan, Farmwald '037, and Release 4 each sought to address the well-known need in the industry for faster data access operations. (*See* RX-5357 at

[22] The system for automatic precharge found in Release 4 is the same as the auto precharge system found in the subsequent JEDEC DDR SDRAM specification Rambus alleges is covered by the asserted Barth claims. (*See* RX-3905.0017.)

28.) This is facilitated by conducting a precharge operation following the write operation when there potentially is no active operation on the bus instead of incurring a time penalty by waiting until the next memory operation to precharge the sense amplifiers. (RX-5429C at Q473.)

Thus, the evidence shows that providing a command to a memory device to initiate a precharge operation was a well-known method in the art and, further, that this command performs the same established function in the asserted Barth claims (*i.e.*, charging amplifiers to an indeterminate intermediate value that is neither logical 0 or 1). (RX-5429C at Q473.) As such, combining the precharge elements from either Farmwald '037 or JEDEC Release 4 with the known write operation method described in each of Yano and Dan does no more than yield predictable results, and therefore such combinations would have been obvious to one of ordinary skill in the art. (RX-5429C at Q473.) *See KSR*, 550 U.S. at 417.

(3) *Multiple Memory Bank Claim Elements*

The multiple memory banks elements are not disclosed in Yano but are disclosed in Dan where it discloses using a plurality of memory banks in Figure 4. (RX-4262 at 7:42-54; RX-5429C at Q476.) The memory bank elements are disclosed in the Farmwald '037 and in the JEDEC Release 4 reference. (RX-5429C at Q475.) As set forth *supra* in Section VI.B.1.e, Farmwald '037 plainly discloses each of the memory bank elements. (RX-4269 at 11:15-18; 23:54-56; 24:26; Fig. 15.) JEDEC Release 4 also discloses the memory bank elements of the asserted claims. (RX-2108C.0018 at 2.2, Section 2.1.6 ("In a RAM that has multiple banks in its architecture, [where] the BANK ADDRESS is used, at any instant of time, [to] select any one of the available banks."); RX-2108C.0111, 5-5, Table 3.11.5-1.)

The evidence shows that it would have been obvious to one of ordinary skill in the art at the time of the Barth Patents to combine memory bank elements from Farmwald '037 or JEDEC

Release 4 with the methods disclosed in Yano and Dan, respectively, to improve the speed of data access operations by allowing multiple banks to cycle in an interleaved fashion. Yano, Dan, Farmwald '037, and JEDEC Release 4 all sought to address the well-known need in the industry for faster data access operations. (RX-5357 at 28.) The evidence shows that it would have been obvious to a person of ordinary skill in the art to implement multiple memory banks in systems that lacked such functionality, particularly in light of the growing need for larger memory capacities and increased access speeds prior to the October 1995 filing date of the Barth I patents. (RX-5429C, Jacobs Direct Q&A 474-476, 512-514.)

Thus, Farmwald '037 and JEDEC Release 4 show that providing bank selection information to a memory device containing a plurality of memory banks was a well-known method in the prior art to the Barth Patents and performs the same established function in the '109 Patent. (RX-5429C at Q476.) As a result, combining the memory bank elements disclosed in Farmwald '037 and in JEDEC Release 4 with the disclosures of Yano and Dan does no more than yield the predictable result of increased data access rates due to interleaved cycling between banks, and therefore such combinations would have been obvious to one of ordinary skill in the art. (RX-5429C at Q476.)

(4) *Sense Amplifier Claim Elements*

While Yano and Dan do not explicitly disclose sense amplifier elements, the evidence shows that providing a control code to a memory device specifying that a row of sense amplifiers be activated, or that a sense operation occur, in the memory device would be inherent in the write operations disclosed in Yano and Dan. (RX-5429C at Q478; *see also* RX-4261.0008 at Figure 2.) This is particularly true as synchronous systems (and the associated sense amplifiers used

therewith) began overtaking asynchronous systems prior to the October 1995 filing date of the Barth I patents. (RX-5429C, Jacobs Direct Q&A 477-478, 515-518.)

Moreover, it would have been obvious for one of ordinary skill in the art as of the alleged October 19, 1995 priority date to apply the write operation methods described in Yano and Dan, respectively, to a variety of memory types including DRAM, in which case the resulting method would necessarily include a code that specifies that a row of sense amplifiers be activated, or that a sense operation occur, in the memory device. (RX-5429C at Q478.)

c) Farmwald in combination with Yano or Dan

As set forth *supra* in Section VI.B.1.e, the ALJ found that Farmwald '037 failed to disclose the claimed "strobe signal" element of the Barth Patents. Rambus only disputed whether Farmwald '037 disclosed the "strobe signal"/ "signal" limitation and does not dispute that Farmwald '037 discloses the other features of the Barth Patents. (CRB at 24-25.) The evidence shows that Farmwald '037 discloses the other limitations of the Barth Patents. (RX-4269; RX-5429C at Q&A 366-384.) Furthermore, certain elements of the asserted claims of the '109 Patent are similar to certain elements in the asserted claims of the '405 and '353 Patents. Thus, to the extent that the elements of the asserted claims of the '109 Patent are disclosed in Farmwald '037, the analysis for those elements applies equally to like elements found in the asserted claims of the '405 and '353 Patents.

The evidence shows that it would have been obvious to one of ordinary skill in the art to combine the element(s) from Yano or Dan with the disclosure of the Farmwald '037, discloses the other missing elements of the Barth Patents from the Yano or Dan disclosures.

As set forth in Section VI.B.1, both Yano and Dan each disclose the "strobe signal" elements of the asserted claims of the '353 and '405 patents. Specifically, Yano discloses that

when "the data strobe signal (DS) creates the active state, the write data is transmitted by the databus (DBx) corresponding to this bit and the data is written to this bit." (RX-4261 at 4:20-21.) Figure 2 of Yano shows that the data strobe signal is asserted and then deasserted when valid data is on the data bus. (*Id.* at Fig. 2; RX-5429C at Q487.)

Similarly, Figures 2 and 3 of Dan show the strobe signal beginning as an internal write strobe on communication path 230 and then continues past write strobe gate 203 onto the write strobe line 256 as the external strobe signal. (RX-4262 at Fig. 2, 3.) Once the external strobe is asserted at time 323, as shown in Figure 3, the memory interface 120 places data on the data bus 250. (*Id.* at Fig. 3.) Once data is placed on the data bus 250, it is written to memory upon the clocking of the strobe signal. (*Id.*; RX-5429C at Q487.) Thus, the "strobe signal" limitations of the asserted Barth claims were well-known in the art as of the alleged October 1995 priority date of the Barth Patents. (RX-5429C at Q488.)

The evidence shows that it would have been obvious to one of ordinary skill in the art to combine the "strobe signal" from Yano or Dan with the write operation method described in Farmwald '037 to improve the efficiency and speed of data access operations by indicating to the target memory device that data is on the bus, thereby enabling higher-frequency data access rates. (RX-5429C at Q488; *see also* RX-5357 at 28.) The claimed "strobe signal" and the "strobe signal" in Yano and Dan perform the same, namely timing signal that initiates the capture of data off of a bus. (*Id.*) As such, combining the "strobe signal" from Yano or Dan with the known write operation method described in Farmwald '037 does no more than yield predictable results, and therefore such combinations would have been obvious to one of ordinary skill in the art. *See KSR*, 550 U.S. at 417.

Moreover, Farmwald '037, Yano, and Dan all sought to address the well-known need in

the industry for faster data access operations, including overcoming the inherent skew associated with various clocking schemes. (RX-5429C at Q488.) Farmwald '037 teaches that "[p]rior art memory systems have attempted to solve the problem of high speed access to memory with limited success." (*See* RX-4269 at 2:12-24.) Similarly, Yano describes "a design can be created which enables processing at a higher speed in comparison to the prior art example." (*See* RX-4261 at 3: 20-21.) And Dan discloses that "[t]o achieve an optimally functioning system, *i.e.*, peak performance, data should be held stable just long enough to meet external memory's timing requirements and not an instant longer." (RX-4262 at 2:1-4.)

(1) *Rambus's Arguments*

Rambus argues that Respondents' prior art combinations fail because Dan and Yano do not disclose the "strobe signal"/ "signal" elements of the Barth Patents and the combinations improperly combine synchronous and asynchronous systems. (CRB at 44-45.) As for the latter, argument, the ALJ found that combining synchronous and asynchronous systems would not be improper during the relevant time period. (*See supra* at Section VI.C.1.a.) Rambus's first argument also fails because, as set forth in the anticipation section (Section VI.B.1) the ALJ found that both Yano and Dan disclose the claimed "strobe signal" of the Barth Patents.

Therefore, the ALJ finds that Respondents have shown by clear and convincing evidence that Yano or Dan in combination with Farmwald '037 or SCI and JEDEC Release 4 and Farmwald '037 in combination with Yano or Dan render the asserted claims of the Barth Patents obvious.

d) NextBus and Harriman in combination with Farmwald or Release 4

As set forth *supra* in Section VI.B.1.c, the ALJ found that the NextBus Spec and Harriman each disclosed each and every element of claims 11-13 of the '353 Patent and claims

1, 20, and 24 of the '109 Patent. Furthermore, certain elements of claims 11-13 of the '353 Patent and claims 1, 20 and 24 of the '109 Patent are similar to certain elements in the asserted claims of the '405 Patent. Thus, to the extent that the elements of claims 1113of the '353 Patent and claims 1, 20 and 24 of the '109 Patent are disclosed in NextBus and Harriman, the analysis for those elements applies equally to like elements found in the asserted claims of the '405 Patent.

To the extent an element of a specific asserted Barth claim is not disclosed in the NextBus Spec or Harriman, it would have been obvious to one of ordinary skill in the art to combine that element from one of a number of prior art references with NextBus Spec, and/or Harriman. Specifically, it would have been obvious to one of ordinary skill in the art to combine NextBus Spec and Harriman with the teachings of either Farmwald '037 or Release 4. (RX-5429C at Q505.) And each of the four resulting combinations independently renders all of the asserted Barth claims invalid as obvious under 35 U.S.C. § 103. (*Id.* at Q505-06.)

(1) *Double Data Rate ("DDR") Claim Elements*

As set forth *supra* in Section VI.B.1.c, the ALJ found that NextBus and Harriman each disclose the DDR elements of the asserted Barth claims. However, to the extent that such elements are not found in those references, Farmwald '037 unquestionably discloses the all the DDR elements from the asserted Barth claims. And for the same reasons discussed previously in Section VI.C.1.b with respect to Yano and Dan, it would have been obvious to one of ordinary skill in art to combine the DDR elements from Farmwald '037 with each of the NextBus and Harriman. (RX-5429C at Q507-08.)

(2) *Precharge Claim Elements*

To the extent the precharge elements of the asserted Barth claims are not disclosed in the NextBus or Harriman, the ALJ finds that such elements are found in Farmwald '037 and JEDEC

Release 4 as discussed *supra* in Section VI.C.1.b. (RX-5429C at Q510.) In addition, it would have been obvious to one of ordinary skill in the art to combine NextBus and Harriman with Farmwald '037 for the same reasons discussed previously with respect to Yano and Dan. (*See* Section VI.C.1.b, *supra.*)

(3) *Multiple Memory Bank Claim Elements*

As set forth supra in SectionVI.C.1.b, the use of a memory having multiple banks is disclosed in Farmwald '037 and JEDEC Release 4. The evidence shows that utilizing the plurality of banks and the transmission of bank selection information disclosed in Farmwald '037 or JEDEC Release 4 with the write operations disclosed in the NextBus Spec and Harriman, respectively, would have been obvious to one of ordinary skill in the art. (*Id.* at Q514.)

(4) *Sense Amplifier Claim Elements*

As set forth *supra* in Section VI.C.1.b, Farmwald '037 discloses the sense amplifier elements.[23] Specifically, Farmwald '037 discloses commanding memory devices to perform a sense operation in response to a write command was a well-known method in the art, and such a command performs the same established function in the asserted Barth claims that it was known to perform in Farmwald '037. (RX-5429C at Q&A 516-518; *see also* RX-4269 at 10:47-55; 11:31-38.) The evidence shows that one of ordinary skill in the art would have been motivated to combine the sense operation elements from Farmwald '037 with the write operations disclosed in the NextBus Spec and Harrimam because all of these references sought to address the well-known need in the industry for faster and more efficient data access to memory. (RX-5429C at Q518.) Therefore, combining the sense operation elements from either Farmwald '037 or

[23] The evidence shows that because sense operations, including providing a control code to a memory device specifying a sense operation, would be inherent in DRAM write operations, each of the NextBus Spec and Harriman disclose the sense operation elements of the asserted Barth claims. (Id. at Q&A 515.)

Release 4 with the known write operation methods described in the NextBus Spec and Harriman, respectively, does no more than yield predictable results, and these combinations would have been obvious to one of ordinary skill in the art.

e) Farmwald in combination with NextBus or Harriman

As set forth *supra* in Section VI.B.1.e, the ALJ found that Farmwald '037 failed to disclose the claimed "strobe signal" element of the Barth Patents. Rambus only disputed whether Farmwald '037 disclosed the "strobe signal"/ "signal" limitation and does not dispute that Farmwald '037 discloses the other features of the Barth Patents. (CRB at 24-25.) The evidence shows that Farmwald '037 discloses the other limitations of the Barth Patents. (RX-4269; RX-5429C at Q&A 366-384.) Furthermore, certain elements of the asserted claims of the '109 Patent are similar to certain elements in the asserted claims of the '405 and '353 Patents. Thus, to the extent that the elements of the asserted claims of the '109 Patent are disclosed in Farmwald '037, the analysis for those elements applies equally to like elements found in the asserted claims of the '405 and '353 Patents.

The evidence shows that it would have been obvious to one of ordinary skill in the art to combine those elements from the NextBus Spec or Harriman with the disclosure of Farmwald '037 because all the references sought to address the well-known need in the industry for faster data access operations by overcoming the inherent skew associated with various clocking schemes. (RX-5429C at Q524, 526; RX-5357 at 28.) Furthermore, the evidence shows that it would have been obvious to one of ordinary skill in the art to combine the "strobe signal" from NextBus or Harriman with the write operation method described in Farmwald '037 to improve the efficiency and speed of data access operations by indicating to the target memory device that data is on the bus, thereby enabling higher-frequency data access rates. (*See id.*)

As set forth *supra* in Section VI.B.1.c, the ALJ found that NextBus and Harriman disclose the "strobe signal" elements of the asserted claims of the '353 Patent. Specifically, NextBus and Harriman both disclose the use of a strobe signal DSTB* to sample data. (*See* RX-4265.0049 at Figs. 4-11; RX-4266 at Fig. 9.)

The claimed "strobe signal" and the "strobe signal" in NextBus and Harriman perform the same, namely timing signal that initiates the capture of data off of a bus. (RX-5429C at Q526.) As such, combining the "strobe signal" from NextBus and Harriman with the known write operation method described in Farmwald '037 does no more than yield predictable results, and therefore such combinations would have been obvious to one of ordinary skill in the art. *See KSR*, 550 U.S. at 417.

(1) *Rambus's arguments*

Rambus argues that Respondents' prior art combinations fail because NextBus, Harriman and Farmwald '037 do not disclose the "strobe signal"/ "signal" elements of the Barth Patents. (CRB at 50-51.) However, as set forth in the anticipation section (Section VI.B.) the ALJ found that both NextBus and Harriman disclose the claimed "strobe signal" of the Barth Patents.

Therefore, the ALJ finds that Respondents have shown by clear and convincing evidence that NextBus and Harriman in combination with Farmwald '037 and/or JEDEC Release 4 and Farmwald '037 in combination with NextBus and Harriman render the asserted claims of the Barth Patents obvious.

The Dally Patents

To the extent that particular motivation to combine and prima facie obviousness arguments are considered, they are considered above with respect to certain elements of certain

claims. The ALJ deals with following remaining references.

f) Nakamura

According to Respondents, the asserted Dally patent claims would have been obvious in view of U.S. Patent No. 3,806,807 ("Nakamura") in combination with other prior art, such as Wafer-Level Integrated Systems: Implementation Issues (1989) ("Tewksburry") (RX-4416) or Mixed Digital / Analog Signal Processing for a Single-Chip 2B1Q *U*-Interface Transceiver (1990) ("Batruni") (RX-4117).[24] However, the Respondents' post-trial briefing only provided a cursory analysis of claim 1 of the '857 patent and attempted to incorporate by reference the witness statement of their expert Dr. Hajimiri as to the remaining claims and contested claim limitations. (*See* RIB at 194 (citing RX-5430C at Q/A 169-266).

The ALJ finds that the cursory treatment of these references violates the previously discussed instruction in Order No. 51 (September 15, 2011) that contentions are to be set forth in detail in the briefs. Accordingly, the ALJ finds that Respondents have waived their arguments with respect to Nakamura.

g) National Semiconductor Art

Respondents also attempt to rely on National Semiconductor's DP83840 device. The DP83840 is an Ethernet controller product that Respondents contend supports serial transmission, with pre-emphasis, over a twisted pair of copper wires. (RX-2360C.) Respondents argue that the DP83840 device provides the "Dally Solution" by performing pre-emphasis on a transmitter on-chip. (RIB at 189.) Respondents attempt to lump the DP83840 with U.S. Patent No. 5,541,957, issued to Lau (hereinafter referred to as "Lau"). (RX-4106; JX-142 at 60:8-10,

[24] Respondents confusingly discuss Nakamura in the anticipation section of their pre-trial brief, but appear to allege only obviousness with respect to that reference. (*See* RIB at 194-201.) The ALJ thus addresses Nakamura in the context of obviousness.

60:12-14.) They refer to the DP83840 and Lau as the National Semiconductor Art.

However, the Respondents' post-trial briefing only provided a cursory analysis of claim 1 of the '857 patent and attempted to incorporate by reference the witness statement of their expert Dr. Hajimiri as to the remaining claims and contested claim limitations. (*See* RIB at 189-194 (citing RX-5430C at Q/A 348-427).

The ALJ finds that the cursory treatment of these references violates the previously discussed instruction in Order No. 51 (September 15, 2011) that contentions are to be set forth in detail in the briefs. Accordingly, the ALJ finds that Respondents have waived their arguments with respect to the National Semiconductor Art.

h) Respondents Waived Additional Obviousness Combinations

The ALJ notes that Respondents list eighteen separate combinations of references that allegedly render obvious the asserted Dally claims. (RPB 292-93.) The ALJ finds that some of these combinations are mentioned in the other invalidity sections of their brief, and the ALJ has addressed them above in the context of those sections. Many of the alleged combinations, however, are not addressed elsewhere. Because Respondents have not provided any explanation on how these combinations render obvious the claimed inventions, Respondents have waived these arguments. *See* Ground Rules 8(f) and (h); Order No. 51.

Objective Indicia of Nonobviousness

As indicated above, one of the *Graham* factors that must be considered in an obviousness analysis, is "objective evidence of nonobviousness," also called "secondary considerations." *See Stratoflex, Inc. v. Aeroquip Corp.*, 713 F.2d 1530, 1536 (Fed. Cir. 1983) ("Thus evidence arising

out of the so-called 'secondary considerations' must always when present be considered en route to a determination of obviousness."). However, secondary considerations, such as commercial success, will not always dislodge a determination of obviousness based on analysis of the prior art. *See KSR Int'l*, 127 S.Ct. at 1745 (commercial success did not alter conclusion of obviousness).

i) Barth Patents

Rambus argues that that secondary considerations of non-obviousness include "traffic commercial success," long felt need, failure of others, copying and praise by others. (CIB at 101-102.) However, the ALJ finds that these secondary considerations cannot overcome the strong showing of obviousness in this instance. *Perfect Web Techs., Inc. v. InfoUSA, Inc.*, 587 F.3d 1324, 1333 (Fed. Cir. 2009) ("Moreover, as we have often held, evidence of secondary considerations does not always overcome a strong prima facie showing of obviousness.); *Sundance, Inc. v. Demonte Fabricating Ltd.*, 550 F.3d 1356, 1368 (Fed. Cir. 2008) ("Secondary considerations of nonobviousness--considered here by the district court--simply cannot overcome this strong prima facie case of obviousness.") (citing *Agrizap, Inc. v. Woodstream Corp.*, 520 F.3d 1337, 1344 (Fed. Cir. 2008)); *see also Dystar Textilfarben GMBH & Co. Deutschland KG v. C.H. Patrick Co.*, 464 F.3d 1356, 1371 (Fed. Cir. 2006) ("The presence of certain secondary considerations of nonobviousness are insufficient as a matter of law to overcome our conclusion that the evidence only supports a legal conclusion that claim 1 would have been obvious."). This is especially true in this instance where the evidence cited by Rambus in support of their secondary considerations is merely the testimony of Dr. Przybylski without any further citations to any other evidence. As set forth *infra* in Section IX, given the

issues with Dr. Przybylski's credibility, Rambus's reliance on his testimony as the only evidence of secondary considerations falls far short of overcoming the strong showing of obviousness.

j) Dally Patents

Rambus raises several secondary considerations of non-obviousness to support the validity of the Dally patents, including: commercial success, long-felt need, licensing, and praise by others.

(1) *Commercial Success*

Rambus argues that the Dally inventions have enjoyed substantial commercial success. However, the only evidence Rambus cites to support this claim are emails from Dr. John Poulton, Dally's co-worker who reduced the Dr. Dally's inventions to practice, (CX-6683C.0004), and Dr. Poulton's deposition and hearing testimony, (JX-99C.0028 at 95:4-8, 95:12-13, *id.* at 96:2-7, Tr. 1751:11-1752:1).

Rambus's effort to use the testimony of Dr. Dally's co-worker who worked with Dr. Dally to reduce the Dally inventions to practice to establish commercial success is unpersuasive. The ALJ finds that this bootstrapping cannot establish commercial success. First, Dr. Poulton's testimony is not completely objective because he was Dr. Dally's co-worker and helped to reduce the invention to practice and so the ALJ finds that it is entitled to less weight. Second, the ALJ finds that Dr. Poulton's statements are vague and cannot demonstrate the necessary nexus to establish that these particular claims are non-obviousness. *W. Union Co. v. MoneyGram Payment Sys., Inc.*, 626 F.3d 1361, 1372 (Fed. Cir. 2010) ("[T]he patentee must establish a nexus between the evidence of commercial success and the patented invention."). Indeed, Dr. Poulton admitted that he had not read the patent at the time he wrote the email (Tr. 1748:15-20; 1772:15-1773:1), and he scaled back his statements at the hearing. (Tr. 1773:11-

1774:1.) Finally, the ALJ finds that this evidence cannot overcome the extremely prima facie obviousness case discussed above. *See Agrizap, Inc. v. Woodstream Corp.*, 520 F.3d 1337, 1344 (Fed. Cir. 2008); *Muniauction, Inc. v. Thomson Corp.*, 532 F.3d 1318, 1328 (Fed. Cir. 2008); *Leapfrog Enters., Inc. v. Fisher-Price, Inc.*, 485 F.3d 1157, 1162 (Fed. Cir. 2007).

(2) *Long Felt Need*

Rambus also contends that the Dally inventions satisfied a long felt need. (CX-10764C.0145-145; JX-120.0013 at 1:25-39; JX-99C.0023 at 75:1-12; Tr. 1719:18-1720:9.) The ALJ does not find this flimsy evidence to be sufficient to establish that the Dally inventions satisfied a long felt need. In particular, the ALJ finds citation to the patent itself and also to Dr. Singer's testimony that relies solely on the same citation as evidence of long felt need particularly unpersuasive. It is certainly possible that there was a long felt need, but the evidence Rambus presented is completely insufficient to establish that and the ALJ gives it no weight. Moreover, even if this evidence did establish a long felt need that the Dally patents fulfilled, the ALJ finds the evidence cited by Rambus insufficient to overcome the strong prima facie case of obviousness. *See Agrizap, Inc. v. Woodstream Corp.*, 520 F.3d 1337, 1344 (Fed. Cir. 2008); *Muniauction, Inc. v. Thomson Corp.*, 532 F.3d 1318, 1328 (Fed. Cir. 2008); *Leapfrog Enters., Inc. v. Fisher-Price, Inc.*, 485 F.3d 1157, 1162 (Fed. Cir. 2007).

(3) *Licensing*

Rambus argues that many companies expressed an interest in licensing the Dally inventions. (CIB at 269-270.) In particular, Rambus argues that AT&T had actually licensed the Dally patents and former "Respondent nVidia also expressed interest in licensing or purchasing rights to the Dally patents, only to find out that Rambus already had the rights." (CIB at 269 (citing CX-7099C.0002 ("Based on what Bill [Dally] has briefly told me, NVIDIA might have

some interest in this patent, either to license or purchase.").) Rambus further argues that in addition to the interest shown by nVidia and AT&T, other parties have actually licensed the Dally patents as part of Rambus's SerDes license portfolio. Rambus contends that these licenses demonstrate that others have acquiesced to the validity of the claimed inventions and have chosen to adopt them rather than seek alternatives, thus objectively demonstrating the nonobviousness of the technology. (CIB at 270.)

The ALJ finds some weight should be given to this evidence, but not a great deal of weight. The ALJ concludes this for several reasons. First, there are a number of Dally patents and the nexus between these licenses and the particular claims at issue here is not particularly strong. Second, the ALJ notes that the Rambus portfolio licenses may be motivated by factors other than the validity of the Dally patents. In particular, the portfolio licenses may be motivated by avoiding litigation as Rambus has been engaged in a number of litigations over the past decade. Finally, without additional evidence regarding nVidia's interest in the Dally patents, the ALJ is reluctant to draw extensive conclusions from a single email. In sum, this evidence is not entitled to much weight, and in any event, the ALJ finds it is insufficient to overcome the strong prima facie case of obviousness discussed above. *See Agrizap, Inc. v. Woodstream Corp.*, 520 F.3d 1337, 1344 (Fed. Cir. 2008); *Muniauction, Inc. v. Thomson Corp.*, 532 F.3d 1318, 1328 (Fed. Cir. 2008); *Leapfrog Enters., Inc. v. Fisher-Price, Inc.*, 485 F.3d 1157, 1162 (Fed. Cir. 2007).

(4) *Praise By Others*

The final secondary consideration raised by Rambus is that members of the industry have also praised the Dally technology. (CIB at 270.) Rambus cites to testimony by Dr. Poulton, after presenting a paper disclosing the Dally technology at the Hot Interconnects conference in

1996, "people were pretty interested in this" and "[t]hey thought this was maybe a game changer, as, in fact, it turned out to be." (JX-99C.0023 at 74:8-11; *see also* JX-99C.0023 at 74:14-25; *id.* at 74:19-22; *id.* at 80:5-8.) Rambus also contends that several members of the industry, including Respondent LSI Logic, Respondent Hewlett Packard, AT&T, and Toshiba, expressed interest in the Dally technology following the presentation and publication of the Hot Interconnects paper. (CIB at 270 (citing JX-122.0097).) Rambus also argues that the 1996 Hot Interconnects paper was also the subject of a write-up in trade publication EE Times and was selected for publication in IEEE Micro as one of "the best papers from the [Hot Interconnects] symposium." (CIB at 271 (citing CX-6681C.0001; *see also* CX-6305C.0038).)

The ALJ finds that Rambus has completely failed to prove praise by others. First, the ALJ finds the evidence cited by Rambus to support this point unconvincing. As evidence of praise by others in the industry, Rambus cites a letter from Dr. Dally to a Dana Beach where he mentions "[w]e have had inquiries from LSI Logic, Hewlett Packard, AT&T and Toshiba." (JX-122.0097.) This second hand, vague, self-serving statement in a grant report is not sufficient evidence to establish praise by others. Rambus submits no evidence to explain what that statement means. Rambus's other evidence suffers from similar faults. Rambus claims that the paper related to the patents (the 1996 Dally Hot Interconnects Paper) was written up in the EE Times and selected as one of the best papers of the conference. However, to support this claim Rambus cites to an email saying the paper was accepted (CX-6681C.0001) (bland praise at best) and an email from Dr. Dally mentioning the EE Times article (CX-6305C.0038). The ALJ does not find this evidence persuasive in the least. Once again, Rambus submits a self-serving statement of the inventor to prove "praise by others," when it could have cited to the actual write-up. Nor does the ALJ find Dr. Poulton's testimony particularly probing. This testimony

relates to work he was intimately involved in, by his friend, and is years after the actual events in question. In sum, the ALJ finds Rambus's self-serving evidence to be utterly unconvincing. Even Dr. Poulton's testimony, the most probative (to use that word loosely) evidence offered, is still too vague to give any weight. His testimony that "people were interested" begs more questions than it answers. The ALJ finds that the evidence Rambus cites is simply too tenuous to overcome the clear prima facie case of obviousness in this case. *See Agrizap, Inc. v. Woodstream Corp.*, 520 F.3d 1337, 1344 (Fed. Cir. 2008); *Muniauction, Inc. v. Thomson Corp.*, 532 F.3d 1318, 1328 (Fed. Cir. 2008); *Leapfrog Enters., Inc. v. Fisher-Price, Inc.*, 485 F.3d 1157, 1162 (Fed. Cir. 2007).

D. Written Description

The first paragraph of 35 U.S.C. § 112 requires:

> The specification ***shall contain a written description of the invention***, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art … to make and use the same …

(emphasis added.)

The Federal Circuit has interpreted 35 U.S.C. § 112, ¶ 1, to require the patent specification to "describe the claimed invention so that one skilled in the art can recognize what is claimed." *Enzo Biochem, Inc. v. Gen-Probe Inc.*, 323 F.3d 956, 968 (Fed. Cir. 2002). In evaluating whether a patentee has fulfilled this requirement, the standard is that the patent's "disclosure must allow one skilled in the art 'to visualize or recognize the identity of' the subject matter purportedly described." *Id.* (quoting *Regents of Univ. of Cal. v. Eli Lilly & Co.*, 119 F.3d 1559, 1573 (Fed. Cir. 1997)); *see also Cordis Corp. v. Medtronic Ave, Inc.*, 339 F.3d 1352, 1364 (Fed. Cir. 2003).

Terms need not be used *in haec verba*. *Eiselstein v. Frank,* 52 F.3d 1035, 1038 (Fed. Cir. 1995). The written description requirement can be satisfied by "words, structures, *figures, diagrams,* formulas, etc." *Lockwood v. Am. Airlines, Inc.,* 107 F.3d 1565, 1572 (Fed. Cir. 1997) (emphasis added).

Barth Patents

Respondents argue that the Barth Patents are invalid for lack of written description. Specifically, Respondents argue (1) that "sampling" is not described in the specification; (2) neither the "strobe signal" or "signal" elements are timing signals used to sample data; and (3) the Barth Patents fail to describe how a "strobe" can be used in a write operation. (RIB at 21-28.) Respondents also argue that the claims are invalid because they do not recite a terminate signal. (RIB at 22 n.12.)

Rambus and Staff argue that the asserted claims meet the written description requirement. (CRB at 21-23; SIB at 40-45.)

The ALJ finds that Respondents have failed to prove by clear and convincing evidence that the asserted claims of the Barth Patents are invalid for failure to satisfy the written description requirement. First, as to Respondents' arguments related to the terminate signal, the ALJ finds that a few sentences in a footnote without any citations to evidence fails to meet the clear and convincing evidence standard.

With regard to whether the Barth Patents disclose sampling, the ALJ finds that the specification does, indeed, disclose "sampling." The evidence shows that data transfers include capturing data, and, in the systems described in the specification, capturing data is accomplished by sampling. (HTr. 2669-70; CX-10765C at 18-19.) The evidence shows that the Barth Patents disclose at least two data transfer operations, *i.e.*, read and write operations, both of which

involve a memory controller, a memory device, and data capture. For example, the "Field Of The Invention" explains:

> The present invention relates to dynamic random access memory (DRAM), and more specifically, to a method and apparatus for controlling *data transfers to and from a dynamic random access memory.*

('353 Patent, 1:11-14 (emphasis added).) A similar discussion appears on the "Detailed Description" of the Barth I patents, which reads in part:

> At step 814, the data is transmitted over the data bus 40 (BusData[8:0]). During this step, *the data may be transmitted to or from the target DRAM, depending on whether the data transfer operation is write or read operation.*

('353 Patent, 7:40-43 (emphasis added).) A person of ordinary skill in the relevant art would understand that during the write operation, the memory controller is the data transferring device and the memory device is the data receiving device, such that the memory controller "writes" data to the memory device. (RX-5429C, Jacobs Direct Q/A 148-149; Jacobs, Tr. 1052:01-03, 1056:07-14.) By contrast, during a read operation, the memory device is the data transferring device and the memory controller is the data receiving device, such that the memory controller "reads" data from the memory device. (RX-5429C, Jacobs Direct Q/A 145-147; Jacobs, Tr. 1052:04-06.)

Furthermore, the ALJ finds that it is of no import that the phrase "initiate sampling" does not appear in the specification or drawings and only appears in the claims (CX-10765C, Przybylski Rebuttal Q&A 108-119.) Respondents point to nothing to support their argument that the failure to include those exact words in the specification proves the patent invalid -- there is no *in haec verba* requirement. Rather, a specification can adequately support issued claims for written description purposes using alternative words or phrases and though implicit or inherent disclosure understood by a person of ordinary skill in the art. (*See* MPEP § 2163(I)(B) ("While there is no *in haec verba* requirement, newly added claim limitations must be supported in the

specification through express, implicit, or inherent disclosure.").) Here, the Barth Patent specification uses the alternative word "samples" in a manner consistent with usage of the related term "sampling" in the asserted claims. ('353 patent, 24:19-21, 29:42-44, and 37:23-25; Przybylski, Tr. 2734:03-06.) The Barth Patent specification describes signals that cause a memory device to "latch" data on transitions thereof. ('353 Patent, 2:25-26; Przybylski, Tr. 2736:07-2738:18.) The evidence shows that the specification uses the term samples and, for example, refers to "bus samples," which the Appendices show are taken twice per clock cycle. ('353 Patent at 19; JX-4 at 24:19-22, App. A, B.) Thus, the Barth Patent specification discloses sampling.

The ALJ finds that the Barth Patent specification also discloses the use of "strobe signal" or "signal" elements as timing signals. Specifically, the Barth Patents explain that both read and write operations may involve the use of a "strobe signal" to facilitate the transfer of data between the memory controller and the memory device. For example, a strobe signal can be used to "initiate sampling" of data propagated between a memory controller and a memory device, *i.e.*, to ensure that the receiving device captures data off the data bus when valid data is available for sampling. ('353 Patent, 8:59-64; CX-10765C, Przybylski Rebuttal Q&A 108-130; SX-5, Illustrated Dictionary of Electronics (5^{th} Ed. 1991) at 318, 360 525, 599.) In the context of a write operation in particular, the strobe signal "initiates sampling" of data by the memory device such that the memory device captures valid data received from the memory controller via the data bus. (CX-10765C, Przybylski Rebuttal Q&A 120-130.)

The Barth Patents disclose at least two distinct ways in which a strobe signal can "initiate sampling" as part of the write operation in the asserted claims of the Barth Patents. In one configuration, the strobe signal *indirectly* initiates the sampling of data: the memory devices in

the preferred embodiments of the Barth Patents can be configured to sample data during a programmable number of clock cycles after first detecting the strobe signal. (Jacobs, Tr. 1058:12-22; Smith, Tr. 908:15-909:12, 943:03-944:04; Przybylski, Tr. 2677:08-12.) Thus, a transition of the clock signal *directly* controls the actual sampling of data by the memory device and the strobe signal preceding the data *indirectly* initiates that process by informing the memory device when sampling is to begin based on the clock signal. ('353 Patent, 10:34-38; Przybylski, Tr. 2677:13-2678:23, 2724:04-2725:06.) One such embodiment is shown in Appendix A of the Barth Patents:

Symbol	Name	Meaning	Length
p	Precharge	Precharge is the closing of a page (deassertion of RAS) and can be caused by closing at the end of a transaction, or opening a page that has not previously been precharged	8 Clocks
s	Sense	Sense is the operation of loading the sense amps to prepare for a CAS and is caused by a command with Open required	8 Clocks
r	RAS	RAS always follows the sense, and is needed to insure that the minimum RAS low time of the core is met.	8 Clocks

Non-interleaved precharged 4 oct 1 bank RWWRR

Clk				!0	Bank				!1	Bank			
Cyc	BE	BC	BD [8:0]	!Col	0	1	2	3	!Col	0	1	2	3 !
35	----	wakeup 1	data 0 3	----	p0	---	---	---	----	---	---	---	---
36	----	----------	data 0 3	----	p0	---	---	---	----	---	---	---	---
37	----	----------	data 0 3	----	p0	---	---	---	----	---	---	---	---
38	----	----------	data 0 3	----	p0	---	---	---	----	---	---	---	---
39	----	req 1	open	----	p0	---	---	---	----	---	---	---	---
40	----	write	close	----	p0	---	---	---	----	---	---	---	---
41	----	pend 0	precharged 0	----	p0	---	---	---	----	---	---	---	---
42	----	----------	----------	----	p0	---	---	---	----	---	---	---	---
43	----	----------	----------	----	---	---	---	---	----	---	---	---	---
44	1 1	----------	----------	----	---	---	---	---	----	---	---	---	---
45	1 1	----------	----------	----	s1	---	---	---	----	---	---	---	---
46	1 1	----------	----------	----	s1	---	---	---	----	---	---	---	---
47	1 1	strobe 1	----------	----	s1	---	---	---	----	---	---	---	---
48	1 2	----------	data 1 0	----	s1	---	---	---	----	---	---	---	---
49	1 2	----------	data 1 0	----	s1	---	---	---	----	---	---	---	---
50	1 2	----------	data 1 0	----	s1	---	---	---	----	---	---	---	---
51	1 2	----------	data 1 0	----	s1	---	---	---	----	---	---	---	---
52	1 3	----------	data 1 1	----	s1	---	---	---	----	---	---	---	---
53	1 3	----------	data 1 1	1 0	r1	---	---	---	----	---	---	---	---
54	1 3	----------	data 1 1	1 0	r1	---	---	---	----	---	---	---	---
55	1 3	----------	data 1 1	1 0	r1	---	---	---	----	---	---	---	---
56	----	----------	data 1 2	1 0	r1	---	---	---	----	---	---	---	---
57	----	----------	data 1 2	1 1	r1	---	---	---	----	---	---	---	---
58	----	----------	data 1 2	1 1	r1	---	---	---	----	---	---	---	---
59	----	----------	data 1 2	1 1	r1	---	---	---	----	---	---	---	---
60	----	term 1	data 1 3	1 1	r1	---	---	---	----	---	---	---	---
61	----	----------	data 1 3	1 2	---	---	---	---	----	---	---	---	---
62	----	----------	data 1 3	1 2	---	---	---	---	----	---	---	---	---

('353 Patent , App. A.) In Appendix A, a write operation is instructed by the "write" command appearing at clock cycle 40. (Barth, Tr. 391:03-08; Przybylski, Tr. 2726:19-2729:03.)

Thereafter, the "strobe" is issued once and only once (for that write operation) at clock cycle 47, one clock cycle before data associated with that write operation appears on the data bus BD[8:0] at clock cycle 48 (and is latched into memory by operation of a clock signal). (Barth, Tr. 391:09-393:14; Przybylski, Tr. 2679:24-2681:18, 2682:03-18, 2729:09-2732:08.) As this embodiment illustrates, the "strobe signal" need not directly control the actual sampling of data by a memory device to nonetheless "initiate sampling" as claimed.

In the other configuration, a strobe signal may *directly* initiate sampling by itself controlling actual sampling of data by a memory device. As set forth in the JEDEC standard, a transition in the DQS strobe signal (high-to-low or low-to-high) after an initial assertion low causes a JEDEC-complaint memory device to capture data off of the DQ data bus:

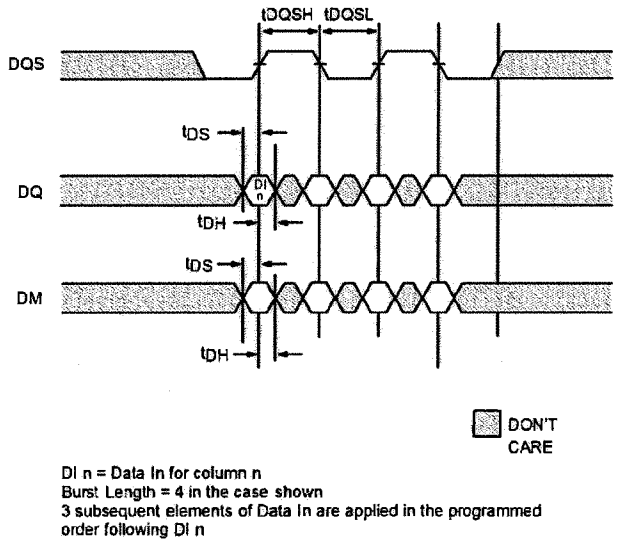


Figure 43 --DATA INPUT (WRITE) TIMING

(CX-4347.0070; *see also* Przybylski, Tr. 2721:06-14; CX-9543C, Przybylski Direct Q&A 336.) This direct control configuration differs from preferred embodiments described previously in that the memory device need not utilize a clock signal to capture data because the DQS signal transitions at the appropriate time (*i.e.*, when valid data is available for sampling on the DQ data bus).

However, a key similarity between the direct control configuration utilized with JEDEC-complaint memory devices (*i.e.*, where the DQS strobe signal controls the latching of data) and the indirect control configuration of certain preferred embodiments in the Barth Patents (*i.e.*, where a clock signal controls the latching of data after first detecting a strobe signal) is that both configurations utilize a strobe signal to *initiate* the sampling of data by a memory device as part of a write operation. The evidence shows that this broad concept, *i.e.*, the use of a strobe signal to initiate sampling, is adequately disclosed by the specification for written description purposes. (Przybylski, Tr. 2738:19-2739:13.) Therefore, the ALJ finds that the evidence shows that the Barth I patents provide written description support for a strobe signal that initiates the sampling of data associated with a write operation.

Dally Patents

The Respondents raise written description and indefiniteness challenges to the asserted Dally patent claims under 35 U.S.C. § 112. (*See* RPB at 205-209.) According to the Respondents, the asserted Dally patent claims suffer from the following two related problems:

(1) The term "output frequency" is indefinite (RIB at 205-207);

(2) "Output frequency" lacks written description (RIB at 207-209).

The ALJ finds that none of these arguments is supported by clear and convincing evidence. (*See* CX-10764C at Q/A 50-74.)

Respondents also cast their indefiniteness arguments as written description and enablement arguments. Specifically, Respondents argue that "the written description fails to enable one of skill in the art to make and use the invention" as it relates to the "unbounded range" limitation. (RIB at 207.) The ALJ notes that while the Respondents' brief attempts to label this challenge a written description challenge, the ALJ agrees with Staff that this challenge

solely raises an enablement challenge. Enablement was not raised in Respondents' pre-hearing brief, so it is waived. However, even if this argument was not waived, it is without merit. First, with respect to "written description" proper, as described, *supra*, there is substantial description for the term as the ALJ has construed it. *See PowerOasis, Inc. v. T-Mobile USA, Inc.*, 522 F.3d 1299, 1306 (Fed. Cir. 2008) ("[T]o satisfy the written description requirement, the missing descriptive matter must necessarily be present in the [original] application's specification such that one skilled in the art would recognize such a disclosure." (quotation marks and alteration in original)). Second, as for enablement, Respondents have utterly failed to meet the burden of proving by clear and convincing evidence that the claims are not enabled. To meet the enablement requirement, "the specification of a patent must teach those skilled in the art how to make and use the full scope of the claimed invention without undue experimentation." *In re Wright*, 999 F.2d 1557, 1561 (Fed. Cir. 1993) (internal quotation marks omitted). "Whether undue experimentation is needed is not a single, simple factual determination, but rather is a conclusion reached by weighing many factual considerations." *In re Wands*, 858 F.2d 731, 737 (Fed. Cir. 1988). As the Federal Circuit has explained:

> Factors to be considered in determining whether a disclosure would require undue experimentation ... include (1) the quantity of experimentation necessary, (2) the amount of direction or guidance presented, (3) the presence or absence of working examples, (4) the nature of the invention, (5) the state of the prior art, (6) the relative skill of those in the art, (7) the predictability or unpredictability of the art, and (8) the breadth of the claims.

Id. Respondents have failed to undertake any analysis under the *Wands* factors. The ALJ finds this insufficient to carry their burden for proving invalidity by clear and convincing evidence. Accordingly, Respondents § 112 arguments are without merit and are rejected.

E. Indefiniteness

Claims must ". . . particularly point[ ] out and distinctly claim[ ] the subject matter which the applicant regards as his invention." 35 U.S.C. § 112, ¶ 2; *Miles Laboratories, Inc. v. Shandon Inc.*, 997 F.2d 870, 874-75 (Fed. Cir. 1994). The purpose of this definiteness requirement is to ensure that the claims delineate the scope of the invention using language that adequately notifies the public of the patentee's right to exclude. *Young v. Lumenis, Inc.*, 492 F.3d 1336, 1346 (Fed. Cir. 2007). If a claim read in light of the specification reasonably apprises one of ordinary skill in the art of its meaning, that claim satisfies § 112, ¶2. *Id.* In contrast, if a claim limitation is "insolubly ambiguous" or "not amenable to construction," then the claim containing that limitation is invalid for indefiniteness. *See, e.g., Datamize, LLC v. Plumtree Software, Inc.*, 417 F.3d 1342, 1347-1356 (Fed. Cir. 2005) (affirming summary judgment of invalidity due to indefiniteness); *Honeywell Int'l, Inc. v. United States Int'l Trade Comm.*, 341 F.3d 1332, 1338-1339 (Fed. Cir. 2003).

Barth Patents

Respondents argue that the asserted Barth Patent claims are invalid for indefiniteness. (RIB at 28.) Respondents argument consists of only a single paragraph:

> All of the asserted claims are deficient for failing to distinctly point out and particularly claim the subject matter the applicants regarded as their invention. As stated, the invention relates to data transfer, not data capture. Accordingly, the claims cannot properly encompass the concept of "sampling," let alone the specific use of a strobe signal to "initiate sampling." Indeed, the only disclosure of how to use a strobe signal in the Barth specification is "to initiate data transfers from a memory device to a controller in a read operation." Likewise, the specification nowhere discloses the use of a "strobe" as a timing signal—instead, the clock is meant to be used as a timing signal. Notwithstanding the complete lack of supporting disclosure, the asserted claims are directed to the use of a strobe in connection with a write operation to initiate sampling. These claims fail to claim the applicants' invention and are thus invalid.

As an initial matter, the ALJ finds that Respondents cursory analysis and conclusory statements fail to rise to the level of clear and convincing evidence. Furthermore, even assuming that Respondents' analysis was sufficient, the ALJ further finds that Respondents have failed to show that the asserted claims of the Barth Patents are indefinite. In particular, Respondents' arguments in support of this defense parallel those for their written description defense. As set forth *supra* in Section VI.F, the ALJ found that the asserted claims of the Barth Patent are not invalid for failure to meet the written description requirement and for those same reasons, he finds that the asserted claims of the Barth Patents are not invalid for indefiniteness.

Dally Patents

The Respondents raise written description and indefiniteness challenges to the asserted Dally patent claims under 35 U.S.C. § 112. *See* RPB at 298-300. According to the Respondents, the asserted Dally patent claims suffer from the following two related problems:

(1) The term "output frequency" is indefinite (RIB at 205-207);

(2) "Output frequency" lacks written description (RIB at 207-209).

The ALJ finds that none of these arguments is supported by clear and convincing evidence. (*See* CX-10764C at Q/A 50-74.

Turning first to "output frequency of 1 GHz" limitation in claims 2, 31, and 49 of the '857 patent, the ALJ finds that the evidence shows that this phrase would be understood by a person of ordinary skill in the relevant art as referring to an output data rate of 1 Gbps as previously discussed in the claim construction portion of this brief.

Indefiniteness is a matter of claim construction, and the same principles that generally govern claim construction are applicable to determining whether allegedly indefinite claim language is subject to construction. *Datamize, LLC v. Plumtree Software, Inc.*, 417 F.3d 1342,

1348 (Fed. Cir. 2005). Indefiniteness, like claim construction, is a question of law, and we review a district court's entry of summary judgment on the issue of indefiniteness de novo. *Id.* at 1347.

The second paragraph of 35 U.S.C. § 112 requires that the specification of every patent must "conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention." This requirement serves a public notice function, ensuring that the patent specification adequately notifies the public of the scope of the patentee's right to exclude. *See Honeywell Int'l, Inc. v. Int'l Trade Comm'n*, 341 F.3d 1332, 1338 (Fed. Cir. 2003). A claim satisfies the definiteness requirement of § 112 "[i]f one skilled in the art would understand the bounds of the claim when read in light of the specification." *Exxon Research & Eng'g Co. v. United States*, 265 F.3d 1371, 1375 (Fed. Cir. 2001). A claim will be found indefinite only if it "is insolubly ambiguous, and no narrowing construction can properly be adopted...." *Id.* On the other hand, "[i]f the meaning of the claim is discernible, even though the task may be formidable and the conclusion may be one over which reasonable persons will disagree, we have held the claim sufficiently clear to avoid invalidity on indefiniteness grounds." *Id.*

As the claim construction analysis, *supra*, demonstrates, this term was easily amenable to construction. Respondents raise a new argument in their post-hearing brief that based on the Federal Circuit's case *Halliburton Energy Services, Inc. v. M-I LLC*, that claims are indefinite when they "did not place any limit on the scope of what was invented beyond the prior art." (RIB at 206 (citing 514 F.3d 1244, 1249-50 (Fed. Cir. 2008).) Respondents did not raise this argument in their pre-hearing brief. It is therefore waived. However, even if this argument was not waived, it is without merit. As Staff points out, Respondents' position is contrary to the very

case on which they rely, *Halliburton Energy*. In *Halliburton Energy*, the Federal Circuit explained that a claim may recite a range with no upper boundary and nonetheless be definite:

> [A] claim may contain a limitation that includes no explicit upper bound at all (*e.g.*, a claim limitation that requires "at least 5" of an element). Since such a limitation does not contemplate an upper bound beyond what is practically required (*e.g.*, the total percentage must be less than 100), the limitation may not present definiteness concerns.

Halliburton Energy, 514 F.3d at 1253 n. 5. Accordingly, the ALJ finds that Respondents have failed to meet the burden of showing that the claims are indefinite. *See Praxair, Inc. v. ATMI, Inc.*, 543 F.3d 1306, 1319-21 (Fed. Cir. 2008).

F. Utility/operability

The utility requirement of 35 U.S.C. § 101 requires that any patentable invention be useful such that the subject matter of a claim is operable. *Process Control Corp. v. HydReclaim Corp.*, 190 F.3d 1350, 1358 (Fed. Cir. 1999). Accordingly, "when an impossible limitation, such as a nonsensical method of operation, is clearly embodied within the claim," the claim is invalid. *Id.* at 1359. However, the fact that an invention may only have limited utility and may only be operable in certain applications is not grounds for finding lack of utility. *Envirotech Corp. v. Al George, Inc.*, 730 F.2d 753, 762 (Fed. Cir. 1984).

Respondents argue that the asserted Barth Patent claims are invalid for lack of utility. (RIB at 28-29.) Respondents argument consists of only a single paragraph:

> Rambus has asserted claims that require a strobe signal to "initiate sampling." However, if the term "initiate" in the asserted claims is given its plain and

> ordinary meaning of "to begin" or "to start," the claims[25] are rendered inoperable. As discussed, the strobe disclosed in the specification is received by the DRAM before the data, and does not continue signaling during the transfer. Were sampling to commence upon receipt of the "strobe," the system would register an error as there would be no valid data on the bus at that time. Further, sampling could not continue during the transfer because no strobe signal would exist to time the sampling of more than one beat of data. The "strobe" thus cannot "initiate sampling" of data by the DRAM from the bus during a write access. Accordingly, the asserted claims requiring the "initiation" of sampling are inoperable and therefore invalid for lack of utility.

As an initial matter, the ALJ finds that Respondents cursory analysis and conclusory statements fail to rise to the level of clear and convincing evidence. Furthermore, even assuming that Respondents' analysis was sufficient, the ALJ further finds that Respondents have failed to show that the asserted claims of the Barth Patents are invalid for lack of utility. In particular, Respondents' arguments in support of this defense parallel those for their written description defense. As set forth *supra* in Section VI.F, the ALJ found that the asserted claims of the Barth Patent are not invalid for failure to meet the written description requirement and, for those same reasons, he finds that the asserted claims of the Barth Patents are not invalid for lack of utility.

VII. INEQUITABLE CONDUCT

A. Applicable Law

A patent is unenforceable on grounds of inequitable conduct if the patentee withheld material information from the PTO with intent to mislead or deceive the PTO into allowing the claims. *LaBounty Mfr. Inc. v. U.S. Int'l Trade Comm'n,* 958 F.2d 1066, 1070 (Fed. Cir. 1992). "The accused infringer must prove by clear and convincing evidence that the applicant knew of the reference, knew that it was material, and made a deliberate decision to withhold

[25] Claims 11-13 of the '353 Patent, Claims 11-13, 15, And 18 of the '405 Patent, and Claims 1, 2, 4, 5, 12, and 13 of the '109 Patent.

it." *Therasense v. Becton, Dickinson and Co.*, 649 F.3d 1276, 1290 (Fed. Cir. 2011). The Federal Circuit has emphasized that

> [t]he need to strictly enforce the burden of proof and elevated standard of proof in the inequitable conduct context is paramount because the penalty to inequitable conduct is so severe . . . [j]ust as it is inequitable to permit a patentee who obtained his patent through deliberate misrepresentations or omissions of material information to enforce the patent against others, it is also inequitable to strike down an entire patent where the patentee only committed minor missteps or acted with minimal culpability or in good faith. As a result, courts must ensure than an accused infringer asserting inequitable conduct has met his burden on materiality and deceptive intent with clear and convincing evidence before exercising its discretion on whether to render a patent unenforceable.

Star Scientific, Inc., v. R.J. Reynolds Tobacco Co., 537 F.3d 1357, 1366 (Fed. Cir. 2008).

Intent and materiality are separate requirements for a finding of inequitable conduct and "a court must weigh the evidence of intent to deceive independent of its analysis of materiality." *Therasense*, 649 F.3d at 1290. A strong showing for one requirement cannot compensate for deficiencies in the other requirement. *Id.* ("A district court should not use a 'sliding scale,' where a weak showing of intent may be found sufficient based on a strong showing of materiality, and vice versa.").

Information that is withheld or misrepresented to the PTO is considered material if it satisfies a "but for" test:

> When an applicant fails to disclose prior art to the PTO, that prior art is but-for material if the PTO would not have allowed a claim had it been aware of the undisclosed prior art. Hence, in assessing the materiality of a withheld reference, the court must determine whether the PTO would have allowed the claim if it had been aware of the undisclosed reference. In making this patentability determination, the court should apply the preponderance of the evidence standard and give claims their broadest reasonable construction.

Id. at 1291-92. Previously the definition of materiality had been tied to PTO Rule 56, found at 37 C.F.R. 1.56, however, in *Therasense*, the Federal Circuit expressly disavowed that practice. *Id.* at 1293-94.

Although but-for materiality is required for a finding of inequitable conduct, there is an exception for cases of affirmative egregious misconduct. *Id.* at 1292. When a patentee has engaged in affirmative egregious misconduct—including but not limited to filing false affidavits—such conduct is considered per se material. *Id.* "Because neither mere nondisclosure of prior art references to the PTO nor failure to mention prior art references in an affidavit constitutes affirmative egregious misconduct, claims of inequitable conduct that are based on such omissions require proof of but-for materiality." *Id.* at 1292-93.

An inequitable conduct claim requires proof that the patentee acted with the specific intent to deceive the PTO. *Star Scientific,* 537 F.3d at 1366. A finding that a patentee was negligent or grossly negligent regarding an omission or misrepresentation to the PTO does not satisfy the intent requirement. *Therasense*, 649 F.3d at 1290. Specific intent to deceive can be inferred from indirect or circumstantial evidence; it cannot, however, be inferred from the materiality of the omitted or misrepresented reference. *Id.* at 1290; *see also Larson Mfg. Co. of S.D., Inc. v. Aluminart Prods. Ltd.,* 559 F.3d 1317, 1340 (Fed. Cir. 2009). Additionally, the absence of a good faith explanation for withholding a material reference does not, by itself, prove intent to deceive. *Star Scientific*, 537 F.3d at 1368. To satisfy the clear and convincing evidence standard the specific intent to deceive must be "the single most reasonable inference able to be drawn from the evidence." *Therasense*, 649 F.3d at 1290 (citing *Star Scientific*, 537 F.3d at 1366). When there are multiple reasonable inferences that can be drawn as reasons for withholding a reference, deceptive intent cannot be found. *Id.* at 1290-91.

Respondents argue that the asserted claims of the Barth Patents are unenforceable due to inequitable conduct. (RIB at 210-217.) Respondents argue that Rambus, the named inventors and the prosecuting attorneys withheld material non-cumulative prior art, namely RamLink and SyncLink. (RIB at 216.) Respondents argue that Rambus had knowledge of RamLink and SyncLink and that there was a clear intent to withhold these references from the Patent and Trademark Office. (RIB at 217.)

Rambus and Staff argue that the Barth Patents are not unenforceable due to inequitable conduct because RamLink and SyncLink are not material prior art references and there was no specific intent to deceive the PTO. (CIB at 51-53; SIB at 110-112.)

The parties do not dispute that Rambus was aware and/or had knowledge of RamLink and SyncLink. (CRB at 51-53; RIB at 210-216; SIB at 110-112.)

B. Materiality

The evidence shows that RamLink and SyncLink were cumulative with art before the Patent Office, and thus not material for purposes of inequitable conduct. *See Leviton Mfg. Co. v. Universal Sec. Instruments, Inc.*, 606 F.3d 1353, 1359 (Fed. Cir. 2010) ("[A] withheld otherwise material reference is not material if it is merely cumulative to, or less relevant than, information already considered by the examiner.") (citation omitted). RamLink and SyncLink disclose "flags" and a "clock signal" that are substantially similar to the AddrValid bit and clock signal, respectively, of the Farmwald prior art, which was submitted and considered during prosecution. (CX-10765C, Przybylski Rebuttal Q/A 403-451.) Thus, Respondents cannot show that the RamLink and SyncLink prior art is but-for material since the elements disclosed in those prior art references were already disclosed and considered by the examiner during prosecution and the

claims were still allowed. Therefore, the ALJ finds that Respondents have failed to show that RamLink and SyncLink are material prior art.

C. Specific Intent to Deceive

The evidence also shows that the named inventors and the prosecution attorney did not have a *specific intent* to deceive the Patent Office by withholding certain RamLink and SyncLink art during prosecution. Respondents merely allege that four of the named inventors and the prosecuting attorney "were *aware* of RamLink and/or SyncLink during prosecution of the Barth patents" and that the lack of explanation as to why these references were not disclosed to the PTO necessarily leads to the inference of "intent to deceive . . . from the facts and circumstances surrounding a knowing failure to disclose material information." (RIB at 217) (emphasis added). Under *Therasense*, however, the Federal Circuit held *en banc* that "a district court may not infer intent solely from materiality. Instead, a court must weigh the evidence of intent to deceive independent of its analysis of materiality." *Therasense*, 649 F.3d at 1290 (emphasis added). The Federal Circuit further explained that while specific intent to deceive can be inferred from indirect or circumstantial evidence, it cannot be inferred from the materiality of the omitted or misrepresented reference. *Id.* at 1290; *see also Star Scientific*, 537 F.3d at 1368 (the absence of a good faith explanation for withholding a material reference does not, by itself, prove intent to deceive). As such, Respondents have failed to show the specific intent required by *Therasense*. Rather, the evidence shows that none of the witnesses questioned at trial were aware of material prior art that was withheld during prosecution. (Vincent, Tr. 2247:21-2248:05, 2250:21-2251:01; Hampel, Tr. 369:04-08, 370:22-371:07; Barth, Tr. 474:09-14.) Thus, the ALJ finds that Respondents have failed to show by clear and convincing evidence that the named inventors and the prosecuting attorney had the requisite and specific intent to deceive the PTO.

Therefore, the ALJ finds that Respondents have failed to show by clear and convincing evidence that the Barth Patent are unenforceable due to inequitable conduct.

VIII. PROSECUTION LACHES

A. Applicable Law

According to the Federal Circuit, "[p]rosecution laches is an equitable defense to a charge of patent infringement." *Cancer Research Tec. Ltd. v. Barr Labs, Inc.*, 625 F.3d 724, 728 (Fed. Cir. 2010) ("*Cancer Research*") (citing *Symbol Techs., Inc. v. Lemelson Med.*, 277 F.3d 1361, 1366 (Fed. Cir. 2002) ("*Symbol Techs. I*")). "The doctrine 'may render a patent unenforceable when it has issued only after an unreasonable and unexplained delay in prosecution' that constitutes an egregious misuse of the statutory patent system under the totality of the circumstances." *Id.* (quoting *Symbol Techs., Inc. v. Lemelson Med.*, 422 F.3d 1378, 1385-86 (Fed. Cir. 2005) ("*Symbol Techs. II*")).

To the extent that a prosecution laches defense is based on continuation filings, the Federal Circuit has explained that "[t]here are legitimate grounds for refiling a patent application which should not normally be grounds for a holding of laches . . . ." *Symbol Techs. II*, 422 F.3d at 1385. Examples include:

- "Filing a divisional application in response to a requirement for restriction . . . ." *Id.*
- "[R]efil[ing] an application containing rejected claims in order to present evidence of unexpected advantages of an invention when that evidence may not have existed at the time of an original application." *Id.*
- "[R]efil[ing] an application to add subject matter in order to attempt to support broader claims as the development of an invention progresses . . ." *Id.*

Simply put, the mere passage of time and/or intent to cover after-arising technology is insufficient to demonstrate prosecution laches:

> [T]here is nothing improper, illegal or inequitable in filing a patent application for the purpose of obtaining a right to exclude a known competitor's product from the market; nor is it in any manner improper to amend or insert claims intended to cover a competitor's product the applicant's attorney has learned about during the prosecution of a patent application.

Medtronic, Inc. v. Boston Scientific Corp., 777 F. Supp. 2d 750, 781 (D.Del. 2011) (quoting *Kingsdown Med. Consultants, Ltd. v. Hollister, Inc.*, 863 F.2d 867, 874 (Fed. Cir. 1988)).

Respondents argue that the Barth and Dally Patents are unenforceable due to prosecution laches. (RIB at 219-228.) Specifically, Respondents base their prosecution laches defense on Rambus's conduct in JEDEC. Respondents argue that Rambus intentionally delayed the filing of its continuation applications for many years until JEDEC was locked into a standard and it could not design around the features covered by the Barth Patents. (RIB at 219.) Respondents argue that it was not until that time that Rambus filed continuation applications, nearly five years after the filing of the original patent application. (RIB at 219.) Respondents argue that such a delay was unreasonable and unexplained and that, during that time period, Respondents invested substantial resources in research and development of its JEDEC compliant products. (RIB at 210-220.) Thus, because Respondents have suffered material prejudice, the Barth Patents should be found unenforceable due to prosecution laches. (RIB at 220.)

For the reasons set forth below, the ALJ finds that Respondents have failed to prove by clear and convincing evidence that the Barth or the Dally Patents are unenforceable due to prosecution laches.

B. Barth Patents

The evidence shows that there were no unreasonable or unexplained delays in prosecution of the Barth Patents and thus no prosecution laches.

a) Prosecution History

(1) *U.S. Patent Application No. 08/545,292*

The initial Barth Patent application was filed on October 19, 1995 as U.S. Patent Application No. 08/545,292 (the "'292 application"). (CX-9696; CX-10773C, Killworth Rebuttal Q&A 82-86.) During prosecution, the application was subjected to a four-way restriction requirement which resulted in the applicants' electing one group of claims for initial prosecution. (CX-1077C, Killworth Rebuttal Q&A 88-90.) The application eventually issued as U.S. Patent No. 5,748,914 on May 5, 1998, less than three years after the initial application was filed. (*Id.* at Q&A 90.) As Mr. Killworth testified at trial, the evidence shows no indication of unreasonable and unexplained delays in prosecution during this brief three year period from initial filing to issuance. (*Id.* at Q&A 92-96.)

(2) *U.S. Patent Application Nos. 08/979,253; 08/980,091; and 08/979,402*

On November 26, 1997, the applicants filed three divisional applications off of the original '292 application, with each application corresponding to one group of unelected claims subjected to the restriction requirement noted above.[26] The '253 application eventually issued as U.S. Patent No. 5,966,731 on October 12, 1999, approximately two years after filing. (CX-10773C, Killworth Rebuttal Q&A 113-120.) The '091 application eventually issued as U.S.

[26] *See* U.S. Patent Application Nos. 08/979,253 (the "'253 application"); 08/980,091 (the "'091 application"); and 08/979,402 (the "'402 application"); CX-9697 (prosecution history for '402 application); CX-3068 (prosecution history for '091 application"); CX-3066 (prosecution history for '253 application).

Patent No. 5,913,046 on June 15, 1999, less than two years after filing. (*Id.* at Q&A 105-112.) The '402 application eventually issued as U.S. Patent No. 6,122,688, less than three years after filing. (*Id.* at Q&A 97-104.) As Mr. Killworth testified at trial, the evidence shows no indication of unreasonable and unexplained delays in prosecution during this brief two to three year period from initial filing to issuance. (*Id.* at Q&A 97-120.)

Moreover, the filing and prosecution of divisional applications *cannot* constitute prosecution laches because the applicants were required by the Patent Office to pursue these claims in separate and distinct applications. *See Symbol Techs. II*, 422 F.3d at 1385 ("Given one's entitlement to claim an invention in various ways, and the PTO's practice of limiting its examination of an application to only one of what it considers to be several inventions, it cannot, without more, be an abuse of the system to file divisional applications on various aspects that the PTO has considered to be separate and distinct from each other."). Indeed, the applicants' decision to pursue all three applications simultaneously when they could instead have pursued them serially indicates that the applicants did *not* delay in prosecuting these three applications.

(3) *U.S. Patent Application Nos. 09/480,767 and 09/561,868*

The next application in the Barth I family, *i.e.*, U.S. Patent Application No. 09/480,767 (the "'0767 application"), was filed on January 10, 2000 as a continuation of the '402 application. (CX-3069 (prosecution history of '0767 application").) The '0767 application was followed shortly thereafter by the '868 application, which was filed on May 1, 2000. (CX-9698 (prosecution history of '868 application").) The '0767 application eventually issued as U.S. Patent No. 6,810,449 on October 6, 2004, roughly four and a half years after filing. (CX-10773C, Killworth Rebuttal QAA 121-130.) The '868 application eventually issued as the asserted '353 Patent on July 8, 2003, roughly three years after filing. (*Id.* at Q&A 131-147.) As

Mr. Killworth testified, the evidence shows no indication of unreasonable and unexplained delays in prosecution during this three to four year period from initial filing to issuance. (*Id.* at 121-147.) Nor can the mere filing and prosecution of continuation applications alone constitute prosecution laches. *See Symbol Techs. II*, 422 F.3d at 1385 (discussing examples of proper continuation filings); CX-10773C, Killworth Rebuttal Q/A 128.

(4) *U.S. Patent Application No. 09/870,322*

U.S. Patent Application No. 09/870,322 (the "'322 application") was thereafter filed on May 29, 2001 as a continuation of the '868 application. (CX-9699 (prosecution history of '322 application").) The '322 application issued as the asserted '405 Patent on October 22, 2002. (CX-10773C, Killworth Q&A 148.) As Mr. Killworth testified, the evidence shows no indication of unreasonable and unexplained delays in prosecution during this roughly one year period from initial filing to issuance. (*Id.* at 148-162). Nor can the mere filing and prosecution of continuation applications alone constitute prosecution laches. *See Symbol Techs. II*, 422 F.3d at 1385 (discussing examples of proper continuation filings).

(5) *U.S. Patent Application Nos. 10/094,547 and 10/966,767*

The '322 application was followed by U.S. Patent Application Nos. 10/094,547 (the "'547 application") and 10/966,767 (the "'6767 application") on March 8, 2002 and October 15, 2004 respectively. (CX-3072 (prosecution history of '547 application); CX-9703 (prosecution history of '6767 application).) These two applications issued as U.S. Patent Nos. 6,931,467 (August 16, 2005) and the asserted '109 Patent (October 23, 2007) respectively. (CX-10773C, Killworth Rebuttal Q&A 163, 171.) As Mr. Killworth testified, the evidence shows no indication of unreasonable and unexplained delays in prosecution during this roughly three year period from initial filing to issuance. (*Id.* at Q&A 163-187.) Nor can the mere filing and

prosecution of continuation applications alone constitute prosecution laches. *See Symbol Techs. II*, 422 F.3d at 1385 (discussing examples of proper continuation filings).

As set forth above, the prosecution history of the Barth Patent family does not reveal any unreasonable and unexplained delays *in prosecution* of the relevant applications. "The relevant inquiry [in assessing prosecution laches] is not whether the patentee unreasonably delayed in *filing* specific claims in a patent application. Rather, it is whether the patentee unreasonably delayed in *prosecuting* those claims once filed." *Novo Nordisk Pharms. v. Bio-Tech. Gen. Corp.*, No. 02-cv-332, 2004 WL 1739720, at *33 (D. Del. Aug. 3, 2004) (internal citations omitted) (emphasis added). Nor do the Respondents identify even a single instance in which Rambus allegedly failed to prosecute its then-pending claims in good faith. Rather, the Respondents argue that Rambus failed to present the asserted "strobe signal" claims that eventually issued in the asserted Barth in order to draft claims that covered after-arising technology compliant with various JEDEC-standards. (RIB at 219-220.) However, the Respondents fail to cite any Federal Circuit or Commission precedent where this type of delay can serve as a basis for a finding of prosecution laches. Such actions do not result in prosecution laches. *SynQor, Inc. v. Artesyn Techs., Inc.*, No. 2:07-CV-497, 2011 WL 2729214, at *7 (E.D. Tex. July 13, 2011) ("[t]here is nothing unusual or improper about drafting claims to cover a competitor's product, as long as there is a basis in the pending application."); *Kingsdown Med. Consultants, Ltd. v. Hollister Inc.*, 863 F.2d 867, 874 (Fed. Cir. 1988). In this case, there is no evidence to suggest an unreasonable or unexplained delay in prosecution of the claims pending at that time. In fact, the Federal Circuit has twice confirmed that Rambus did nothing improper in pursuing claims that cover a JEDEC-standard or products intended to comply with various JEDEC standards *even while Rambus was itself participating in JEDEC as a member*. *See Hynix*, 645 F.3d at 1349; *Rambus*

Inc. v. Infineon Techs. Ag, 318 F.3d 1081, 1096-1105 (Fed. Cir. 2003) ("*Infineon*"). For at least these reasons, the evidence fails to show any of the Barth Patents to be unenforceable for prosecution laches. (CX-10773, Killworth Rebuttal Q/A 32-38, 78-187.)

Respondents have also failed to show that they were prejudiced by any alleged delay. The evidence shows that Rambus prosecuted all applications in the Barth Patent family in a reasonable time frame. Respondents' arguments, namely that Rambus "intentionally delayed the filing of its continuation applications for many years ... until JEDEC was locked into a standard," and that Rambus allegedly copied proposed industry standards, are irrelevant to establish prosecution laches.

C. Dally Patents

With respect to the asserted Dally patents, the Respondents only appear to raise one unenforceability defense: *i.e.*, unenforceability due to prosecution laches. (*See* RPB at 324-327.) While several headings in Respondents' Initial Post-Hearing brief mention the Dally patents and prosecution laches, there is no evidence or arguments presented with respect to prosecution laches in either the Respondents' Initial Pre-Hearing Brief or Post-Hearing Reply Brief. Accordingly, the ALJ finds these arguments waived. Even if they were not waived, the ALJ finds that the evidence cited by Staff establishes that there was no unreasonable delay as required to prove prosecution laches. *See Medtronic, Inc. v. Boston Scientific Corp.*, 777 F. Supp. 2d 750, 781 (D. Del. 2011).

IX. UNCLEAN HANDS

A. Applicable Law

"To succeed in an unclean hands claim, a plaintiff is required to show that the defendant has 'engaged in particularly egregious conduct which would change the equities significantly in the plaintiff's favor.'" *Serdarevic v. Adv. Med. Optics, Inc.*, 532 F.3d 1352, 1361 (Fed. Cir. 2008) (quoting *Aukerman Co. v. R.L. Chaides Constr. Co.*, 960 F. 2d 1020, 1032 (Fed Cir. 1992) (en banc)). "But it is not enough merely to show misconduct." *Id.* Rather, the party asserting unclean hands must show prejudice resulting therefrom.

The Respondents' unclean hands defense is rooted in Rambus' alleged spoliation of evidence. "Spoliation refers to the destruction or material alteration of evidence or to the failure to preserve property for another's use as evidence in pending or reasonably foreseeable litigation." *Micron Tech., Inc. v. Rambus Inc.* 645 F.3d 1311, 1320 (Fed. Cir. 2011) (quoting *Silvestri v. General Motors Corp.*, 271 F.3d 583, 590 (4th Cir. 2011).). The instant that litigation becomes reasonably foreseeable, a duty to preserve evidence arises. *Id.* If a violation of that duty is found, the next inquiry is to determine whether there is evidence of bad faith and prejudice to the opposing party. *Id.* At 1328-29. If bad faith is found, the alleged spoliator has the burden of proving, by clear and convincing evidence, that the destruction did not prejudice the opposing party. *Micron*, 645 F.3d at 1328. (citing *Anderson v. Cryovac, Inc.,* 862 F.2d 910, 925 (1st Cir. 1988).)

The parties dispute certain aspects of the *Micron* spoliation inquiry as they relate to Respondents' unclean hands defense and, more specifically, to Rambus' alleged destruction of materials relevant to the Barth Patents. Much of the parties' dispute focuses on who bears the burden of proving destruction (or lack thereof) of relevant materials, and, correspondingly, what materials were actually destroyed by Rambus and the extent to which Respondents were

prejudiced by Rambus' actions. The parties also dispute the extent to which Rambus should be sanctioned in the event that spoliation of relevant materials is found.

B. Rambus Violated its Duty to Preserve Evidence Because Litigation was Reasonably Foreseeable by July 1998

Rambus argues repeatedly that it could not have foreseen litigation on the Barth Patents because the patents had not issued and the litigation preparation Rambus undertook did not consider the Barth Patents. (CRB 64-69.) Rambus also contends that the findings in *Micron* and *Hynix* are irrelevant for purposes of the "reasonable foreseeability" inquiry in this investigation because it was based on different patents, products and parties. (*See* CIB at 235.)

As the Staff noted, the inquiry set forth in *Micron* and *Hynix* focuses on whether litigation against *some* party on *some* patents was reasonably foreseeable. (SIB 85.) The Staff concludes, however, that while the evidence shows that Rambus foresaw litigation related to the Farmwald-Horowitz patent family, Rambus did not foresee litigation related respect to the Barth Patents because the first Barth Patent was not issued until 2002. (SIB 92.)

The ALJ declines to read *Micron* and *Hynix* as suggesting that Rambus could intentionally destroy (in bad faith) materials relevant to both its Farmwald-Horowitz litigations on DRAMs and this subsequent Barth litigation on DRAM controllers, but still proceed unhindered in this investigation on the grounds that it had reasonably foreseen only near-term litigation against a different party with different products on different patents when the materials were destroyed. Both Rambus' and the Staff's argument fail as the Federal Circuit did not set forth the narrow requirement reasonable foreseeability to litigation based on *issued* patents.

Rather, the spoliation inquiry here is broader: whether Rambus reasonably foresaw litigation prior to July 1998 and, thus, had a duty to preserve evidence. Reasonable foreseeability is an objective standard that asks not whether the party in fact reasonably foresaw

litigation, but whether a party similarly situated would have reasonably foreseen litigation. *Micron*, 645 F.3d at 1320. The standard is flexible and fact-specific, allowing the district court "to exercise the discretion necessary to confront the myriad factual situations inherent in the spoliation inquiry." *Id.* (citing *Fujitsu Ltd. V. Fed. Express Corp.*, 247 F.3d 423, 436 (2d Cir. 2001).) In *Micron,* the Federal Circuit upheld the district court's findings that litigation involving Rambus' Farmwald-Horowitz patent family and various DRAM manufacturers was reasonably foreseeable. *Id.* at 1325-26.

The ALJ finds that Rambus not only could foresee, but was planning litigation involving the Barth Patents as early as July 1998 and, as such, had a duty to preserve the evidence. In *Micron*, the Federal Circuit found five circumstances weighed in favor of finding spoliation: (1) Rambus adopted its document retention policy to further litigation; (2) Rambus was on notice of potentially infringing activities by particular manufacturers; (3) Rambus took steps in furtherance of litigation; (4) Rambus was the plaintiff-patentee; and (5) the relationship between Rambus and manufacturers did not make litigation less likely. *Micron*, 645 F.3d at 1322-25. Following *Micron*, the ALJ concludes that because the same five circumstances are present here and Rambus reasonably foresaw litigation by July 1998.

First, it is evident that Rambus implemented its document retention policy to further Rambus' litigation policy concerning multiple patent families. Their action in destroying documents was intended to frustrate the fact-finding efforts of parties adverse to Rambus. As stated by the Federal Circuit in *Micron*, "This is a natural reading of getting "[b]attle ready," *Micron*, 645 F.3d at 1322, and Joel Karp acknowledged that "battle ready" meant preparing "for the war of litigation." (Karp, Tr. 1917:11-15.) Rambus attributes the recommendation to become "battle ready" to outside counsel, Dan Johnson. (Karp, Tr. 1917:16-1918:1.) However,

when asked if he recalled the phrase Dan Johnson stated that he did "recall the substance" but did not "normally talk about making somebody battle ready." (JX-058C.0018-19, 1493:19-1494:1.) His intention was to [redacted] (JX-058C.0019, 1494:1-5.)

Rambus' argues that, because the Barth Patents were not issued at the time of the alleged spoliation then they could not reasonably foresee litigation related to those patents. (CIB 64-65.) Rambus filed, Patent No. 5,748,914 (the original Barth Patent) in October 1995. (JX-09.0344; Barth, Tr. 445:17-19.) Nothing in the record indicates that Rambus implemented a document retention policy that treated information relating to the Barth Patents any differently from information relating to the Farmwald-Horowitz patents. In his 2007 testimony in Delaware, Mr. Karp stated that the battle readiness step was not patent specific and was not taken only in regards to the Farmwald Horowitz Family. (Karp, Tr. 1918: 15-19; RDX-4813.) Preparing a document retention policy was one of Rambus's general "IP litigation Activity" goals in the second and third quarters of 1998. (RX-477C; RX-500C; RX-2990C.) These goals did not specifically reference the Farmwald-Horowitz Patents or the Barth Patents. (*Id.*) On July 22, 1998, Karp emailed a document retention policy to Rambus employees and made presentations to Rambus employees on what to discard. (JX-60C.0192 at 271:3-23; RX-506C; RX-507C). At the bottom of at least seven slides in all capitals, Karp wrote "LOOK FOR THINGS TO KEEP." (RX-507C; JX-60C.0195-196 at 274:23-275:7.) Mr. Karp instructed Rambus engineers to look for things to keep that would help establish conception and prove that Rambus had intellectual property, but did not limit his instruction to a specific patent or patent family. (JX-60C.0188 at 267:5-16; RX-506C; RX 507C.) Mr. Karp's presentation's first page stated that even, "[e]-mail

is discoverable in litigation . . . Elimination of e-mail is an integral part of document control . . . e-mail message should be deleted as soon as they are read." (Karp, Tr. 1949:24-1950:17; JX-507C.) The document retention policy Rambus implemented instructed employees to selectively retain evidence that would help Rambus and destroy other, discoverable evidence. (*See* Hampel, Tr. 328:15-22; JX-0049C.0194-195 at 168:18-169:7.) However, in instructing engineers and employees, Mr. Karp never limited the document retention policy to only the Farmwald Horowitz patents: when asked whether there was a distinction between information concerning Farmwald Horowitz patents or information concerning other patents or inventions within Rambus, Mr. Karp answered that it was neutral. (Karp, Tr. 1950:10-17.) Rambus' implementation of a document retention policy as an important component of its general (i.e. not patent-specific) litigation strategy makes it more likely that litigation was reasonably foreseeable. *See Micron*, 645 F.3d at 1322.

Second, Rambus was on notice of potentially infringing activities by particular manufacturers. Rambus repetitively references the Federal Circuit's analogy in *Micron* to loading a gun ("Once the patent issued, the gun was loaded; when the targets were acquired , it was cocked; all that was left was to pull the trigger" *Micron*, 645 F.3d at 1323.) and concludes that because the Barth Patents were not issued, litigation could not be foreseeable. (CIB 135, 160; CRB 66.) This argument also fails. The Federal Circuit used the analogy only to show that Rambus was on notice of potentially infringing activities by particular manufacturers, which weighed in favor of finding that litigation was objectively foreseeable. *See Micron,* 645 F.3d at 1323. The Federal Circuit did not state that a patent must be issued for litigation to be reasonably foreseeable. *Id.* Thus, the proper question is not whether the Barth Patents had

issued before the 1998 shred day as Rambus argues, but rather if Rambus knew that particular parties were engaging in activities that Rambus could ultimately use to show infringement.

Although the activity may not have been infringing at the time, the evidence shows that Rambus intended to make additional claims that would encompass their activity. In 1995, Tate sent an email to the executive board stating that "it would be very helpful if at any time you have an e-mail talking about competitive technology developments/directions (example JEDEC meeting reports, et cetera) If you would add Adienpenb to your distribution list." (Tate, Tr. 1342: 3-8; RX-772C). "Adienpenb" is the e-mail address for Anthony Diepenbrock, Rambus's in house patent counsel. (Tate, Tr. 1339:22-1340:1). Additionally, Mr. Crisp, who worked with Mr. Barth to enhance claim coverage of the Barth Patents and monitored JEDEC meetings, was continuously feeding Rambus executives information regarding the standards JEDEC intended to implement. (Tate, Tr. 1337:16-1338:15; RX-456C; Hampel, Tr. 312:3-10; Barth, Tr. 404:21-405:2, 407:2-8.) Tate would forward the information from Mr. Crisp to Mr. Barth. (Tate, Tr. 1338:24-1339:2.) Mr. Barth testified that he received an email from Mr. Crisp dated June 6th 1995, in which Mr. Crisp said that Rambus should do whatever is necessary to get a claim to "shoot SynchLink in the head." (Barth, Tr. 406:1-13; RX-4288C.) SynchLink was a competing DRAM control company. (*Id.*) Mr. Crisp would also drop off copies of JEDEC meeting materials at Barth's desk. (Barth, Tr. 407:17-24.) From Mr. Barth's testimony alone, is clear that the information from JEDEC was used to draft the claims of the Barth Patents. (Barth, Tr. 407:17-408:15.)

Thus, Rambus was more than on notice because, by its own admission, it intentionally broadened the Barth Patents' claims to cover JEDEC standard-compliant products. While the Barth Patents may not have been mature, they were a part of a long term strategic litigation plan.

According to a "Strategy Update" dated October 1998, the top priority was strengthening Rambus's patent portfolio, including claims covering SDRAM, DDR, SLDRAM, and controllers. (Karp, Tr. 1962:25-1963:13; RX-517C.) To the extent that Rambus must be on notice of potentially infringing activities, the ALJ finds that Rambus's actions, namely intentionally broadening its claims to encompass the JEDEC standard, clearly satisfies this requirement. In other words, Rambus "created" the infringement by claiming JEDEC compliant products and, as such, was clearly "on notice."

Third, early on Rambus took steps evidencing it was furthering a long term litigation plan. In a 1996 email, Mr. Tate told Anthony Diepenbrock, in house patent counsel for Rambus, to "prepare a patent minefield" (Tate, Tr. 1339:22-1340: 10; RX-448C). In a 1997 email, Mr. Tate wrote "[D]ave believes we should meet with intel . . . to get them aware that IF they were to consider a DDR chipset that there is a minefield of 60+ Rambus patents that would have to be avoided." (RX-468C.) Like Rambus' "battle ready" plan, the natural reading of "prepare a patent minefield" is that Rambus wanted to prepare multiple patents for offensive use. This patent minefield was clearly applicable to Barth controller patents as, shortly before filing the patent application for the Barth Patents, Rambus discussed expanding its patent portfolio to be more "controller centric" (RX-1094C; Tate, Tr. 1427:4-19.) Rambus' patents focused on expanding its claim scope to cover "auto-precharge" that "would have high harassment value" against controller manufacturers. (RX-2115C; Tate, Tr. 1331:20-1333:5.)

Furthermore, Rambus hired Joel Karp in October 1997 for the purpose of furthering its litigation campaign. (Karp, Tr. 1903:6-13, 1904:8-18.) At the time, it was Rambus' belief, and Mr. Tate in particular, that companies using memory chips or working on controllers that were not direct RDRAM were using Rambus' inventions. (Karp, Tr. 1905:4-1906:10; Tate, Tr.

1346:10-13; RX-475C.0006.) To avoid raising any red flags in the industry, Mr. Tate testified that his thought was to say "externally that Joel [Karp] is coming onboard to help us with contracts and IP licensing," (Tate, Tr. 1346:3-5; *see also* Karp, Tr. 1904:13-1905:3.), and to have Rambus's "spin control" ready to "downplay the whole infringement/IP issue." (Tate, Tr. 1345:25-1346:3; RX-472C; RX-473C.) In January 1998, Mr. Tate instructed Mr. Karp to prepare a litigation strategy for the March 1998 Board of Directors meeting. (RX-475C.002; Karp, Tr. 1906:17-1907:17; Tate, Tr. 1349: 17-25.) Mr. Karp testified at trial that his "sole focus" was the Farmwald Horowitz portfolio, but his interactions with Mr. Tate, who never directed Mr. Karp to focus on a particular portfolio, demonstrate that his focus was all Rambus IP. (Karp, Tr. 2015:25-2016:04.) Mr. Karp contacted the Cooley Godward firm, "looking for some litigation—somebody to provide him with litigation assistance." (JX-112C.0046-47 at 9:16-22, 10:19-24.) In a February 1998 meeting with Cooley attorneys Dan Johnson, John Girvin and Peter Leal, Mr. Karp noted [redacted]. (Karp, Tr. 2010:7-11; RX-484.) Mr. Karp also noted that Rambus needed to make itself "battle ready" and further stated [redacted] (Karp, Tr. 2010:15- 2011:1; 2011:22-2012:4; RX-484.) While Mr. Karp attributed these ideas to the three attorneys from Cooley (*Id.*), it is clear that litigation was foreseeable at this time as Mr. Karp himself noted that [redacted]. (Karp, Tr. 1918:22-1919: 16; RDX-4840.) On March 2, 1998, Mr. Karp presented a "Licensing and Litigation Strategy" to Rambus' Board of Directors that included a detailed litigation plan with a tiered litigation strategy, preferred venues, and a hierarchy of targets (RX-486C; RX 487C.) Thus, the evidence shows that Rambus was clearly preparing for litigation, including

preparing a patent minefield, hiring Mr. Karp, and presenting the board with a proposal for a 5% royalty, and reasonably foresaw litigation prior to July 1998.

Furthermore, the ALJ notes that Rambus has failed to present any evidence that it was truly preparing for a licensing plan, as it claims. (CIB 137-38.) There is no evidence that Rambus' efforts focused on preparing a licensing team, evaluating negotiating strategies, or considering "peaceful" action. Mr. Karp was aware that the 5% royalty request was about twice what companies were actually paying and he noted that it would push them to litigation. (Karp, Tr. 1918:22-1919: 16; RDX-4840.) In fact, Mr. Karp noted that Rambus "[n]eed[ed] to litigate against someone to establish [the] royalty rate" (Karp, Tr. 1920: 12-22; RX-484C.) It is evident that, at the very least, Rambus was planning a *litigation-based* licensing campaign making litigation reasonably foreseeable. In the absence of evidence supporting Rambus' claim that it was only pursuing a licensing plan, the circumstances show that Rambus took steps, not to further its licensing plan, but rather its litigation plan.

Fourth, just as in *Micron*, Rambus is again the plaintiff-patentee and the decision of whether to litigate is clearly within their control. *Micron*, 645 F.3d at 1325. Thus, it is more reasonable for Rambus, in the position of the patentee, to foresee litigation than it is for the manufacturers as the accused. *See Id.*

Fifth, the relationship between Rambus and the controller manufacturers did not make litigation significantly less likely. The Federal Circuit noted that "[i]n general, when parties have a business relationship that is mutually beneficial and that ultimately turns sour, sparking litigation, the litigation will generally be less foreseeable than would litigation resulting from a relationship that is not mutually beneficial or is naturally adversarial." *Micron*, 645 F.3d at 1325. Rambus argues that because no such relationship was alleged, this factor weighs in favor of

finding that litigation on the Barth Patents was not reasonably foreseeable by July 1998. (CRB 68.) Rambus misunderstands the Federal Circuit's opinion. In *Micron*, the relationship between Rambus and RDRAM manufacturers did nothing to make litigation *less likely*; the relationship was a neutral circumstance and, as such, did not affect the Federal Circuit's determination of reasonable foreseeability. *See Micron*, 645 F.3d at 1325. The Federal Circuit explained that when parties have a mutually beneficial business relationship and that relationship ultimately turns sour and litigation results, litigation is generally less foreseeable than litigation that occurs between parties whose relationship is not mutually beneficial or is naturally adversarial. *Id.* Because Rambus did not have a mutually beneficial and longstanding relationship with RDRAM manufacturers, Rambus could not use its delay tactics[27] to undermine the other considerations. *Id.* As in *Micron*, Rambus's relationship with controller manufacturers in this investigation did nothing to make litigation less likely. There is no evidence that Rambus had a mutually beneficial and longstanding business relationship with controller manufacturers. Thus, Rambus' argument, that "no such relationship is alleged here," is inapposite. Similarly, Rambus' delay in initiating litigation on the Barth Patents was a strategic part of its litigation plan as the Barth Patents were the long term component of the plan. Rambus has alleged no mutually beneficial relationship that would make litigation less likely or undermine the four other considerations discussed herein. Like in *Micron*, the ALJ finds that this factor is, at best, neutral.

In sum, Rambus repeatedly argues that litigation relating to the Barth Patents was not reasonably foreseeable. However, it is clear that Rambus's wide-spread document destruction was not patent specific. Furthermore, given the wide breadth of the document retention policy,

[27] The Federal Circuit explained Rambus' "delay tactics" as Rambus' intention to delay the initiation of litigation until the manufacturers were either too invested in RDRAM for the SDRAM litigation to negatively impact Rambus' sales or until Rambus had no choice but to sue because RDRAM was rejected. *Micron*, 645 F.3d at 1325. b

one can easily conclude that this certainly implicated the Barth Patents, especially since the parent patent US Pat. No. 5,748,614 was filed in 1995. It is safe to assume that any documentation relating to conception or reduction to practice was likely in existence during the relevant time period.

C. Rambus Destroyed Documents in Bad Faith

Rambus argues that the evidence cannot show bad faith because "Rambus did not destroy documents with the intent to impair the ability of *these* Respondents to defend themselves." CPB at 242 (emphasis added). Respondents argue that all of the facts that the Federal Circuit in *Micron* said "may lead to a determination of bad faith" are present in this case. The Staff argues that, while litigation was reasonably foreseeable on the Farmwald-Horowitz patent family, the degree of foreseeability and, thus, the corresponding degree of bad faith is significantly less in regards to the Barth Patent family.

Rambus' argument fails. For reasons similar to those discussed above with respect to "reasonable foreseeability," the Federal Circuit did not limit the scope of its "bad faith" inquiry to solely the particular parties, products and patents at issue in the litigations that followed shortly after the document destruction activities. *See Micron*, 645 F.3d at 1326-27. Thus, bad faith can be found even if Rambus did not necessarily intend to prejudice *these* parties in *this* investigation.

The Staff's argument also fails. Although the Barth Patents were not mature during the relevant time period, it is evident that Rambus intended to use the Barth Patents as part of its long term litigation plan: the Barth Patents were part of Rambus' "patent minefield." That Rambus prepared a long term litigation plan and, during the relevant time period, did not foresee *near term* litigation for the Barth Patents does not warrant a finding that Rambus did not have the

requisite intent to litigate under the Barth Patents or to impair the ability of the Respondents (or any other similarly situated defendants) to defend themselves. The evidence presented here not only shows that Rambus reasonably foresaw litigation but that Rambus intentionally sought to disadvantage the respondents and, thus, acted in bad faith.

To make a determination of bad faith, the district court must find that the spoliating party "intended to impair the ability of the potential defendant to defend itself." Micron, 645 F.3d at 1326 (citing *Schmid v. Milwaukee Elec. Toll Corp.*, 13 F.3d 76, 80 (3rd Cir. 1994).) The fundamental element in this determination of bad faith spoliation is "advantage seeking behavior" by the party with superior access to information relevant to the proceeding. *Id.* The Federal Circuit in *Micron* noted that a determination of bad faith might be found based on (1) facts showing the document destruction policy was adopted as part of a litigation plan; (2) facts showing selective execution of the policy; (3) facts showing Rambus acknowledged the impropriety of the policy; and (4) litigation misconduct. *Micron*, 645 F.3d at 1327.

The ALJ finds that the same factors present in *Micron* are present here and, therefore, support a finding of bad faith. The ALJ notes the presence of an additional, fifth factor that weighs in favor of a finding of bad faith: the lack of credibility and dishonesty shown by many of Rambus' witnesses.

Rambus Adopted its Document Retention Policy as Part of a Litigation Plan

Rambus' document retention plan was always discussed in the context and as part of its litigation plan. In Mr. Karp's notes from the February 12, 1998 meeting with Cooley Godward attorneys, Mr. Karp stated that Rambus needed to "[m]ake ourselves battle ready . . . Need company policy on document retention policy." (RX-484C) Mr. Karp acknowledged that "battle ready" meant preparing for the war of litigation. (Karp, Tr. 1917:11-17.) When Mr.

Karp presented Rambus' "Licensing and Litigation Strategy" to the Board in March 1998, he listed the document retention policy as a "near term action" and presented it to the Board in the context of Rambus "being prepared for this battle or war that was to take place." (RX-486C; JX-60C.0163 at 243:1-12.) Rambus' quarterly goals repeatedly classified the document retention policy under the heading "IP Litigation Activity." (RX-477C); *See also* RX-500C (Q3'98).) Further linking the policy to Rambus' litigation plan, employees were told to delete emails because emails were discoverable. (RX-488C; RX-612C.)

Although Rambus attributes the document retention policy to the "advice of counsel," specifically Dan Johnson of Cooley, the evidence does not support a finding that Rambus blindly followed Mr. Johnson's instructions. Dan Johnson did [redacted] Mr. Johnson's suggestion was based [redacted] (JX-058C.0019, 1494:1-5.) Furthermore, Mr. Johnson did not have all the information requisite to provide Rambus with a tailored opinion on its document retention policy: Mr. Karp never informed Mr. Johnson that Mr. Tate directed Mr. Karp in 1998 to prepare a litigation strategy for the Board. (JX-058C.0049-50, 1555:18-1556:8.) Even by July of 1999, Mr. Johnson had no indication that Rambus was ready to file litigation. (JX.058C.0045 at 1546, 17-23.) When Mr. Johnson gave his presentation in July 1998, he did not consider it a legal opinion or that he was telling them that they should dispose of relevant evidence that would relate to a patent claim. (JX-058C.0114, 172513-1726:2.) The ALJ finds Rambus' claim of reliance on Mr. Johnson misleading as Rambus did not disclose all relevant information to Mr.

Johnson that would have allowed him to render an appropriate legal opinion. Mr. Johnson's suggestion to implement a document retention policy was a generalized one with the underlying purpose being to organize documents and save searching expenses *if* Rambus ever found itself faced with litigation. Rambus did not disclose its intention of actively and repeatedly pursuing litigation.

Rambus Selectively Executed its Document Retention Policy

Rambus' document retention policy was one that preserved helpful documents and destroyed potentially adverse documents. Mr. Karp wrote "LOOK FOR THINGS TO KEEP" on nearly every slide he presented to employees regarding the document retention policy. (RX-507C; JX-60C.0195-196 at 274:23-275:7.) Mr. Karp instructed Rambus' engineers to look for things to keep that would help establish conception and prove that Rambus had intellectual property. (JX-60C.0188 at 267:5-16; RX-506C; RX 507C.) Mr. Hampel previously testified that he understood the document retention policy as one in which "you don't keep things that you don't need except for proof of invention. That's probably the one exception." (Hampel, Tr. 328:15-22.) Mr. Hampel also testified that Mr. Karp told Rambus personnel not to keep evidence that would cast doubt on the patentability of an invention (JX-0049C.0194-195 at 168:18-169:7.)

Mr. Karp, himself, showed the selectiveness of the policy when he frantically searched for a backup tape that evidenced conception. (Karp, Tr. 1945:3-1946:15.) Although Mr. Karp attempted to downplay the importance of the backup tape, he was "sweating bullets" trying to find the conception date on a backup tape. *Id.* It is unreasonable to conclude that searching for this tape "wasn't necessary" and that it was just "the way [Mr. Karp] approached the problem," when he was "sweating bullets" and, upon finding the tape, reported to Mr. Tate

that he found the tape. (*Id*; RX-475C.0088.) Mr. Karp clearly recognized the importance of saving some documents over others as the document retention policy implemented by Mr. Karp sought out helpful documents with no apparent concern for adverse documents. This "sweating bullets" incident evidences the selective execution of the document retention policy and further evidences Rambus' bad faith.

Rambus Acknowledged the Impropriety of its Destruction and Sought to Cover Up its Shredding

Mr. Karp, at the very least, acknowledged that Rambus' destruction may be improper as he attempted to keep concerns about the policy undocumented. In a May 14, 1998 email announcing that backup tapes would only be saved for three months, Mr. Karp stated that he would prefer to "discuss this issue [of the retention policy] face to face" and if an email is sent to "keep them brief, and keep the distribution narrow." (RX-493C). Additionally, Mr. Karp originally listed "I. organize 1999 shredding party at Rambus" under the "Licensing/Litigation Readiness" for Rambus' IP goals for Q3'99. (RX-539C.) In the final version, Mr. Karp moved the shredding party to the section titled "Database Maintenance" and changed the description to "[o]rganized document retention compliance event." (Karp, Tr. 1983:10-1985:2; RX-539C; RX-541C.) Mr. Karp testified that he would not have made the changes but for the inputs of Mr. Steinberg. (Karp, Tr. 1985:3-1986:15.) However, Mr. Steinberg testified that he did not know of a 1999 shredding party and denied discussing it with Mr. Karp at any time. (Karp, Tr. 1986:16-1987:1; RDX-4830.) Regardless of whether Mr. Steinberg suggested the change, this attempt to re-style the 1999 Shred Day also shows Rambus' acknowledged that its destruction of documents as related to litigation was improper and evinces Rambus' bad faith.

Rambus' Witnesses Were Dishonest and Lack Credibility

The ALJ finds that any statement made by Mr. Karp, Steinberg, Tate or other Rambus former employee witness that is not supported by other evidence, such as a document, has little if any credibility. Time and again they proved they either could not remember details that might be unfavorable or anything when asked by respondent's counsel, but could remember bits that were not in their notes or elsewhere if it might be of service to their cause. The number of such incidents, along with the pecuniary and other interest the witnesses have in the company and the case renders them unreliable. From the observations of the ALJ, it renders them dishonest as well.

The witnesses that were Rambus employees during the time frame in question were difficult to deal with. Not since the long ago era of the Watergate hearings have the words "I don't recall" been used so regularly in answering questions under oath. What stood out in the ALJ's mind however was not just the general "failure" of the memory of the witnesses, Joel Karp, Geoff Tate and others, but of the selective memories that were retained. When confronted with notes, slides and other evidence of their words or actions during the relevant timeframe, the witnesses offered little, accept that those words were on the paper. They could recall nothing else. An examination of the Rambus witness's testimony reflects the lack of credibility and honesty of the Rambus witnesses:

a) Joel Karp

Mr. Karp's first line of defense was failure to recall. In reviewing his testimony, it becomes clear that he made efforts to recall as little as possible on cross-examination:

> Q. But you also talked about what you had been doing more recently at Samsung?
> A. I don't recall the actual conversations we had. I think he knew my background very well. (Tr. at 1900:15-19.)

> Q. Okay. So because of that you got right on this and you, for one thing, had internal discussions within Rambus as to what kind of royalty rate you would be demanding on these non-compatible products, that is, products Rambus thought used its intellectual property but was not direct RDRAM?
> A. I really don't recall those specific meetings. I mean, if you could show me a document or something to refresh my memory on it. (Tr. at1908: 15-25.)

> Q. And SLDRAM was a potential competitive technology that had a data sheet? You obviously had a data sheet for it, right?
> A. I just don't recall. And I know what SLDRAM was, but I don't recall the data sheet.
> Q. My question was different. No one on the board said don't go forward with this retention policy or this licensing litigation strategy, right?
> A. I don't recall any of the comments the board made at that time. I don't recall if they made any comments. (Karp, Tr. at1931:17-21, 1926:23-1927:4, 1931:17-21.)

There are many other instances of Mr. Karp's absence of memory or failure to recall, and it would serve no purpose to detail them all here. His inability to remember anything that might hurt Rambus, coupled with his selective memory regarding things he considers helpful, rendered him as unreliable a witness as could be presented.

In addition to his selective memory, the ALJ believes that Mr. Karp's testimony was often at odds with the written evidence and other witnesses. Rambus's contention that it was only anticipating litigation on the Farmwald Horwitz patents (or on that portion of their intellectual property) is demonstrably false based on the evidence presented through Mr. Karp. After filing the specification for the Barth Patents, Mr. Karp had Rambus take its time to craft Barth patent claims not based on its own intellectual property, but on the independent work of others. (*See infra* Section IX.C.4.e (Barth).) This appears to be so that Rambus could know that these patents would be useful against competitors at the time and in the court of Rambus's choosing. Rambus crafted its claims not based on its inventor's notebooks, or its own research, but by looking at the work of other companies through JEDEC, or through analysis of the competitive products. (*See*

infra Section IX.C.4.e (Barth).) While there was nothing improper per se under the law with Rambus's attempts to draft the Barth claims to cover the JEDEC standard,[28] the ALJ finds that the *manner* in which Rambus went about this process was, in fact, improper. The Barth claims read on JEDEC compliant products because Mr. Barth sat with the JEDEC standards, took notes and drafted claims. To use an analogy Rambus was fond of, to "get battle ready" Rambus "inventors" sent spies to the enemy (JEDEC), and developed from the result of spying, weapons specifically designed to defeat them. (*See infra* Section IX.C.4.e (Barth).) This battle readiness was stated by Mr. Karp many times – from 'why hurry' to letting others get to the point of no return. When Mr. Karp stated he only worked on preparing for the Farmwald patents, in the shredding and in the preparing for litigation, that testimony contradicts his own prior testimony, the documentation in the case, and other Rambus witnesses' recollection. Not only do Mr Karp's notes make no distinction between the patent families in preparing for battle, but his instruction to Mr. Vincent and his receipt of information from Mr. Vincent demonstrate that he wanted the Barth Patents, as well as the other files, ready for litigation. (Vincent, Tr. 2204 and 2212.) In his directions, there is never a distinction between any of the patents, proposed patents, or claims for use in the coming battles. (Karp, Tr. 1961-62.) Mr. Karp's notes and slides make clear that he was to manage Rambus' overall portfolio of patents and IP in order to do battle with Rambus' enemies, using whatever means were best for the given fight. (RX-486; Tr. 2015.) The distinction between using one family of patents over another is not one that was ever mentioned

[28] *See Kingsdown Medical Consultants, Ltd. v. Hollister, Inc.*, 863 F.2d 867, 874 (Fed. Cir. 1988) (It should be made clear at the outset of the present discussion that there is nothing improper, illegal or inequitable in filing a patent application for the purpose of obtaining a right to exclude a known competitor's product from the market; nor is it in any manner improper to amend or insert claims intended to cover a competitor's product the applicant's attorney has learned about during the prosecution of a patent application. Any such amendment or insertion must comply with all statutes and regulations, of course, but, if it does, its genesis in the marketplace is simply irrelevant and cannot of itself evidence deceitful intent.)

in the surviving documents of Rambus, but appears to be a doctrine that sprung fully from the imaginative minds of Rambus' litigation teams, post hoc.

Mr. Karp testified at trial:

> Q. Did your efforts in the non-compatible licensing program focus on any particular portfolio:
>
> A. The Farmwald Horowitz [portfolio] was my sole focus during, during the subsequent time.

(Karp, Tr. 2015:25-2016:04.) This statement regarding his focus is contradicted by every piece of physical evidence presented in the case regarding Mr. Karp's duties and the scope of his employment. Each time the scope of his duties or the scope of the shredding is mentioned, it is not limited to the Farmwald Horowitz portfolio. In his notes for a board meeting before shred day in September 3 1998, no distinction between families of patents was made:

> Q. And, again, there is no distinction here between types of intellectual information and intellectual or documents that are part of this document retention policy, whether it is Farmwald Horwitz or Barth or something else?
>
> A. It is totally content neutral.
>
> Q. And in this presentation there is no discussion about your doing this because of something Kroll told you or something Mr. Brill told you, correct?
>
> A. I just see the bullets on this slide. I really don't recall the actual, the actual discussion.
>
> Q. It is not in your presentation?
>
> A. It is not -- well, I don't know if it was in the presentation. It is not on the slide.

(Karp, Tr. at 1961: 21-1962:12.) That Mr. Karp was involved in far more than the Farmwald Horowitz patents is also proven by the testimony of Mr. Vincent, the outside patent counsel that Rambus used, and his interaction with Mr. Karp. When Mr. Karp [redacted]

[redacted]. (Vincent, Tr. 2204 and 2212.) He also did not tell Mr. Vincent about the litigation plans Rambus had – plans that may have created a legal duty on the part of Mr. Vincent to preserve the evidence had Mr. Karp told him.

Throwing things out and shredding was not limited to a single family of patents:

> A. We did a review of the files. We teed things up and looked at them all. And so, I mean, we didn't -- pending applications weren't, you know, cleaned.
>
> Q. Well, you were prosecuting various families of patents such as the Farmwald Horwitz family, right?
>
> A. Yes.
>
> Q. And the Barth family?
>
> A. Yes.
>
> Q. And the cleaning you did was not different depending upon which family you were cleaning, correct?
>
> A. Well, okay. The process of, you know, my secretary teeing up the files, going through the files, retaining, you know, prior art, various things in the right side with communications with the Patent Office and teeing up on the outside of the files some documents to be considered by me, whether or not we actually were going to purge them, you know, we did that systematically, you know, in terms of the teeing up through the files. But, you know, in terms of deciding whether to actually throw things out was kind of on a file by file basis, so, you know, in some instances, things might not have been thrown out.

(Vincent, Tr. 2212: 5-2213:3.) It is clear from the Vincent passage above and other passages, that the "document retention" was geared toward not just the Farmwald patents, but the entire portfolio of Rambus, including the Barth patents. Mr. Barth also testified to his belief that Mr. Karp's duties included the Barth Patents.

> Q. Besides yourself and Mr. Diepenbrock, was anyone else tasked with monitoring the patent prosecution activities around those and making sure that there was sufficient claim coverage on the features that you wanted?
> A. Well, Joel certainly had a role in that, once he came onboard.

Q. Can you tell us his last name?
A. Karp. (Barth, Tr. at 411:13-22.)

Q. And Mr. Karp was another person that was involved in monitoring patent prosecution activities and making sure that there was sufficient claim coverage on features, correct?
A. He certainly had job responsibilities with respect to patents, but as far as making sure that they are broad enough, yeah, yes, he did do some of that. (Barth, Tr. at 410: 20-411:2)

Finally, Mr. Karp's testimony regarding his duties undermines his efforts to convince the ALJ that he had limited responsibility to the Farmwald family. Mr. Karp testified regarding the possible loss of a document on date of conception.

Q. After you sent out this e-mail talking about the change in the policy, and before completely implementing it, you went and preserved a specific backup tape to establish a conception date for a Rambus invention, correct?

A. There was one point where I went to a backup tape to find the conception date because the document that was being saved on the engineer's workstation got corrupted. And my task was then to ask him to go find where -- to go find on that tape where we could reestablish that, that date.

Q. So if we can get the context, backup tapes that are more than three months old, that contain e-mails, you are going to get rid of those, erase those, and you didn't want this specific e-mail you were looking for or, I'm sorry, document you were looking for to be erased as part of that?

A. It wouldn't have been.

Q. Well, let me ask you this: You went to -- it was actually Rick Barth that you went to, correct?

A. Yes.

Q. And it was Mr. Barth you asked to call up something on his computer and that changed the date by just calling it up, right?

A. Yes.

Q. And you had to go to a backup tape which still existed at the time, right?

A. The backup tapes existed at that time, yes.

Q. And I think you testified that in doing that you put in hours of work, right?

A. Yes.

Q. And that you sweated bullets to try to find this conception date on a backup tape, right?

A. Right, the backup tapes are really used for system crashes, to recover from system crashes. And at that time my particular -- what I really wanted to see was let's find a tape where we can actually see maybe the very first instance of that, which really wasn't necessary, but that's what I wanted to do at that time.

Q. It was necessary enough that you were sweating bullets?

A. I could have gone to the most recent backup tape and I would have seen it, seen the same data because that would be carried forward on all future backup tapes.

Q. But at the time you said you were sweating bullets trying to find this?

A. Yeah, it is hard. There is no index. There is trillions of bits.

Q. Then you went and informed Mr. Tate that that backup tape still was working, right?

A. Well, the file we were looking for was found on a fairly old backup tape, that's correct.

Q. And you reported that to Mr. Tate?

A. Well, I have sent this --

Q. If you look at, again, your notes, 475C, and look at page 88.

A. Okay, I said backup tape still working.

Q. That was in connection with this search that you did to make sure you had the conception date or a conception date, correct?

A. Yes. Again, it wasn't necessary to do that but that's the way I approached the problem.

> Q. So after then you have the backup tape policy set out, eventually you did present an overall document retention policy to the employees at Rambus, correct?
>
> A. Right, implementation of backup tapes was part of the policy.

(Karp, Tr. at 1943:17-1946:19.) There are two things about this quick account of the hunt for a back-up tape that are important in this matter. First, as the Farmwald patents were already filed with the PTO and Mr. Barth was not involved with them, Mr. Karp's frantic efforts(" sweating bullets" and such) were not on behalf the Farmwald patents, but were on the Barth patents or other patents Barth was working on. If his sole responsibility were truly limited to the Farmwald patents, then he would not be responsible for the date of conception on other later patents. Yet, Mr. Barth knew to call Mr. Karp.. Second, the testimony also demonstrates (1) that the back-up tapes were used to preserve favorable things, and (2) that he spent "hours of work" to find the conception date for this "Rambus invention," which was not a part of the Farmwald family. Thus, in this brief passage of testimony, Mr. Karp once more confirms he was not just preparing the battlefield for the Farmwald patents, but he was doing so through a selective retention of materials from the great mass that he was preparing to destroy.

Mr. Karp's credibility is further undercut by his ready acquiescence to the testimony of other witnesses. Not only did Mr. Karp attempt to minimize the scope of his duties and conform his testimony to a fact pattern that would afford him the least amount of responsibility, he also seemed to defer to any other witness with a different story. In examining Mr. Karp's testimony regarding his conversation with Mr. Johnson, Mr. Karp tells the ALJ he (Karp) is not reliable. Here, Mr. Karp is confronted with Mr. Johnson's memory regarding the document retention plan. As shown below, when Mr. Karp believes there may be a witness that contradicts what he would say, he admits it is better to trust the other witness rather than to trust Karp:

A. Well, let me back up on that. I don't know -- they sent people over to help with the prosecution files at one point. I don't remember the date of that. It could have been before July.
And the other thing -- I just lost my train of thought. I do that a lot these days. I'm sorry, if it pops up in my mind, I will, but there was one other issue --

Q. Okay.

A. -- that I know he helped us with.

Q. So if Mr. Johnson testified that he was not involved in implementation of the plan and that he offered his services and you refused to accept them, or pay for them, not gratis, he would be mistaken?

A. I don't really know what he testified, but I know that if he testified to that, then that would be, that would be the actual case. And I just don't, I just don't know what he testified. And I don't know that I actually, you know, would say the same thing.

(Tr.at 1974 :11-22.) Rarely do you have a witness who will warn you not to trust him, but in Mr. Karp it may be the best advice he could give. Mr. Karp does not say he has a different memory, or does not know, but only that he does not know what Mr. Johnson testified to.

When Mr. Karp was confronted with a contradiction between his testimony and that of Neil Steinberg and documentation, he is unable to come up with a reasonable reconciliation, and skids into a series of implausible mis-statements:

Q. Then if we can go to what is page 1 in this exhibit, other activities in connection with this plan, you have document retention policy written and implemented. Training sessions were held. New system backup policy, correct, that's what you told the Board of Directors, right?

A. That's correct.

Q. You told the Board of Directors there was an all-day shredding party on September 3rd, right?

A. Okay.

Q. You told the Board of Directors that the plan was to monitor compliance through random spot checks, right?

A. Right, I told them that at that time, yes.

Q. And, again, there is no distinction here between types of intellectual information and intellectual or documents that are part of this document retention policy, whether it is Farmwald Horwitz or Barth or something else?

A. It is totally content neutral.

Q. And in this presentation there is no discussion about your doing this because of something Kroll told you or something Mr. Brill told you, correct?

A. I just see the bullets on this slide. I really don't recall the actual, the actual discussion.

Q. It is not in your presentation?

A. It is not -- well, I don't know if it was in the presentation. It is not on the slide.

(Trans. At 1961:4-1962:12.) As his testimony goes on, Mr. Karp not only contradicts Neil Steinberg, but in doing so manages to contradict the documentary evidence and himself, all in one passage:

Q. And then there is another example. Let's look at Exhibit 2990C. You have got third quarter of '98 under IP litigation activity, the first bullet point is implement the document retention action plan, right?

A. Yes.

Q. Now, I want to go fast forward now to June '99. At the time that you have been directed by Mr. Tate to pick a company to litigate against and then commence it in the first quarter of 2000. At that time you were getting heavy input from Mr. Steinberg on how you should do your IP goals, correct?

A. I don't know if I would characterize it as heavy input. I certainly had input on it from him.

Q. Let me show you Exhibit 539C. And this is the one I think where the third page might be a better copy. Can you look at the third page of this and see? This is type for legibility. The top is third quarter goals, final, July 1, 1999. Do you see that?

A. Yes.

Q. Let's go down to the bottom of this where it says, now it says, licensing/litigation readiness. Do you see that?

A. Yes.

Q. And at the bottom of this, this goes I'm sorry, this goes A through H, right?

A. Yes.

Q. And we go to the next page, and there is an I, which is also under this IP licensing litigation readiness. And it says, "organize 1999 shredding party at Rambus."

A. Yes.

Q. And what happened is you have a clear memory of showing this to Mr. Steinberg and him saying, [redacted]

A. Is this some -- I see what it says but these are the joint goals between Neil and I at this point.

Q. Well, let me show you Exhibit 541C. And you see this also says final, July 1, '99, right?

A. Yes.

Q. And if we go down to the licensing litigation readiness, we have A through H. Right?

A. Yes.

Q. And let's go to the next page. We no longer have "I" under licensing litigation readiness, right?

A. Okay.

Q. Instead under database maintenance, you have organize document retention compliance event.

A. Yes.

Q. So you took out the thing about the shredding party altogether, the language was changed?

A. There is a lawyer involved in this. And I'm sure that I created the original things. [redacted]

Q. And by lawyer, you are referring to Mr. Steinberg?

A. Mr. Steinberg, yes.

Q. And so you have, I think you testified, it is a clear memory that [redacted] right?

A. Well, I would recognize it as that even today without remembering exactly what happened then. This, this would have been [redacted].

Q. Well, actually, if we can put up RDX-4801. This is your November '97 testimony. I want to go through it quickly. Do you remember when you were presented with this previously, you said I have a clear memory of this one, and then you talk about showing this to Neil. And the second one, the one where you moved it and changed the language [redacted] Do you recall that?

A. Right. I think I just said that that would have [redacted].

Q. [redacted]

A. Yes.

Q. So given that, it would certainly be your memory -- if we can put up RDX-4830 -- this is testimony from Mr. Steinberg in his deposition where he had asked: "Question: Did you participate in the 1999 shredding party at Rambus, Mr. Steinberg? "Answer: No, and I don't even know of a 1999 shredding party. "Question: Did you discuss that with Mr. Karp at any time? "Answer: No, never." Your testimony is that would be inaccurate?

A. I don't recall anything about the 1999 shredding party -- I don't know if that – I don't know whether we ever discussed it or not. I just don't remember. I have no recall of anything like that. I don't even recall the shredding in 1999.

Q. Well, wait a minute. I am confused because you said in Exhibit 539C, [redacted] that the goal you had under licensing/litigation readiness under "I" -- the next page, Jeff – was "organize 1999 shredding party at Rambus." That's the thing that he told you to change the language of and to move to a different category?

A. Yes.

Q. Okay. And so, for example, if we can put up RDX-4845, this is what Mr. Steinberg testified.
"Question: Are you telling me that as you sit here today you never heard the word shred day used in the context of Rambus before? "Answer: I don't remember that phrase being used, correct." You recall you actually talked to him about that, about shred day, about a shredding party?

A. I saw that it was an initial goal and that he changed it to a different category. I don't remember any discussions related to it. I can see that that happened from the documents. They speak for themselves.

Q. He is the one who circled and changed it?

A. He made those changes.

Q. And the final on this, if we can go to 4845A testimony, Mr. Steinberg in Virginia: Did you participate in the organization of the 1999 shredding party at Rambus? "Answer: Gosh, I didn't even know they had a 1999 shredding party. "Question: That's news to you? "Answer: It absolutely is." Your testimony would be that's not news to him because he is the one that told you to change your goals so that that shredding party would not appear under litigation, correct?

A. Well, you are asking -- this is a different set of questions, I think. I don't know whether the shredding party ever took part. I totally agree with you that in the goals that we stated that we had that in there. Whether it ever happened or not is, I think, I think what we're talking about here. Not every goal we ever set was met. There were lots of goals that were not met.

Q. But there was a 1999 shredding party. And Mr. Tate sent an e-mail to the entire staff saying I hope you have a good time there.

A. And I don't remember it.

Q. So let's go forward then. After July '99 when you had your goals changed, I want to focus then on -- I want you to assume the shredding party is August 25th.

(Trans 1982:19-1989:18.) In this passage, not only do the two witnesses contradict each other under oath (Steinberg by deposition), but Mr. Karp accomplishes the impressive feat of contradicting himself on at least 4 separate occasions: from organizing a shred party to not knowing if one took place, from being certain he talked to Steinberg about it to not recalling if it

even took place. He cannot recall the party, or Mr. Tate's message. Mr. Karp knew about how the message was changed early and then he only knew what the document said. The ALJ finds this unbelievable. As a result of this and other aspects of his testimony, the ALJ finds that nothing that Mr. Karp stated that was not supported by documentation should be relied upon.

b) Neil Steinberg

Neil Steinberg was a similar witness and his testimony was entered through deposition. His statements in the above excerpts, and in his testimony regarding the shred days are not credible. Mr. Steiberg bears the additional burden of having been designated a 30 (b)(6) witness and charged with having knowledge of matters that included the destruction of materials:

> Q. Do you understand that you are here today pursuant to a Rule 30(b)(6) notice of deposition in the Micron Technology, Inc., versus Rambus, Inc., litigation?
>
> A. Yes.
>
> Q. I would like to show you what has been marked as Exhibit 12-14. If you could take a moment to look at that document, Mr. Steinberg? "And do you understand that you are the corporate designee for Rambus, Inc., for the topics contained in Exhibit -- and do you understand that you are the corporate designee for Rambus, Inc., for the topics contained in Exhibit Number 1214, Numbers 1 through 5?
>
> A. Yes.
>
> Q. Do you believe that you are under any obligation to conduct any investigation to familiarize yourself with the topics contained in 1 through 5?
>
> A. I don't know if I was under any obligation.
>
> Q. But did you do so?
>
> A. Yes.
>
> Q. Which is what you already have in front of you. Can you turn to page 2, please? Under subjects, the first subject is Rambus policies and procedures

> regarding the retention of documents, electronic mail, and electronically stored documents or other computer files. "Do you see that?
>
> A. Yes.

(Tr. at 1225:22-1226:13.) Mr. Steinberg makes a number of factual misstatements, from stating he believed that the burlap bags were only used once (Tr. p 1230) to stating that Rambus had never changed its document retention policy:

> Q. Has Rambus, since July 22nd, 1998 to the present, suspended its document destruction efforts at any time?
>
> A. I don't believe so. If I understand your question, I don't believe so.
>
> Q. Were you aware that Rambus went into litigation with Hitachi in January 2000?
>
> A. Rambus filed suit against Hitachi in January of 2000, yes.
>
> Q. Was there any change in Rambus' destruction of documents due to being in litigation with Hitachi in January 2000?
>
> A. There was no change in the document retention policy when we entered litigation with Hitachi.

(Tr. at 1231 :1-16.) This statement contradicts the other Rambus witnesses on when they put documents on a litigation hold (Hampel, Tr. 360), and also demonstrates that Mr. Steinberg has no idea what Rambus was doing regarding document retention. To make him available as a 30 (b)(6) witness, without more effort to give him the knowledge needed to answer the questions, bolsters the evidence that Rambus has engaged in bad faith throughout this and other litigations., Rambus has hidden information not just through shredding, but in providing witnesses who do not have the relevant information. While his attorney helped rehabilitate Mr. Steinberg regarding the use of litigation holds, it was clear that he was sent to deposition not to provide testimony, but to prevent disclosure. The ALJ further notes that Mr. Steinberg was not an

employee of Rambus during the first shred day and proclaimed he had no knowledge of it. Nevertheless, he was then able to testify that he did not know that Rambus had destroyed any documents that opposing parties might seek and be entitled to. Rambus also used the same tactic with another witness, Mr. Moniz, who testified that the prosecution files from Mr. Vincent had no documents destroyed from them. (JX-88.0051-52, 219.) However, Mr. Moniz had only received the files after Mr. Vincent had already purged them and could not provide the ALJ with any information regarding the relevant time frame. In effect, Rambus provided two witnesses, who were not with Rambus at the relevant time and place, to testify on the lack of destruction of relevant evidence. Such an approach certainly damages its credibility and the ability of the Commission and ALJ to rely on anything that Rambus has presented.

Turning back to Mr. Steinberg's 30(b)(6) testimony on document retention:

> (Videotape played and transcribed as follows:)
> Question: When you started at Rambus, was that before -- starting at Rambus, meaning started working for Rambus as outside counsel, was that before or after the September 5th, 1998 shred day?
>
> Answer: Firstly, I don't know what shred day means. Secondly, I've made clear to you that I don't know the exact day in which I started to work for Rambus as outside counsel. It was in the August, September timeframe, but I don't know -- I don't know how to answer that
>
> Question: Actually --
>
> Answer: -- other than to say I have no idea what you mean by September 5th shred day.
>
> Question: I think I made a mistake because, looking at the documents, I think it is September 3rd, so I don't want to trip you up, if it's the September 3rd shred day. Do you understand what that shred day was?
>
> Answer: I'll say it again. I don't know what is meant by shred day or September 3rd shred day or words to that effect.
>
> Question: Are you telling me that, as you sit here today, you never heard the word 'shred day' used in the context of Rambus before?

Answer: I don't remember that phrase being used, correct.

Question: Please mark this as the next exhibit. I've given you Exhibit 4135. Do you see that? That's an August 19th, 1998 e-mail from Ed Larsen to the staff at Rambus.

Answer: That's what it appears to be.

Question: And the subject line is Thursday, 9/30, which is September 3rd, shredder day. Do you see that?

Answer: I see that in the subject line.

Question: Have you ever seen this e-mail before, as you're sitting here right now?

Answer: I believe I was shown it yesterday, although I have no vivid memory of it, but I believe this was one of the documents that was shown to me yesterday. Prior to that, no, I'd never seen this before.

Question: But you do know that Rambus hired a shredding company to come to Rambus on Thursday, September 3rd, 1998; don't you?

Answer: I don't -- I don't – to that detail, no, I can't say I do know that.

Question: You do know that, in August of 1998, Rambus had burlap sacks passed around to all the employees, so that they could put documents in them, right? You know that, don't you?

Answer: You know, as I sit here today, no, I can't say I know that. This is -- you're talking about almost six years ago -- events almost six years ago, at the time when I wasn't an employee and would not have been provided this e-mail, if we assume that staff@Rambus.com means the employees of Rambus, so I wouldn't have been provided this. And I can't say that this event, as I sit here today.

Question: But you have come to learn, during your time as counsel for Rambus, that, in fact, Rambus passed out burlap sacks to their employees, so that the employees could fill them with documents to be shred, right? You've learned that?

Answer: As vaguely as you put it, no, I can't say I would agree with that misleading statement, but what I would say is that I did understand that, sometime in 1998, that in the -- with the implementation of the document retention policy, that employees were asked to retain certain documents in the performance of their responsibilities. That, I do remember in terms of finding that out during my tenure as employee of Rambus.

> Question: And you know, don't you, that the documents that the employees were not asked to retain, they were supposed to put into burlap sacks to be shred, don't you know that?
>
> Answer: No, I don't know that.

(Tr. 1243:7-1244:3.) If this were true, Mr. Steinberg was the only individual that did not possess this knowledge. Mr. Steinberg worked with Mr. Karp, Mr. Tate and many others at Rambus who did know about the shred days. He was their 30(b)(6) corporate witness. He could not have remained accidently ignorant on such matters. In any event, regardless of whether he was lying, deliberately ignorant, or some combination of the two, Mr. Steinberg violated his duties as a corporate witness.

Mr. Steinberg was similarly ignorant of events involving the document destruction while he was at Rambus:

> Question: Did you participate in the organization of the 1999 shredding party at Rambus?
>
> Answer: Gosh, I didn't even know they had a 1999 shredding party.
>
> Question: That's news to you?
>
> Answer: It absolutely is.

(Transcript. 1246:11-16.) Mr. Steinberg began at Rambus on April 26, 1999, and remained through at least 2001. His alleged lack of knowledge of such an event is highly improbable. A competent properly prepared witness would have been able to answer the question, and Mr. Steinberg had a duty to answer it. The ALJ found Mr. Steinberg's testimony to be untrustworthy in every sense of the word. Mr. Steinberg's testimony appeared to be dishonest and, as Rambus's 30(b)(6) witness, his poor recall is inexcusable.

c) Mr. Jose Moniz

There was another witness associated with Mr. Steinberg, Mr. Jose Moniz, who came to Rambus in September of 1999, having worked previously with Mr. Steinberg at Jones Valentine Steinberg & Whitt. (Tr., at 2262). Mr. Moniz was Mr. Steinberg's assistant. However, with regard to Rambus and its shredding days, he did not share his boss's ignorance:

> Q. You were not at Rambus when it rolled out its document retention policy, right?
>
> A. To my knowledge, that's correct.
>
> Q. You have heard, as part of your work for Rambus, that Rambus had a shred day in 1998, right?
>
> A. Sure.
>
> Q. And you weren't at Rambus for that shred day, correct?
>
> A. Correct.
>
> Q. And you have heard that Rambus had a shred day in 1999, correct?
>
> A. Yes.
>
> Q. And you were not at Rambus for that shred day?
>
> A. That's correct.
>
> Q. So you would not have any firsthand knowledge of whether documents related to the Barth patent files were destroyed during those shred days, right?
>
> A. Well, the knowledge I have is that the files were actually transferred to Rambus after I joined, so then, therefore, to the extent any shredding occurred, it would not have occurred in connection with the Barth files.
>
> Q. What do you mean when you say the files were transferred to Rambus after you joined, what files?
>
> A. The Barth files that preceded my joining Rambus.
>
> Q. Those files were transferred by Mr. Vincent, right?
>
> A. They were transferred from Mr. Vincent.

Q. When do you believe those were filed -- excuse me, transferred?

A. It was shortly after I joined, so it would be in the fall or winter of 1999.

Q. You would agree that Mr. Vincent would know best as to what date he transferred the Barth files to Rambus, correct?

(Trans 2265-22672265:10-2267:6.) It is beyond belief that Mr. Steinberg's assistant, who came to Rambus in 1999, would know about the shred days, while his boss, the designated corporate witness, would not. It is also typical of Rambus's approach to this case that in order to argue that files and parts of files were not destroyed, (or if some of the pages were, they were not relevant) to offer a witness who was not present in the relevant time or place in question. Mr. Moniz is at best another misdirection play for Rambus. In the 661 Investigation, Rambus called the ALJ's attention to the destruction of pizza boxes and phone books. In this investigation, they call the ALJ's and Commission's attention to the non-destruction of records, years later and at a different location, in a different business than the original destruction involving those files. To state it conclusively: Mr. Moniz's testimony is that there is not a shred of evidence that any material was lost from the Barth prosecution files when Mr. Moniz possessed them. However, that fact is not relevant in this matter because there is conclusive evidence of a shred by Mr. Vincent of information in those same files, at a time and place that is relevant.

d) Geoff Tate

Mr. Geoff Tate had many of the same flaws of memory that afflicted Mr. Karp. While under cross examination, he also seemed unable to recall anything pertinent to the case, his employment or Rambus:

Q. And between May of 1990 and late 1999, you were the chief executive officer and president at Rambus?
A. I think I went by the title of president. I don't recall the exact titles, I was the number 1 executive person there. (Tr. at 1316.:12-17.)

Q. Do you recall that there was a time in1998 when Rambus basically erased, degaussed electronic media tapes?
A. I have been deposed or testified 25 or plus times, so I have a hard time remembering what I would have recalled without all those intermediate events. So I don't recall specifically sitting here today. I know that it happened. (Tr. at 1318:6-14.)

Q. And do you recall there being a third shred day in 2000?
A. I don't know that I recall that, but I believe that that's -- that this is -- I'm not disputing the factual nature of this. If the dates are wrong, I'm sure the other side will indicate.
Q. Well, let me ask you, certainly toward in '98, '99, 2000, you were aware of the events that were taking place then concerning the destruction of documents at Rambus, correct?
A. I was aware that we had a document retention policy, and that involved destroying documents as well. (Tr. 1320:7-21.)

Q. As of -- yes or no, as of October 1, 1997, your belief is that some DRAM companies were infringing your patents and competing against you, yes or no?
A. I don't recall. (Tr. 1347: 15-17.)

Q. You asked Mr. Karp in January 7 of '98 to develop a litigation strategy and present it to a board meeting in March, correct?
A. Sitting here today, I don't have a recollection of that. I don't have a recollection of this one on one on January 7th, whatever this year was.
Q. And you deny that you told Mr. Karp, directed him January 7th, 1998, to develop a litigation strategy and present it to the board in March?
A. I don't have a recollection of what words I used or -- of this one on one with Mr. Karp, sitting here today, 14 years ago, if this was 1997.
Q. My question is whether you deny that this happened?
A. He wrote the words here. He will be here tomorrow. You can ask him. I don't have a recollection of what happened. I don't recall -- I don't know why he wrote his notes. I didn't get a copy of his notes. I hadn't seen them before depositions.

(Trans 1350:1-23.) Not only does Mr. Tate not recall the events that went on to make him personally, and his company, a great deal of money, but he does not even attempt to cooperate as a witness. The ALJ had not, in a long career in trial work, heard a witness tell his examiner that another party will be there tomorrow, and to ask him. (Tr. 1350.) That he should state he cannot recall his title, does not know if he recalls a third shred day, and does not recall if he thought

DRAM companies were infringing are all statements that that ALJ finds are unbelievable. Indeed, his failed memory continued throughout his time on the stand:

> Q. So let me split this up. First of all, then, you thought that competitors were using your technology to compete against you.
> That's what you just said, correct?
>
> A. Well, some competitors were using our technology to compete against us. And some of those companies were companies we were also working with to develop Rambus DRAMs and the source of their learnings was because we were teaching them through showing them how to make Rambus DRAMs or Rambus controllers.
>
> Q. Okay.
>
> A. They were starting to understand what we were doing and the value of what we were doing and they were incorporating it in some of their ideas, which -- well, they weren't their ideas, because they were using our ideas.
>
> Q. As of -- yes or no, as of October 1, 1997, your belief is that some DRAM companies were infringing your patents and competing against you, yes or no?
>
> A. I don't recall.
>
> Q. Well, let's fast forward, if we can, to show -- if we can, go to the time line quickly, we will go fast forward, past January '98 and I want to focus your attention on March 4, 1998 and, particularly, Exhibit 486C concerning a strategy presented at a Board of Directors meeting, if we can show 486. You recall this is a presentation that was made at a Board of Directors meeting?
>
> A. If I understand the meaning of "recall," no, I don't have a recollection of this. That doesn't mean it wasn't. We had a lot of meetings and there was a lot of slides and a lot of presentations. I don't know if this was presented at a board meeting or not, sitting here today.
>
> Q. Your memory of what happened a long time ago wasn't that good, is it? Not to fault you.
>
> A. It is not as good as it was five years ago and ten years ago.

(Tr. 1346:23-1347:19; 1350:24-1351:25.) The ALJ has never heard a live witness question his ability to understand the meaning of "recall," which is more disturbing in this case since it is a word Mr. Tate worked particularly hard. It calls to mind a phrase that condemned the legal profession: "It depends on what the meaning of 'is' is." The ALJ finds that this lack of cooperation and disregard for the trial and testimony has rendered Mr. Tate a completely unreliable witness. As a further example:

> Q. Okay.
> A. But you are asking, do I know that this slide was presented to the board? Sitting here today, I don't know that this slide was presented to the board. Maybe somebody else.
> Q. Okay. Well --
> A. I don't know, sitting here today.
> Q. Okay. So let's look at the presentation here then. We will determine later with another witness whether this was presented to your board.
> A. Okay.
> Q. And you see it talks about licenses with 5 percent royalty rates. Do you see that? Now, did Mr. Karp tell you that his view was that a 5 percent royalty rate would mean that you would have to go into litigation with someone? Just yes or no, did he tell you that?
>
> A. I don't have a recollection of that sitting here today. I believe that there is some sort of document or testimony that indicates something like that. (Trans. P 1352:1-23.)
>
> Q. And then in January of 2000, in fact,Rambus sued Hitachi in the ITC?
> A. Again, I don't have a recollection of that sitting here today. I believe at some point that we went to the ITC with some company.
> Q. Let me call your attention to the last page of this licensing and litigation strategy where it says near-term actions. The first near-term action in connection with Rambus's licensing and litigation strategy was to create a document retention policy. Correct?
> A. That's the words on this slide. (Trans. 1353:1-15.)
>
> Q. Okay. Now, you have testified that your belief after looking at these documents is that certainly Mr. Karp in late '97, early '98 was anticipating litigation?
> A. If you are referring to a piece of deposition testimony, I recall that there is something to that effect which I imagine you will show me shortly.

Q. Sure. Let's look at RDX-4406. Question -- this is from your deposition testimony on July 31, 2001. "Question: No, my question is, was Rambus's business anticipating litigation in late 1997 and early 1998 when Mr. Karp was brought in? "Answer: Apparently Joel Karp was, yes." And these goals which have document retention as part of IP litigation activity, those were done several quarters? I mean, it is not just -- it wasn't just the second quarter of '98. There were goals in the third quarter and in '99, correct?
A. I don't recall sitting here today. (Trans.1354:10 – 1355:8.)

Q. It is true, as you testified before, it wasn't usually your practice to notify employees of vacations you were talking, right?
A. I'm sorry, it was or was not?
Q. Was not.
A. I thought it was, but I don't recall sitting here today then. (Trans. 1362:1-1363:2.)

However, it is telling that Mr. Tate testified in a far different manner when Rambus's attorney asked him questions:

Q. Good morning, Your Honor. Mike Jakes for Complainant, Rambus. Good morning, Mr. Tate.

A. Good morning, Mr. Jakes.

Q. Why did Rambus decide to adopt a document retention policy?

A. Because we were advised by a lawyer to do so, and my recollection is we were told that companies that -- as they got larger, all adopted document retention policies and that we needed to do so as well.

Q. Did you follow that advice?

A. I kept more documents than the policy required, but we followed the advice to put in the document retention policy and advise our team.

Q. And so what did you understand that document retention policy to be?

A. I think that there was a category of documents where you were required to keep them for legal reasons, and it was important to make sure that all of your employees kept those documents, final drafts of contracts, you have to keep tax returns for certain periods of time. So there was lists of things that were required. And there was advice that other documents should not be kept.

(Tr. 1380:24-1382:1.) When Rambus's counsel questioned him, Mr. Tate's memory did not fail him once. His answers were coherent and he even volunteered material that he was not asked about. However, once he was again questioned by Respondents' attorney, Mr. Price, his earlier inability to recall any information, or to be helpful any anyway, returned. (*See* Trans. 1384-85, generally.)

Mr. Tate's credibility is further undermined by this interesting piece of testimony:

> Q. So you didn't tell him that obviously?
>
> A. I told you I didn't have a recollection of what I discussed with Mr. Johnson. You asked me if we were doing something. That's separate from your question about what I discussed with Mr. Johnson. I don't think with Mr. Johnson, that if he asked a question, I told him anything that wasn't truthful.

(Transcript 1384:16-24.) It is remarkable that a witness, under oath, cannot say for certain if he was honest with outside counsel regarding an important issue, namely document retention. If Mr Tate cannot be certain of his truthfulness then, it follows that the ALJ cannot be certain of his truthfulness now. Rambus's case rests on unreliable and false testimony in many important aspects.

These events were not minor. Rather they were major events that Mr. Tate was planning with Mr. Karp and, based on the records, were aimed toward completing a major goal of the company. (Trans P 1317). It is unbelievable that they cannot recall the most basic matters.

While the memories of these men, and others at Rambus, were vague and unsure, even when refreshed with their own notes, the witnesses were very good at recalling things that had no notes or other evidence associated with them, if those things appeared helpful to the Rambus legal case. For example, there is no written evidence that Mr. Karp relied on advice from outside counsel to form the document retention policy nor do his notes or slides indicate the policy came from outside. But, while he can recall nothing of so much, he now, after serving as a witness for

many years, "remembers" all the information came from outside counsel. It is far too convenient that the only memory the former Rambus employee witnesses claim to possess today are for things that are useful to the Rambus case and for which there was no written evidence. The ALJ finds that they have peculiar selective retention indeed and of such a nature that the ALJ discounts their testimony to the extent that it was not supported by other evidence.

e) Richard Barth

Mr. Barth was also an interesting witness for the events of this time period. While he is a named inventor on the patents, he did not refer to his notebooks, or the lab, or any other normal tools of the inventors' trade during his testimony. To the extent that he obtained his patent claims not from his own work, but from that of others, Mr. Barth appeared to be less an inventor, and more a copyist. Mr. Barth was in contact with those that were getting information on the competition in order to deter them. Mr. Barth was not focused on what Rambus had invented:

> Q. So let's put up RDX-2221 and, Mr. Barth, what we did was took an excerpt from one of the documents, RX-4288C, and this is an e-mail. This is from Mr. Crisp, correct?
>
> A. That's what it says, yes.
>
> Q. It was an e-mail dated June 6th, 1995, right?
>
> A. Yes.
>
> Q. And it specifically was sent to you, Mr. Barth, along with Allen Roberts?
>
> A. That's what it says.
>
> Q. And this is what Mr. Crisp told you at the time, "well, if it is possible to salvage and get anything that helps us get a claim to shoot SynchLink in the head, we should do it file whatever divisional is necessary. I am willing to take ownership of this if you guys cannot support it. I will simply make the time."
>
> Do you see that?

A. I see what it says, yes.

Q. And SynchLink was a competing technology for DRAM control, correct?

A. Yes.

Q. And when it talks about divisional, that's talking about patent prosecution, isn't it?

A. That's over -- part of that process, yes.

(Tr. 405:6-406:18.) This testimony is illuminating on two points. First, there is no discussion of the Barth patents actually covering the technology of SynchLink, but only of using a claim against the competition. It clearly indicates that Rambus is anticipating using a not yet filed divisional application against the competition. This is contrary to the contention that the only patents Rambus was considering for litigation were the Farmwald patents. The date of the e-mail is June 6th 1995 so it is clear that Rambus was planning its patent war that included the Barth Patents well before the time of the shred days. Second, Mr. Crisp indicates that if Mr. Barth and the others on the e-mail cannot do it he will: "I am willing to take ownership of this if you guys cannot support it. I will simply make the time." The ALJ notes that Mr. Crisp is not an inventor on any of the asserted Barth patents. If Mr. Barth and the others listed on the Barth I patents are the "inventors," how can Mr. Crisp "take ownership" and "make the time"? Clearly this is not a process of invention, but of entrapment of competitors.

Mr. Barth gave further testimony about the claims writing process at Rambus:

Q. For now let's get this point across. From time to time, Mr. Crisp would drop off copies of JEDEC meeting materials at your desk; isn't that right?

A. That's correct.

Q. And he was doing that so you can take a look at them, right?

A. Yes.

Q. And he was dropping off copies of JEDEC meeting summaries with other people at Rambus as well, correct?

A. I think that he did. I don't know who he gave them to in specific.

Q. From time to time, Mr. Crisp himself would come to you and ask to see your files so that he can look at the Rambus patents and patent applications himself, correct?

A. Yeah, I think I remember Richard wanting to look at some patent files, yes.

Q. And he offered that in this e-mail, he said, look, if you guys don't have the time to do it, I will take care of it. That's what he was saying in that e-mail, right?

A. That's what he was offering, yes.

(Tr. 407:17 – 408:15.) If the inventors are writing claims to cover their inventions, there is no mention of any one of them referring to their own work. Instead, a non-inventor is handing them the work of others and making sure that the claims cover the work of its competitors, rather than its own "inventions." Again, this is not something that was done in 1997, or 1998, but back in 1995. Rambus was readying the Barth Patents and creating their claims to use against others in the field from at least that time.

Mr. Barth also worked with Joel Karp, and in working with him understood the scope of Mr. Karp's duties:

Q. Another person that you worked with, Joel Karp. Do you recall Mr. Karp?

A. I do.

Q. And Mr. Karp was another person that was involved in monitoring patent prosecution activities and making sure that there was sufficient claim coverage on features, correct?

A. He certainly had job responsibilities with respect to patents, but as far as making sure that they are broad enough, yeah, yes, he did do some of that.

Q. Are you certain about that? Because we can play some more clip if you need to refresh.

A. It would probably be best to play the clip.

Q. Okay. Let's do that. June 28th, 2011, you were deposed, page 152, line 8 through

(Videotape played and transcribed as follows:)

"Question: Besides yourself and Mr. Diepenbrock, was anyone else tasked with monitoring the patent prosecution activities around those and making sure that there was sufficient claim coverage on the features that you wanted?

"Answer: Well, Joel certainly had a role in that, once he came onboard.

"Question: Can you tell us his last name?

"Answer: Karp."

(Tr. 410:17 – 411:23.) In contrast to Mr. Karp's own testimony, Mr. Karp did not represent to his coworkers that he only had responsibility for the Farmwald patents, or for licensing them. He had a role in prosecution activities and in ensuring the claims coverage was broad enough. Just as his notes and presentations made to Rambus suggested, he was establishing the patent minefield set, for all Rambus IP, including the Barth Patents.

Mr. Barth is forthcoming on the use of competitive products as the basis for forming claims in the Barth patents, even on ideas that were not in the specification at the time:

Q. And here for the '109 patent on the references cited and considered by the Patent Office in connection with your '109 patent prosecution, SynchLink is not listed anywhere, correct?

A. Well, I don't know what Konishi et al. is or Chesley. So if those don't reference SynchLink, then no.

Q. I will represent to you that they don't. Based on that representation, you would agree with me the '109 patent does not list SynchLink as one of the references considered by the Patent Office, correct?

A. According to your representations, apparently not.

Q. Isn't it true none of the SynchLink proposals and documents we saw were submitted by you or anyone at Rambus to the United States Patent Office while the '109 patent was being prosecuted there?

A. I certainly didn't do so. I have no way of knowing if anybody else did.

Q. Let me get this straight. You filed (sic) to submit SynchLink documents to the Patent Office that you had in your possession, despite the fact that you and others at Rambus were analyzing SynchLink as a competing technology at the time; is that correct?

A. Well, one amongst several others, I'm sure.

Q. But it is one of the things that you looked at for competitive analysis, correct?

A. The competitive analysis was not necessarily intimately associated with what we thought was appropriate to send to the Patent Office as prior art for any particular patent.

Q. So you are asking us to -- okay. Let me step back and ask you the next question. Mr. Barth, you failed to submit SynchLink to the United States Patent Office, despite the fact that SynchLink disclosed a strobe signal before you filed your original application for the Barth patents. Isn't that true?

A. It is clear that I knew about SynchLink before this patent application was submitted. Is that what you are asking?

Q. And you didn't submit SynchLink to the Patent Office, correct?

A. Apparently not.

Q. And you knew as we saw before that SynchLink had a strobe. That's what Mr. Crisp said in that summary, correct?

A. At some point in time, I knew that. Whether I knew that when I was trying to make up the list of prior art is speculative.

Q. Sitting here today in 2011, you really can't explain to us why you decided not to submit SynchLink to the --

A. Definitively, no.

(Tr. 447-450448:2-450:11.) Again, the ALJ notes that the issue is not that Mr. Barth drafted his claims to cover his competitor's products, which he is certainly allowed to do under the law to the extent that those claims are supported by the specification. The ALJ highlights this whole process to re-emphasize the fact that the Barth Patents were part of Rambus's ongoing litigation strategy and that the shred days and destruction of documents are relevant to this family of patents and not just the Farmwald family.

Mr. Barth's testimony also made it very clear that Rambus had destroyed some evidence that he had used in drafting the Barth Patents – evidence that Rambus knew it had a clear duty to preserve as evidenced by Mr. Tate and Mr. Karp. Here the questions and answers are referring to patent charts created by Mr. Barth:

> Q. I will represent to you that this application number here corresponds to the original filing of the Barth patents. Do you see that?
>
> A. I do.
>
> Q. Do you see the ID P048?
>
> A. I do.
>
> Q. P048, that's a code that Rambus was using to keep track of different types of patent filings, correct?
>
> A. It wasn't so much a type of patent filing as it was just a serial number for – as each one came along.
>
> Q. So P048 was for the Barth family, correct?
>
> A. I don't remember that. From this diagram, I assume that it is, given what you just told me.
>
> Q. Let's zoom back out and see if we can give you some more clarity. So off of P048, do you see these lines going down here (indicating)?
>
> A. Yes.

Q. And at the top?

A. Yes.

Q. And if you look at this box (indicating), that's the 6,591,353 patent. That's one of your Barth patents, correct?

A. Correct.

Q. Let's zoom back out. Go to the next box and zoom in. That's the 6,470,405, that's another Barth patent, correct?

A. I assume so. I don't remember all these numbers.

Q. Zoom back out. The last box here, this one here at the end, 7,287,109. That's another Barth patent, correct?

A. Okay.

Q. So based on this information, it is accurate to say that the P048 corresponded to the Barth patent family?

A. Yes.

Q. What I would like to do now is give you the opportunity to look -- at Rambus has identified five versions that it believes correspond to the conceptual tree.

A. Okay.

Q. In this investigation. So I want to walk you through each one. The basic question I am going to ask you is when you look at the conceptual tree is there any reference to the P048 code that corresponds to the Barth patents? That's my question. Do you follow me?

A. Yes.

Q. Okay. Let's go to the first one, RX-2468C. And these are also here in your witness binder so why don't we give him a copy.

A. Let me switch glasses. That will probably help.

Q. Robin, if you could hand him that document.

A. I have got it here.

Q. So we look at the first page, P048 is not there?

A. I don't see it.

Q. And the next page there are a bunch of P numbers. Do you see P048?

A. No.

Q. Next page. The last page of this one, do you see P048?

A. I don't see it.

Q. Let's go to the next conceptual tree document that Rambus alleges, which is RX-2469C. And actually, let's go -- there is a number of pages here. There is the same kind of list that shows up on page 12 and I want to focus your questioning on that, page 12. Again, we see a similar list of Rambus categorization, lots of P numbers. Do you see P048?

A. No, I don't.

Q. Next page? Do you see P048 on this page?

A. I do not.

Q. Let's go to the next document, RX-2470C. Mr. Barth, do you see P048 on this page?

A. I don't see any P numbers on this page.

Q. Let's go to the next one. Second page of 2470C, do you see any P048 references?

A. No, I don't.

Q. Next page. Any there with respect to P048?

A. No.

Q. Bear with me, two more 2471C, RX. Do you see any P048 references on this page?

A. No.

Q. In fact, you have testified before that you have kept handwritten notes from time to time on your conceptual tree, correct?

A. Correct.

Q. Can you tell whether these are your handwriting or not?

A. Not from what I can see right here. There is not enough resolution.

Q. Maybe let's zoom in to this section. Does that look like your handwriting?

A. No.

Q. Let's go to the last document or actually the second page of this document. Do you see any P048 there?

A. No.

Q. Next page.

A. Can you zoom it?

Q. Okay. Is this the last page? Okay. So the last document, RX-2472C, this is then last document that Rambus has identified as being one of the conceptual tree documents. Do you see any --

A. There are no P numbers on this page.

Q. Second page? Do you see any P048, sir?

A. Nope.

Q. Next page. Any P048?

A. I don't see any.

Q. Okay. So we have looked at the evidence. You would agree with me, Mr. Barth, that none of these versions of the conceptual tree documents produced by Rambus in this investigation contains a reference to the P048 number for the Barth patents, correct?

A. I didn't see any.

Q. Okay. And, in fact, you can't verify for me that these are the complete copies of the conceptual tree documents that you left behind in the filing cabinet when you walked away, correct?

A. No, I couldn't possibly remember all the versions of it.

> Q. And just looking at the documents, there is no way to tell whether these documents came from your filing cabinet or whether they came from some other source, correct?
>
> A. No.
>
> Q. That's because you didn't keep a record of what was in your filing cabinet, correct?
>
> A. I don't see why one logically follows from the other.
>
> Q. You would agree with me you didn't keep a record of what was in the filing cabinet?
>
> A. Other than what was in my head, no.

(Tr. 462:7-468:11.) In this testimony, Mr. Barth helps establish that the shred days and destruction of documents and e-mails by Rambus did destroy relevant evidence that Rambus had a duty to preserve. The evidence has clearly demonstrated Rambus did this in bad faith.[29] Mr. Barth testified that he had written on some of the conceptual trees while he was with Rambus and that none of the conceptual trees submitted into evidence contained his handwriting. and he further testified that certain patents were missing from the conceptual trees. Rambus has not presented any evidence that would meet its heavy burden that the vanished documents were of minimal import.

Mr. Barth testified further about how the Barth claims came into existence, upon the questioning by the ALJ:

> JUDGE ESSEX: Thank you. Just one moment before you get up there. Let me ask you a couple questions, because I am -- I have gotten the impression from a lot of the documents just flashed up here briefly that you were able to look at some competitor product, maybe SynchLink, other things, and generally the

[29] As set forth herein, this shifts the burden to Rambus to prove the lack of prejudice to the Respondents in the destruction of the documents. *Micron,* 645 F.3d at 1328, (If it is shown that the spoliator acted in bad faith, the spoliator bears the "heavy burden" to show a lack of prejudice to the opposing party because "[a] party who is guilty of . . . intentionally shredding documents . . . should not easily be able to excuse the misconduct by claiming that the vanished documents were of minimal import.")(citing *Anderson v. Cry-ovac, Inc.*, 862 F.2d 910, 925 (1st Cir. 1988).)

> JEDEC technology and are able to consider or write claims to make sure they encompass those things. Is that an accurate statement?
>
> THE WITNESS: Yeah, by and large.
>
> JUDGE ESSEX: All right. And do you know, do you recall if that included SynchLink?
>
> THE WITNESS: Well, given the evidence that I saw today, I must have had the SynchLink documents prior to actually filing that application.
>
> JUDGE ESSEX: All right. Now I am not an inventor and I am kind of new to patents, so follow me if you would, please. If you thought SynchLink was in the area, and you were working on your claims, so it is encompassed, how could it not be relevant to the PTO?
>
> THE WITNESS: Oh, I don't know that I did that.
>
> JUDGE ESSEX: So you don't know if you did, but for others that may have happened?
>
> THE WITNESS: Well, I can't -- I can only tell you my assumption is how surprised I would be if somebody did it or didn't do it. Obviously I didn't monitor everybody and see what they did.

(Tr. 475:25-477:7.) Also absent from the evidence are the documents that Mr. Crisp shared with Mr. Barth, documents used to create the Barth Patent claims. It is clear from Mr. Barth's testimony that these documents were relevant and should have been saved. Not only was Rambus preparing the Barth Patents for litigation, the material given to Mr. Barth was actually used to draft the claims is now gone. This is in addition to the e-mails that are admittedly destroyed, e-mails clearly relevant to the anticipated litigation.

So in the end, Mr. Barth is uncertain how it happened that the prior art from which Rambus directly obtained the information to write its claims failed to reach the PTO.

f) Dr. Steven Przybylski

Finally, before leaving the witnesses for Rambus, the ALJ would offer a few observations on Dr. Przybylski. While a written record can never capture the full dynamic of a witness on the

stand, there are instances where the cold word on paper cannot even convey the smallest sense of what goes on live. In the testimony of Dr. Steven Przybylski, we had such an experience. The doctor's testimony was inconsistent with that which he gave in the 661 Investigation, and his demeanor on the stand, as he was confronted with prior art, previous statements he and others had made, and diagrams of the evidence was remarkable: he would have long periods of silence, punctuated with heavy sighs, conveyed the impression that he had run out of answers and was making statements that he himself did not believe. He often merely disputed the words on the paper, rather than offering an explanation or argument for the court to consider. Where an expert no longer can explain apparent inconsistencies or contradictions, but merely asserts that his answer is what a person of ordinary skill in the art would give, the witness ceases to act as an expert. -. He provides no useful testimony to the ALJ or the Commission. One example of Dr. Przybylski's contradictory testimony came as he attempted to distinguish the prior art Yano device:

> Q. Dr. Przybylski, this is from your deposition taken in August of this year. 267, page 267, lines 18 through 24. "Question: The memory controller disclosed in Yano, you would agree with me is synchronous, correct?
>
> "Answer: It is. The memory controller is a part of or within microprocessor 3. It -- that is presumed to be a synchronous device."
>
> Do you remember that testimony?
>
> A. Yeah, and I think the critical word here is presumption, that there is no concrete disclosure of the nature of the memory controller but one of ordinary skill would see that there is an alignment between the activities of the memory controller and that system clock.
>
> Q. Is this accurate testimony, sir?
>
> A. Yes, it is. (Tr. 2613:19-2614:13.)

Another example:

Q. Okay. Now, with respect to the memory device, which you have been wanting to talk about here, let's talk about that for a second, okay?

A. All right.

Q. You say the memory device is asynchronous in Yano, right?

A. Yes, there is no disclosure of any clocks.

Q. And for that reason, you are offering the opinion to His Honor that Yano does not disclose sampling by the DS signal, correct?

A. The fact that the memory device of Yano is not synchronous is one aspect of the total body of evidence that would lead one of ordinary skill looking at Yano to recognize that it does not sample the data as we have defined it as being capturing at a discrete point in time.

(Tr. 2614:14-2615:7.) For the ALJ and the Commission to consider the testimony of an expert and weigh his statement versus, for example, a piece of prior art, the expert must offer more than the statement that the prior art does not mean what it says. In other instances, he is able to see things in claims that are not in the claims and to argue with the attorney without grounding his testimony in science:

Q. Now let's go to the claim language, one of the claims to get our bearing here. This is RDX-3363, claim 11, just as an illustration. This is from the '353 patent, RX-4 --or JX-4. Now, claim 11 has no limitation to synchronous memory devices, does it, sir?

A. Although the claims don't specifically recite a clock in the context of the Barth I patents, and reciting a write command, they are essentially limited to synchronous memories.

Q. Where in here is there a limitation that requires that the memory devices be synchronous? Show me the words.

A. The words write command in the context of the Barth I spec to one of ordinary skill in 1995 implies that there is going to be a synchronous capturing of one or more bits to indicate that the memory device is to perform a write operation.

(Trans 2637:2-21.) He also shapes his testimony in ways that were not consistent with his claims construction:

> Q. So it is your testimony the word write command would be interpreted by a person of ordinary skill in the art to mean this entire claim requires a clock signal and it is synchronous? That's your testimony to His Honor?
>
> A. Let me say it again. To one of ordinary skill in light of the specification and the general state of the art in 1995, would interpret write command to be the one or more bits captured synchronously to perform a write operation.
>
> Q. Did you propose a claim construction in your claim construction witness statement that write commands should be so construed, sir?
>
> A. I'm sorry, which witness statement are you referring to?
>
> Q. Your first witness statement in this investigation, in which you gave your opinions with respect to claim construction. Did you, sir, provide a formal proposed claim construction that write command should be construed in the manner that you just testified to?
>
> A. Is there a particular passage you want to refer me to or are you asking in general, do I remember doing so?
>
> Q. Let me rephrase it. You did not do that, did you?
>
> A. I don't recall doing that one way or the other right now. I could look for it if you want me to spend that time.
>
> Q. You didn't do it, did you, sir?
>
> A. I don't recall. If you want me to look and be absolutely certain, I will be happy to spend that time.

(Trans 2638:11-2639:22.) It is one thing for Rambus's fact witnesses to be unable to recall anything that occurred back when they were with the company, another entirely for their expert to not be able to recall his claim construction and what he put into it. When an expert, who is opining on whether prior art discloses the elements of the claims of the patent, cannot recall his own claim construction, his opinion regarding whether the elements of the claims are met can have no value. In effect, Dr. Przybylski does not remember the claim construction and, as such,

cannot tell if the prior art meets it or not. In the end, Dr. Przybylski discredited his own testimony to the point that it could not be relied upon. He was evasive, forgetful, contradictory and offered set statements with no explanation. The ALJ found Dr. Przybylski so unreliable overall that his testimony in this matter could not assist him.

g) Rambus's misrepresentations

In the 661 Investigation, the ALJ spent a section of the ID, and a good deal of time, highlighting that Rambus and its counsel had made a number of both misleading and irrelevant claims, such that the ALJ felt compelled to comment on them. One would hope that they would have learned their lesson, however such is not the case.

In the 661 Investigation, Rambus indicated that on its "Shred Days" it shredded numerous things, from phone books to pizza boxes:

> There were stacks of computer printouts 4-5 feet high in some places. CFF-VII.C.457. The "bulk" of materials discarded consisted of computer printouts of circuitry analyses from engineers but also included pizza boxes, phone books, old marketing material, and other "junk." (CFF.VII.C.467-471.)

(661 Investigation, Rambus's Initial Post Hearing Brief at 103.) Rather than revisit irrelevant pizza boxes and phone books in this case, Rambus, through its counsel, moved on to irrelevant employment records. (RIB at 340.) While the document Rambus cited (RX-506C) does appear on its face content neutral, it also is dealing with state and federal law on document retention on some matters (employment records and discrimination) and has no relationship to the documents and plan designed and carried out by Joel Karp, which had as its purpose: "make ourselves battle ready. [redacted] (Tr. 1916:5-7.) Mr. Karp explains further what battle ready means: "You knew that when it said make ourselves

battle ready, you have characterized that as sort of like getting prepared for a war, which could include litigation, right? A. Yes." (Tr. 1917:11-14.) While the Rambus's counsel accurately represents what is stated in the document, it is irrelevant to the document retention policy that Mr. Karp and Mr. Tate put together. In offering it as evidence to demonstrate the reasoning behind the document retention policy, it is misleading. Counsel again expended in this case an extraordinary amount of energy and time to try to distract the ALJ from the relevant evidence.

Once more, while it may be true that some of the materials shredded by Rambus in its preparation for litigation may have been irrelevant, and some of the materials may have triggered no duty to preserve them, this is not an issue that concerns this trial or the Commission. That Rambus shredded things that were not relevant to this case does not lead or assist in coming to the conclusion that they did not shred things that were, in fact, relevant to the case, and that they had a duty to preserve. This is a classic misdirection presented to the ALJ. By claiming they used their shredder to shred a "bulk" of irrelevant material, Rambus seems to wish others in the case to forget that if the shred resulted in the loss of relevant evidence, then the amount of other shredding would not matter. Page after page of the notes of Karp and others discuss destroying items such as emails because they are subject to discovery. All of the witnesses relevant to this topic admit destruction of material relevant to the case was done, including backup tapes and other sources. Whether the material was the phone books of the 661 Investigation, or the employment records of the instant case ((RX-506C) does not actually say to shred employment records, but suggests they must be kept for a longer period than some other records), Rambus's counsel's decision to mention the irrelevant shredding is itself irrelevant and presents no legitimate point. .

This was not the only example of counsel for Rambus attempting to mislead in this case. In this case, Mr. Vincent appeared and testified regarding his purging of the Barth I prosecution files at the request of Mr. Karp. Yet in spite of this, Rambus called Mr. Moniz, who began work at Rambus in September of 1999, to testify that the files had not been purged at Rambus while he had them. But he also testified they came to Rambus from Mr. Vincent after he got to Rambus. (Tr. 2266.) The issue in this case is the destruction of relevant material on certain dates that may have prevented the Respondents from preparing their defense. Rambus and their counsel knew the dates and events we were concerned about, and, yet, here is what Mr. Moniz testified to:

> Q. You don't have any firsthand knowledge of whether Rambus cleaned its own patent files before your arrival, correct?
>
> A. That's correct.
>
> Q. And you don't know if Mr. Diepenbroch cleaned patent files at Rambus, correct?
>
> A. That's correct.
>
> Q. You don't know if Mr. Karp cleaned patent files at Rambus, correct?
>
> A. That's correct.
>
> Q. You don't know if Mr. Karp told Mr. Vincent that Rambus had cleaned all of its patent files in one big event, right?
>
> A. Those are not things that I have knowledge of.
>
> Q. And you were never the party to any conversations between Joel Karp and Lester Vincent in April of 1999 when Mr. Karp asked that Blakely apply a document retention policy to Blakely's patent files, correct?
>
> A. To the extent any conversations occurred, it is correct that I was not a party.

(Trans. 2268:4-25.) Mr. Moniz provided no relevant or pertinent testimony.

D. Rambus Failed to Show Lack of Prejudice by Clear and Convincing Evidence

The Staff argues that the evidence of record in this investigation supports finding a lack of prejudice arising out of Rambus' document destruction activities irrespective of who bears the burden of proof. (SRB 54.) Rambus also argues that the Respondents were not prejudiced regardless of who bears the burden of proof. (CRB 80-81.) Respondents argue that Rambus has the burden of showing a lack of prejudice and, because Rambus failed to catalog its document destruction, it cannot show a lack of prejudice. (RIB 116.)

A finding of prejudice requires a showing that "spoliation materially affects the substantial rights of the adverse party and is prejudicial to the presentation of his case." *Micron,* 645 F.3d at 1328 (quoting *Wilson v. Volkswagon of Am., Inc.,* 561 F.2d 494, 504 (4th Cir. 1977)). The party alleging spoliation of evidence has the burden of coming forward with plausible, concrete suggestions as to what the destroyed evidence might have been. *Id.* (citing *Schmid*, 13 F.3d at 80.) However, if it is shown that the spoliator acted in bad faith, the spoliator bears the "heavy burden" of showing by clear and convincing evidence that the destroyed material was in fact inconsequential. *Id.* (citing *Anderson*, 862 F.2d at 925 ("A party who is guilty of, say, intentionally shredding documents in order to stymie the opposition , should not easily be able to excuse the misconduct by claiming that the vanished documents were of minimal import. Without the imposition of a heavy burden such as the "clear and convincing" standard, spoliators would almost certainly benefit from having destroyed documents, since the opposing party could probably muster little evidence concerning the value of papers it never saw.")

Both Rambus' and the Staff's arguments fail as neither argument presents the requisite clear and convincing evidence necessary to demonstrate that the destroyed documents were in fact inconsequential. *See Anderson*, 862 F.2d at 915. Respondents over-emphasize Rambus'

failure to catalog destroyed documents. The failure to catalog destroyed documents does not necessarily mean that a party cannot show lack of prejudice, but does weigh heavily in favor of finding that a bad faith spoliator did not meet its burden of showing clear and convincing evidence of lack of prejudice. *Micron*, 645 F.3d at 1328; *Leon v. IDX Sys. Corp.*, 464 F.3d 951, 960 (9th Cir. 2006).

The ALJ finds that Rambus failed to meet its "heavy burden" of showing a lack of prejudice. Respondents put forth several suggestions of what the destroyed evidence might have been. However, Rambus has been unable to show, by clear and convincing evidence, that there was a lack of prejudice. Rambus presents no evidence that the documents destroyed were ever cataloged. A bad faith spoliator cannot expect to benefit from destroying documents in bad faith and then claim lack of prejudice when it has no list or catalog of what was destroyed. In this situation, the presumption that the bad faith spoliator's document destruction prejudiced the Respondents is particularly strong.

Specifically, Rambus destroyed numerous emails and backup tapes. For example, Mr. Barth left behind tens of thousands of emails when he abruptly left Rambus, all of which would have been destroyed under the retention policy. (Barth, Tr. 441:11-24, 452:17-23.) Email correspondence, from Mr. Barth alone, could have provided support for Respondents' invalidity contentions. Although Rambus argues that Respondents have not shown that many of these documents ever existed or were destroyed, Rambus confuses whose burden it is to prove the existence or nonexistence of such documents. (CIB 81.) Rambus continually states that Respondents failed to make a concrete and plausible suggestion. However, due to Rambus' bad faith spoliation, Respondents' are not required to meet such a high standard, in fact, it is because of Rambus' bad faith spoliation that they cannot. (CIB 82-94.) Although witnesses testified

that they were unaware of documents questioning the patentability of the Barth Patents that were destroyed during one or more of the shred days, this does not amount to clear and convincing evidence. (*See* Hampel, Tr. 369:09-13, 372:21-373:09; CX-10767, Hampel Rebuttal Q/A 12-17; Barth, Tr. 475:09-13; Vincent, Tr. 2248:06-17.) Therefore, Rambus failed to show, by clear and convincing evidence, that its bad faith spoliation did not prejudice the Respondents.

E. Finding the Barth Patents Unenforceable is an Appropriate Sanction

Rambus argues that declaring the Barth Patents unenforceable and refusing to grant any relief on them is not warranted. (CIB 175.) According to Rambus, this case does not evidence the requisite degree of fault by Rambus or prejudice suffered by respondents. (CIB 175-177.) Rambus also argues that there is a lesser, more appropriate sanction that will avoid substantial unfairness to the Respondents. (CIB 175-79.) As to degree of fault, Rambus suggests that clear and convincing evidence of bad faith spoliation can only exist when the spoliating party failed to preserve documents while litigation is *pending*. (CIB 176) (emphasis added) As to the degree prejudice, Rambus cites several cases for its proposition that, for clear and convincing evidence of prejudice resulting from spoliation, there must be "deliberate destruction of unique, identifiable evidence bearing critical importance to the opposing party's case." (CIB 177.) Finally, Rambus argues that lesser sanctions, such as monetary damages or adverse inferences are more appropriate. (CIB 177-179.)

The Staff argues that there is a lesser degree of culpability and thus a lesser degree of prejudice than in the *Micron* and *Hynix* decisions based on the fact that the particular patent in issue was not issued until after the relevant timeframe. (SIB 104). The Staff concludes that an adverse inference would be an appropriate sanction. (SIB 105.)

Dismissal may be imposed in "particularly egregious situations" where "a party has engaged deliberately in deceptive practices that undermine the integrity of judicial proceedings" *Micron*, 645 F.3d at 1328 (quoting *Leon*, 464 F.3d at 958). In evaluating the appropriate sanction to impose for bad faith destruction of evidence relevant to a reasonably foreseeable litigation, the Federal Circuit explained:

> [T]he district court must take into account "(1) the *degree* of fault of the party who altered or destroyed the evidence; (2) the *degree* of prejudice suffered by the opposing party; and (3) *whether there is a lesser sanction* that will avoid substantial unfairness to the opposing party and, where the offending party is seriously at fault, will serve to deter such conduct by others in the future.

Micron 645 F.3d at 1329 (quoting *Schmid*, 13 F. 3d at 79) (emphasis in original).

Rambus' argument is flawed for several reasons. Contrary to Rambus' assertion, a finding of clear and convincing evidence of bad faith spoliation does not require that litigation is actually *pending*. The Federal Circuit in *Micron* required no such limitation. The Federal Circuit also does not require that the spoliation concern a single "identifiable" and "unique" piece of evidence to find prejudice as suggested by Rambus. The appropriate question in this case is whether Rambus' wholesale destruction of evidence significantly prejudiced Respondents' defenses. As Rambus never cataloged its document destruction it is unclear how Respondents could ever identify any unique piece of evidence. Furthermore, monetary sanctions in this forum are rare, and when they are imposed are usually used in discovery disputes. An adverse inference would be ineffective at this stage of the investigation and would not absolve the substantial unfairness Respondents suffer.

The Staff fails to acknowledge that the Barth Patents were always a part of Rambus' litigation plan and that Rambus drafted claims to cover competitors' products so that they could assert their patents against those same competitors. Again, the fact that the patents had not

issued at this time is not the cardinal question in this case. It is clear that Rambus intentionally destroyed documents related to the Barth Patents and that destruction prejudiced Respondents' ability to defend themselves. The fact that the Barth Patents were still in the development phase is not as critical as the Staff and Rambus assert in light of Rambus litigation plan.

The ALJ finds that holding the Barth Patents unenforceable is the most appropriate sanction in light of Rambus' destruction of documents with the intent to prejudice Respondents. In deciding the appropriate sanction, the ALJ has considered the three factors the Federal Circuit described in *Micron.*

First, Rambus' litigation campaign clearly contemplated the wholesale destruction of documents and Rambus executed this destruction in bad faith. Numerous Rambus witnesses contradicted each other and out-right lied about Rambus' document retention policy. Here, the evidence clearly shows that the Barth Patents were always a part of Rambus' long term litigation campaign and, in preparation for that campaign, Rambus destroyed documents that it knew were relevant to Respondents' defenses. The fault, in this case, clearly lies with Rambus.

Second, the degree of prejudice resulting from Rambus' spoliation is severe because the Respondents are forced to rely on "incomplete and spotty evidence." *See Anheuser-Busch, Inc. v. Natural Beverage Distribs.,* 69 F.3d 337, 348 (9th Cir.1995). The types of documents destroyed by Rambus relating to the Barth Patents, such as Mr. Barth's emails, documents Mr. Barth received regarding JEDEC, etc., would likely be "at the heart" of Respondents' invalidity defenses. *See Leon*, 464 F.3d at 960.

Finally, in light of the egregious nature of Rambus' conduct, unenforceability is the most appropriate sanction. The sanction will serve to deter such conduct by others as it will show that

one cannot enforce a patent where one's intentional document destruction prejudiced respondents.

A less drastic sanction is not useful because an adverse inference (on invalidity, for example) would leave the Respondents in the same substantially unfair position that Rambus put them in at the outset (i.e. having to prove their defenses using evidence sculpted by Rambus). An adverse inference would not help Respondents as they would be equally helpless to rebut any material that Rambus may use to overcome the adverse inference. *See Leon*, 464 F.3d at 960. Such an inference is particularly useless where the Respondents cannot obtain candid or forthright testimony from Rambus' witnesses. Respondents would be left to prove their defenses through intransigent witnesses, such as Geoff Tate, who would not even concede that his own prior sworn testimony was accurate:

> Q: Do you have any reason to think that that testimony is inaccurate?
> A: I don't have a reason to think it is inaccurate. I don't have reason to know that it is inaccurate.

Because Rambus' bad faith spoliation effectively prohibits Respondents' from challenging a rebuttal Rambus would make to an adverse inference, an adverse inference is a useless sanction in the circumstances of this case.

X. EQUITABLE ESTOPPEL

In *A.C. Aukerman*, the Federal Circuit set forth the legal standard for equitable estoppel:

> The following statement of the underlying factual elements of equitable estoppel which generally are deemed significant reflects a reasonable and fairly complete distillation from the case law:
>
> [equitable] estoppel case . . . has three important elements. [1] The actor, who usually must have knowledge of the true facts, communicates something in a misleading way, either by words, conduct or silence. [2] The other relies upon that

communication. [3] And the other would be harmed materially if the actor is later permitted to assert any claim inconsistent with his earlier conduct.

Remedies § 2.3, at 42. In other authorities, elements [2] and [3] are frequently combined into a single "detrimental reliance" requirement. See, e.g., 5 Chisum § 19.05[3], at 19-189. However, the statement of reliance and detriment as separate factors adds some clarity in this confusing area of the law.

The first element of equitable estoppel concerns the statements or conduct of the patentee which must "communicate something in a misleading way." The "something" with which this case, as well as the vast majority of equitable estoppel cases in the patent field is concerned, is that the accused infringer will not be disturbed by the plaintiff patentee in the activities in which the former is currently engaged. The patentee's conduct must have supported an inference that the patentee did not intend to press an infringement claim against the alleged infringer. It is clear, thus, that for equitable estoppel the alleged infringer cannot be unaware--as is possible under laches--of the patentee and/or its patent. The alleged infringer also must know or reasonably be able to infer that the patentee has known of the former's activities for some time. In the most common situation, the patentee specifically objects to the activities currently asserted as infringement in the suit and then does not follow up for years. In *Dwight & Lloyd Sintering*, Judge Learned Hand noted that estoppel was regularly based on "no further assurance [that a known competitor would not be sued than] the patentee's long inaction." 27 F.2d at 827. There is ample subsequent precedent that equitable estoppel may arise where, coupled with other factors, a patentee's "misleading conduct" is essentially misleading inaction. *See Hottel Corp.*, 833 F.2d at 1573-74, 4 USPQ2d at 1941, and cases cited therein. However, plaintiff's inaction must be combined with other facts respecting the relationship or contacts between the parties to give rise to the necessary inference that the claim against the defendant is abandoned. *Id.; A.C. Aukerman Co. v. Miller Formless Co.*, 693 F.2d at 701, 216 USPQ at 866; *Jensen*, 650 F.2d at 169, 207 USPQ at 819; *Continental Coatings Corp. v. Metco, Inc.*, 464 F.2d 1375, 1379-80, 174 USPQ 423, 426-427 (7th Cir. 1972).

The second element, reliance, is not a requirement of laches but is essential to equitable estoppel. *Heckler v. Community Health Svcs.*, 467 U.S. 51, 59, 81 L. Ed. 2d 42, 104 S. Ct. 2218 (1984). The accused infringer must show that, in fact, it substantially relied on the misleading conduct of the patentee in connection with taking some action. Reliance is not the same as prejudice or harm, although frequently confused. An infringer can build a plant being entirely unaware of the patent. As a result of infringement, the infringer may be unable to use the facility. Although harmed, the infringer could not show reliance on the patentee's conduct. To show reliance, the infringer must have had a relationship or communication with the plaintiff which lulls the infringer into a sense of security in going ahead with building the plant.

> Finally, the accused infringer must establish that it would be materially prejudiced if the patentee is now permitted to proceed. As with laches, the prejudice may be a change of economic position or loss of evidence. See, e.g., *Advanced Hydraulics*, 525 F.2d at 481-82, 186 USPQ at 4-5.
>
> Finally, the trial court must, even where the three elements of equitable estoppel are established, take into consideration any other evidence and facts respecting the equities of the parties in exercising its discretion and deciding whether to allow the defense of equitable estoppel to bar the suit.

A.C. Aukerman Co. v. R.L. Chaides Constr. Co., 960 F.2d 1020, 1039 (Fed. Cir. 1992).

Respondents argue that Rambus should be precluded from enforcing its patents under the doctrine of equitable estoppel and waiver based on their prior association with JEDEC. (RIB at 217-218.) Respondents argue that Rambus had a duty to disclose patents and patent applications while a member of JEDEC and/or while monitoring JEDEC activities after ceasing participation as a member. (RIB at 217-219.)

The ALJ finds Respondents' arguments unpersuasive. First, this defense has already been considered and rejected by the Federal Circuit. *See Hynix*, 645 F.3d 1336 (finding that Rambus was not equitably estopped from bringing infringement claims and did not waive right to bring infringement claims based on its duty to disclose patents and patent applications as a JEDEC member); *Infineon*, 318 F.3d 1081 (finding that substantial evidence did not exist to support Infineon's fraud claim based on Rambus's duty to disclose patents and patent applications as a JEDEC member); *see also Rambus v. Fed. Trade Comm'n*, 522 F.3d 456 (D.C. Cir. 2008) (finding the evidence of record failed to show exclusory conduct based on Rambus's duty to disclose patents and patent applications as a JEDEC member). Respondents have failed to present any new evidence that would change the analysis set forth in those appellate opinions. As such, the ALJ finds that Respondents have failed to show by clear and convincing evidence that Rambus should be equitably estopped from enforcing its patents and waived its right to bring infringement claims.

The evidence fails to show that Rambus violated JEDEC's patent disclosure policies. The Federal Circuit explained in *Infineon*:

> Rambus's duty to disclose extended only to claims in patents or applications that reasonably might be necessary to practice the standard. In other words, this duty encompassed any patent or application with claims that a competitor or other JEDEC member reasonably would construe to cover the standardized technology. This does not require a formal infringement analysis. Members are not required to perform a limitation-by-limitation comparison or conduct an equivalents analysis. Rather, the disclosure duty operates when a reasonable competitor would not expect to practice the standard without a license under the undisclosed claims. Stated another way, there must be some reasonable expectation that a license is needed to implement the standard. By the same token, the disclosure duty does not arise for a claim that recites individual limitations directed to a feature of the JEDEC standard as long as that claim also includes limitations not needed to practice the standard. This is so because the claim could not reasonably be read to cover the standard or require a license to practice the standard.

Infineon, 318 F.3d at 1100-01.

Respondents failed to show that a license to the Barth Patents was needed to implement a standard that had issued or was under formal consideration by JEDEC in the relevant timeframe. Respondents argue that the "overlapping subject matter [in the '292 Application] and Rambus' membership [in JEDEC]" and Rambus's failure to disclose the application are a sufficient basis for finding equitable estoppel and waiver.[30] (RIB at 217-219.) This argument fails under the Federal Circuit's analysis in *Infineon* for the following reasons.

First, since JEDEC's policies at the time did not require disclosure of "a member's intentions to file or amend patent applications" (*Infineon*, 318 F.3d at 1102), the relevant inquiry focuses on Complainant's then pending *claims*, *e.g.*, *claims* from the '292 Application .

Second, Respondents failed to address whether the claims from the '292 Application *also include limitations not needed to practice the standard.* Respondents must demonstrate a

[30] The '292 Application "describes specific technologies that were under discussion at JEDEC at the time when Rambus was a member." (RIB at 218.)

reasonable expectation that a then pending claim, *in its entirety*, was necessary to practice the JEDEC standard. *Infineon*, 318 F.3d at 1101 ("[T]he disclosure duty does not arise for a claim that recites individual limitations directed to a feature of the JEDEC standard as long as that claim also includes limitations not needed to practice the standard."). Respondents only allege that the '292 Application covers overlapping subject matter. However, the mere existence of some overlap between pending claims and features in a JEDEC standard was not enough to trigger JEDEC's disclosure duty under the Federal Circuit's analysis. "To hold otherwise would . . . render the JEDEC disclosure duty unbounded." *Id.*

In addition to its failure on substantive grounds, the ALJ finds that Respondents have failed to meet their burden of showing this defense by clear and convincing evidence. The entire defense consists of a little over a single page of argument. While the specific number of pages is not dispositive, it is certainly indicative as to how Respondents have clearly not met their burden of clear and convincing evidence.

Therefore, the ALJ finds that Respondents have failed to show by clear and convincing evidence that Rambus is equitably estopped from bringing infringement claims and waived its right to bring infringement claims based on its duty to disclose patents and patent applications as a JEDEC member.

XI. PRECLUSION FROM SEEKING INJUNCTIVE RELIEF

According to the Respondents, a Rambus predecessor-in-interest to the Dally patents participated in a standard setting organization ("SSO") called Peripheral Component Interconnect Special Interest Group ("PCI-SIG") and thereby subjected these patents to certain licensing obligations under the PCI-SIG bylaws. (*See* RIB at 260-270; RX-2407C.004.)

More specifically, the Respondents' defense is premised on their view that the SSO that promulgated the PCI Express standard, *i.e.*, one of the interface technologies allegedly covered by the asserted Dally patent claims, required members to license on FRAND (Fair Reasonable And Non-Discriminatory) terms "Necessary Claims" covering various aspects of the PCI Express standard. The Respondents argue that a Rambus predecessor-in-interest to the Dally patents was a member of the SSO that adopted PCI Express, and that the Dally patents are therefore subject to the SSO's FRAND obligations. (*See* RIB at 261-264.) According to the Respondents, these FRAND obligations prevent Rambus from seeking injunctive relief in any forum, including at the Commission, which can only provide relief in the form of exclusion orders and cease and desist orders. (*See* RIB at 264-270.)

The ALJ finds that this defense is without merit because the Dally patents do not come within the scope of the FRAND obligation of PCI-SIG. The ALJ does not reach the question of whether such an obligation would bar relief before the Commission.

Two sections of the PCI-SIG bylaws are dispositive as to this defense. Section 15.3 on its face requires PCI-SIG members to grant other members and their affiliates a license to "Necessary Claims" on FRAND terms. (*See* RX-4653C, Bylaws of PCI-SIG at § 15.3.) Section 15.1 defines the "Necessary Claims" as follows:

> **"Necessary Claims"** means those claims of all patents and patent applications ... throughout the world which a Member or its Affiliates has the right, any time during the term of this Agreement, to grant licenses of the nature agreed to be granted herein without such grant resulting in payment of royalties or other consideration to third parties (except for payments to Affiliates or employees).

See id. at §15.1 (bold in original, underlining added for emphasis). Thus, patent claims where the grant of FRAND license would "result[] in payment of royalties or other consideration to third parties" are outside the scope of the FRAND obligation. The key dispute between the parties is whether Rambus's payment of royalties or other consideration to third party MIT

exempts the asserted Dally patent claims from the "Necessary Claims" definition in Section 15.1 above.

Respondents are of the view that Section 15.1 distinguishes between two types of third-party payment approaches, only one of which is exempted from the FRAND obligations in Section 15.3. (RRB at 130-132.) In the first approach, which the Respondents call a "grant-based fee" arrangement, a prospective licensee member pays an exclusive licensee, who in turn pays a sublicensing fee to the patent holder. (*See* RRB at 130-132.) According to the Respondents, this first approach is exempt from the FRAND obligations in Section 15.3. In the second approach, which the Respondents call a revenue sharing arrangement, a prospective licensee member pays royalties to *both* an exclusive licensee *and* the patent holder. *See id.* According to the Respondents, this second scheme is *not* exempt from the FRAND obligations in Section 15.3. *See id.* The ALJ agrees with Staff that the only apparent distinctions between the two schemes appear to be *who* is ultimately paying the patent holder and *whether* the payment is called a "royalty" or a "sublicensing fee." (SIB at 199.)

The Dally patents are assigned to MIT. (CIB at 273.) In November 1999, MIT licensed the Dally patents to Chip2Chip, Inc. (CX-4012C.) Chip2Chip, Inc. became Velio Communications. (CIB at 274.) Velio subsequently assigned the MIT/Chip2Chip agreement to Rambus in 2003. (CX-4013C; *see also*, CX-4014C, CX-4015C.) Rambus and MIT also entered into an Amended and Restated Exclusive Patent License Agreement on November 29, 2010. (CX-4016C.)

The Dally patent licenses require payment to MIT for any further licensing or sublicensing. (CX-4012C; CX-4016C.) Under the Exclusive Patent License Agreement between Chip2Chip and MIT, Chip2Chip/Velio (the "COMPANY") was required to pay

royalties to MIT:

(CX-4012C at 7.) Chip2Chip/Velio had to pay a "Running Royalty" on the income associated with the sale or license of the design cores. (*Id.*) Chip2Chip/Velio further had to share sublicense income for licensing of the patent rights:

(*Id.* at 8.) Rambus has been under the same restriction regarding payment of royalties to MIT. (CX-4014C; CX-4015C.) The Amended and Restated Exclusive Patent License Agreement that MIT and Rambus entered into on November 29, 2010, also requires Rambus to pay MIT a portion of any Dally-related sublicense income. (CX-4016C.) Rambus has paid royalties to MIT based on such sublicensing income that it has received. (CX-7586C.0009-11.)

The ALJ finds that Rambus unquestionably has an obligation to pay royalties or other consideration to MIT and thus the Dally patents cannot be "Necessary Claims." MIT is not Rambus's Affiliate as it has never controlled, or been controlled by, Rambus. (CX-6418C.0001.) Nor is MIT Rambus's employee. (CIB at 276.) And MIT was not an Affiliate or employee of Velio. (CIB at 276.) Thus, MIT is a third-party to both Rambus and Velio. (CIB at 276.) And both Velio's and Rambus's agreement with MIT have required royalty payments to MIT. (CIB at 276.) Neither Velio nor Rambus could license the Dally patents "without such grant resulting in payment of royalties or other consideration to" MIT. Thus, any license under the Dally

patents has always required a payment of royalties to MIT. The Dally patent claims were not, and are not, "Necessary Claims."

Respondents nevertheless argue that the Rambus-MIT arrangement is of the second, non-exempt type, because Rambus's predecessor-in-interest (which had the right to sublicense the Dally patents) and MIT (the patent holder of record with the USPTO), were to share in any subsequent amounts collected from prospective licensees. (*See* RRB at 130-131.) The ALJ finds that this argument is inconsistent with the plain language of the PCI-SIG bylaws – which do *not* distinguish between "grant-based fee" arrangements and "revenue sharing" arrangements.

Respondents rely heavily on the fact that [redacted] The ALJ finds that such extrinsic evidence is irrelevant because the language in Section 15.1 is clear and unambiguous on its face. *See Certain Coamoxiclav Products, Potassium Clavulanate Products, and other Products Derived From Clavulanic Acid*, Inv. No. 337-TA-479, Order No. 7 (March 6, 2003) ("[T]he administrative law judge finds that the Settlement Agreement, insofar as it relates to whether or not complainants have relinquished their trade secret allegation and whether or not complainants can state a claim for conversion is unambiguous on its face, and therefore the use of extrinsic evidence in interpreting the document is unnecessary and inappropriate."); *Certain Personal Computers With Memory Management Information Stored in External Memory and Related Materials*, Inv. No. 337-TA-352, Order No. 25 (June 6, 1994) ("As a matter of law, the Intel-ST

agreement is unambiguous; therefore, no extrinsic evidence regarding the intent of the parties is admissible.").

Respondents also argue that Rambus should be precluded from seeking injunctive relief for the Barth Patents for the same reasons, namely Rambus's agreement that it would accept specified royalties for memory controllers covered by its patents to resolve a European Commission investigation. (RIB at 270.) As set forth *supra*, the ALJ finds that Rambus is not precluded from seeking injunctive relief.

XII. STANDING

A. Applicable Law

To assert a patent at the Commission, the complainant must own the patent or hold certain exclusive rights thereto. See Certain Point of Sale Terminals, Inv. No. 337-TA-524, Order No. 31 (February 7, 2005). The Commission Rules require complainants to demonstrate standing upon filing of the complaint by "showing that at least one complainant is the owner or exclusive licensee of the subject intellectual property." See 19 C.F.R. § 210.12(a)(7). In addition, complainants must provide a certified copy of the assignments of each patent as well as a copy of any license agreement relied upon to establish standing to bring the complaint. See 19 C.F.R. § 210.12(a)(9)(ii)-(iv). While respondents may raise standing as a defense in their answer to the complaint, the question of whether a party lacks standing can be raised sua sponte and cannot be waived. Pandrol USA, LP v. Airboss Ry. Prods., Inc., 320 F.3d 1354, 1368 (Fed. Cir. 2003) (internal citation omitted) ("It is well-established that any party, and even the court sua sponte, can raise the issue of standing for the first time at any stage of the litigation, including on appeal.").

B. Factual Background

The parties agree that the named inventor, Dr. William Dally assigned the parent patent application of the Dally patents and all subsequent applications and related patents to the Massachusetts Institute of Technology (MIT), where he was a Professor at the time, and that assignment was recorded at the U.S.P.T.O. on October 27, 1997 at reel 8759, frames 202-04. (CX-4008.) On November 1, 1999, MIT exclusively licensed the Dally Patents to Chip2Chip Inc., later renamed Velio Communications, Inc. (Velio). (CX-4012C.) Velio assigned the agreement to Rambus in December 2003. (CX-4013C.) Effective November 29, 2010, Rambus obtained all substantial rights in the Dally patents. (CX-4016C.0003.)

DARPA awarded Dr. Dally and MIT a contract in August 1996 pursuant to a research proposal submitted by Dr. Dally. (CX-6288C.) Based on a purchase order covering the period starting September 31, 1996, MIT entered into a subcontract with University of North Carolina - Chapel Hill (UNC), naming Dr. John Poulton as Key Personnel. (RX-2023C.) Article 1 of the UNC subcontract identifies the "Statement of Work." (RX-2023C.0001.) Specifically it states that UNC "shall provide research relating to the subject entitled 'Equalized 4Gb/s CMOs Signaling' under DARPA contract No. DABT63-96-C0039." (RX-2023C.0001.)

Article 10 of the UNC subcontract states:

> All rights, title and interests to all inventions, copyrightable materials, computer software, semiconductor maskworks, tangible research property and trademarks ("Intellectual Property") conceived, invented, authorized or reduced to practice, either solely or jointly with others which are developed under this subcontract in the course of or pursuant to sponsored research shall vest in [UNC].

(RX-2023C.0007-08.)

The ALJ finds that Article 10 is clear in addressing Intellectual Property "developed under this subcontract." (RX-2023C.0007-08.) The ALJ finds that although work on reducing the Dally inventions to practice occurred at UNC, that the Dally patents were not developed

under the UNC subcontract but was developed solely by Dr. Dally. Consistent with the MIT/DARPA contract and the UNC subcontract, the Dally inventions were assigned to MIT while the separate inventions of UNC, developed under the subcontract, were assigned to UNC.

Respondents argue to the contrary that Article 10's "developed under" requirement subsumes intellectual property "conceived, invented, authorized or reduced to practice." (See RIB at 105; Tr. 2099:20-2100:9.) However, the ALJ finds that the plain language of Article 10 includes a separate requirement that the intellectual property covered by this clause must be developed under the subcontract distinct from other activities. (RX-2023.0008.) As discussed below, the evidence demonstrates that the Dally inventions were developed before the UNC subcontract, and thus, they were not developed under it. Therefore, Article 10 of the subcontract does not apply.

The ALJ notes that John Poulton, identified as UNC's "key personnel" in the subcontract, confirmed that Dally had already developed the inventions disclosed in the Dally patents before the UNC subcontract was entered into. Specifically, he testified that Dally approached him about the ideas embodied in the Dally patents in the Fall of 1995, a year before the UNC subcontract was executed. (Tr. 1716:17-22; see also JX-99C at 30:20-31:6.) Poulton further testified that, at that time, the idea was "pretty much fully formed by Bill [Dally]," and he believed Dally had simulations showing that the idea would work. (JX-99C.0012 at 32:13-18, 33:9-13.) Poulton "had no doubt that it was a great idea" that it "was going to solve a very serious problem." (Tr. 1716:21-1720:9.) Dally memorialized these ideas in June 1996 notes and later provided these notes to Poulton. Dally also described the inventions in the August 1996 Hot Interconnects paper. (CX-6324; RX-2015.) Poulton confirmed that the subject matter of the Dally patent application, as described in the Hot Interconnects paper, was solely Dally's

invention. (Tr. 1732:15-1733:5 (referring to RX-2015.0002).) Dally likewise testified that the transmitter in the Hot Interconnects paper was his. (JX-0032C at 102:18-22.) Thus, it is irrelevant that the Fast Links chip was the actual reduction to practice because the invention was not developed under the sub-contract.

Respondents also argue that because the Final Technical Report identifies the Dally inventions and the separate Poulton inventions, this means that the Dally inventions were developed under the UNC subcontract. (RIB 106-107.) But the Final Technical Report addresses the DARPA contract, not just the UNC subcontract. (RX-2018C.0001.) Discussing the Dally inventions, the report says that "a pending U.S. Patent (assigned to MIT) that covers this technology." (RX-2018C.0002.) The ALJ finds that, contrary to Respondents' argument, this Final Technical Report does not give any indication that the Dally inventions were developed under the subcontract. Instead, it confirms MIT's rightful ownership.

The language of the subcontract supports that conclusion. Article 10, the only provision Respondents rely on, states that "inventions . . . conceived, invented, authorized or reduced to practice, either solely or Jointly with others which are developed under this Subcontract in the course of or pursuant to sponsored research shall vest in Subcontractor." RX-2891.007-08 (emphasis added). According to the plain language, this provision only applies to inventions developed under the subcontract. Since the Dally inventions were developed earlier, the inventions are not subject to Article 10.

Finally, the conduct of UNC and MIT made clear that UNC thought it owned Dr. Poulton's inventions developed under the subcontract, while MIT owned Dr. Dally's inventions. For example, when UNC submitted "Reports of Invention," it provided data on the "Multi-wire Signaling" invention. UNC provided no information on the Dally inventions. (See CX-7650C;

CX-7660C.) UNC and MIT separately patented the inventions they developed and UNC never sought to patent the Dally inventions based on any reduction to practice work done at UNC.

Tim Quigg, an employee of UNC who testified at the hearing, refused to say that UNC owns the Dally patents. (Tr. 2116.) Moreover, under the subcontract, UNC was required to submit to MIT a "final patent report indicating whether any inventions or discoveries were conceived in the course of effort under this contract." (RX-2023C.0008-9.) UNC never did. (Tr. 2114.) This behavior is completely consistent with what the ALJ believes to be the correct reading of Article X.

Accordingly, the ALJ finds that Respondents have failed to establish that UNC has any rights in the Dally patents. Respondents offer no other challenge to MIT and Rambus's chain of title. Thus, the ALJ finds that Rambus has standing to assert the Dally patents.

XIII. PATENT EXHAUSTION

A. Applicable Law

The doctrine of patent exhaustion provides that the initial authorized sale of a patented item in the United States terminates all patent rights to that item. *See Quanta Computer, Inc. v. LG Electronics, Inc.*, 128 S. Ct. 2109, 2115 (2008) ("*Quanta*"). More specifically, patent exhaustion may apply to the authorized sale of a component comprising part of a patented system or product when the following elements are present: (1) the component "substantially embodies" the patented invention; and (2) the sale of such component was authorized. *Id.* at 2113. With respect to the first part of the test, the Court explained in *Quanta* that a component "substantially embodies" the patented invention where (1) the component's only reasonable and intended use is to practice the patented invention; and (2) the component embodies essential features of the patented invention. *Id.* at 2119. With respect to the second part of the test, the

Court explained in *Quanta* that an agreement broadly permitting a manufacturer to "make, use, or sell" products free of the patent-holder's claims constitutes authorization to sell its products to downstream customers. *Id.* at 2122. However, the sale must take place *within the United States* to trigger patent exhaustion. *See Jazz Photo Corp. v. U.S. Int'l Trade Comm'n*, 264 F.3d 1094, 1105 (Fed. Cir. 2001) ("*Jazz*"); *see also Minebea Co. Ltd. v. Georg Papst*, 44 F.Supp. 2d 68, 137, 139 (D.D.C. 2006) ("*Minebea*") (citing *Jazz*, 264 F.3d at 1105).

Numerous district court and appellate opinions have addressed whether a sale is an "authorized" sale "within the United States" for purposes of a patent exhaustion analysis. In one such case, a district court held that the sale of a product delivered abroad *cannot* constitute an authorized first sale for patent exhaustion purposes even when price negotiations were conducted in the United States and payments were made in the United States. *Minebea*, 44 F. Supp. 2d at 141-44. According to the Court, an authorized foreign sale can never occur under a U.S. patent because the U.S. patent's territorial reach is only as far as the U.S. borders. *See id.* at 141.

More recently, the Federal Circuit addressed exhaustion in the context of toll-collection systems purchased by the Illinois State Toll Highway Authority (ISTHA) from a company called Mark IV. *See TransCore, L.P. v. Electronic Transaction Consultants Corp.*, 563 F.3d 1271, 1273 (Fed. Cir. 2009) ("*TransCore*"). In that case, the parties disputed the extent to which a prior covenant not to sue between TransCore and Mark IV exhausted TransCore's rights in the patents-at-issue.[31] Analogizing covenants not to sue with license agreements, the Court found

[31] *See TranCore*, 563 F.3d at 1277 ("The only issue relevant to patent exhaustion is whether Mark IV's sales were authorized, not whether TransCore and Mark IV intended, expressly or impliedly, for the covenant to extend to Mark IV's customers.").

that Mark IV was in fact authorized to sell its products under the relevant agreement.[32] Because the parties also disputed whether the "sale" took place in the United States or abroad, the Court then turned to an examination of territoriality:

> Although the parties do not agree about which Mark IV entity actually sold the toll collection products--the irrevocable offer was made by Mark IV US, but the purchase order was placed with (and the order was ultimately filled by) Mark IV Canada--there is no dispute that a Mark IV entity was responsible for the sale.
>
> Moreover, there is no dispute that the toll collection products were sold and shipped to ISTHA. Even if we accept TransCore's assertions that the products were shipped from Canada, this does not alter the essential fact that the transaction as a whole ultimately occurred "to" the United States. *See Litecubes, LLC v. N. Light Prods.*, 523 F.3d 1353, 1369-71 (Fed. Cir. 2008) (finding that a sale 'to' the United States is sufficient to support infringement liability).

Id. at 1278. The Court thus considered the "transaction as a whole" in determining a sale took place in the United States.

In *Fujifilm*, the Federal Circuit addressed exhaustion in the context of single-use cameras that were being refurbished and resold as new. *See Fujifilm Corp. v. Benum*, 605 F.3d 1366, 1368 (Fed. Cir. 2010) ("*Fujifilm*"). More specifically, the parties disputed "whether *Quanta* . . . eliminated the territoriality requirement for patent exhaustion announced in *Jazz Photo Corp. v. United States International Trade Commission*, 264 F.3d 1094 (Fed. Cir. 2001) . . . ." *Id.* at 1370. The Court held that it did not.[33] Because the parties also disputed whether the "sale" took place

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[32] *See TranCore*, 563 F.3d at 1276 ("The real question . . . is not whether an agreement is framed in terms of a 'covenant not to sue' or a 'license.' That difference is only one of form, not substance--both are properly viewed as 'authorizations.' Rather, the pertinent question here is not whether but what the TransCor-Mark IV settlement agreement authorizes. More specifically, does the TransCore-Mark IV settlement agreement authorize *sales*? We conclude that it does.") (emphasis in original).

[33] *See Fujifilm*, 605 F.3d at 1371 ("*Quanta Computer, Inc. v. LG Electronics, Inc.* did not eliminate the first sale rule's territoriality requirement.").

in the United States or abroad, the Court then turned to the evidence of sales in the United States and abroad:

> Defendants' remaining arguments are unconvincing. The district court correctly relied on three fact witness reports and a statistical expert to show that *imported LFFPs included shells that were not first sold in the United States*, and not redesigned. Therefore, the court did not abuse its discretion in finding contempt of the preliminary injunction.

Id. at 1373 (emphasis added).

In another case, the Federal Circuit addressed exhaustion in the context of semiconductor packages purchased from multiple suppliers that had taken a license to the patents-at-issue. *See Tessera, Inc. v. Int'l Trade Comm'n*, 646 F.3d 1357, 1362 (Fed. Cir. May 23, 2011) ("*Tessera*"). In that case, the parties disputed the extent to which a licensee's dilatory royalty payments should impact the Commission's finding that the licensee's sales were nonetheless "authorized" by Tessera.[34] The Court agreed with the Commission:

> The proper focus is on whether the sales were authorized. Tessera overlooks important aspects of the structure of its TCC Licenses. These agreements expressly authorize licensees to sell the licensed products and to pay up at the end of the reporting period. Thus, in these agreements, Tessera authorizes its licensees to sell the licensed products on credit and pay later. That some licensees subsequently renege or fall behind on their royalty payments does not convert a once authorized sale into a non-authorized sale. Any subsequent non-payment of royalty obligations arising under the TCC Licenses would give rise to a dispute with Tessera's licensees, not with its licensees' customers.

Id. at 1370. In this regard, it bears noting that the Court did not address *where* the relevant sales took place because the parties did not seek appellate review on that issue. Thus, *Tessera* does not provide guidance on application of the territoriality requirement for patent exhaustion.

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[34] *See Tessera*, 646 F.3d at 1369 ("Because royalties were not paid or were paid late by some licensees, Tessera asserts that sales by those licensees did not trigger exhaustion of its patent rights.").

Finally, the Commission addressed a patent exhaustion defense raised by nVidia in the 661 Investigation with respect to its alleged use of licensed Samsung memory devices based on the same Samsung license agreement relied upon by the Exhaustion Respondents in this investigation. Due to the timing of Rambus's license with Samsung (entered into just days before issuance of the 661 ID), the effects of that license were presented to the Commission after the close of proceedings before the Judge.[35] The Commission nonetheless determined to address the issue of the Samsung license, and invited briefing from each party on the effect, if any, of the Samsung license. nVidia relied on *Quanta*, and argued that Samsung's memory products "substantially embody the asserted claims of the Barth I Patents."[36] However, nVidia's briefs failed to address whether the alleged exhausting sales occurred in the United States or abroad. After the Federal Circuit issued its *Fujifilm* decision, the Commission sought additional briefing from the parties on the effect of *Fujifilm*. Rambus provided evidence that Samsung memory was sold overseas to nVidia, while nVidia failed to provide any evidence to suggest the sales occurred in the United States.[37] On that basis, the Commission found that nVidia had not established exhaustion with respect to any of its accused products.[38]

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35 *See Certain Semiconductor Chips Having Synchronous Dynamic Random Access Memory Controllers and Products Containing Same*, Inv. No. 337-TA-661, Respondents' Petition for Review of Initial Determination on Violation of Section 337 and Recommended Determination on Remedy and Bond, EDIS Doc. ID 418745 at 90-91 (Feb. 12, 2010).

36 *See Certain Semiconductor Chips Having Synchronous Dynamic Random Access Memory Controllers and Products Containing Same*, Inv. No. 337-TA-661, Respondents' Supplemental Brief Regarding Patent Exhaustion, EDIS Doc. ID 427026 at 17 (June 7, 2010).

37 *See Certain Semiconductor Chips Having Synchronous Dynamic Random Access Memory Controllers and Products Containing Same*, Inv. No. 337-TA-661, Complainant Rambus's Response to the June 22, 2010 Notice of the Commission, EDIS Doc. ID 428148 at 3-5 (June 25, 2010).

38 *See* 661 Comm'n Op. at 17 ("[W]e find that Respondents have failed to demonstrate that Rambus has exhausted its patent rights with respect to accused products that incorporate Samsung memory. Specifically, Respondents have failed to demonstrate that the relevant sales of Samsung memory take place in the United States.").

Respondents argue that Rambus has exhausted its rights in the Barth Patents based on the authorized sale of Samsung and Elpida DRAM memory devices in certain of Respondents' accused products. (RIB at 270-271.) Those respondents are Cisco and [redacted] -- no other Respondents have claimed to have purchased memory devices from Samsung and/or Elpida.[39]

B. Accused Product "Substantially Embody" The Patented Invention

Respondents and Staff argue that the Samsung/Elpida memory devices "substantially embody" the patented invention. (RIB at 274-275; SIB at 127-128.) Rambus argues that the Samsung/Elpida memory devices do not "substantially embody" the asserted claims of the Barth Patents because the Barth Patents are not directed at memory devices. (CIB at 126-127.) However, as set forth *supra* in Section VI.B, the ALJ found that the asserted claims of the Barth Patents did not exclude memory devices. Thus, for those same reasons, Rambus's argument fails here.

Furthermore, a significant portion of the infringement evidence identified by Rambus in its brief consists of evidence from the perspective of a memory device – *e.g.*, datasheets and JEDEC standards that show JEDEC-complaint memory devices must be controlled in an infringing manner as to the asserted '353 and '109 Patents. Therefore, the ALJ finds that the Samsung/Elpida memory devices substantially embody the Barth Patents.

C. Authorized Sale in the United States

Respondents argue that the Samsung/Elpida memory devices were authorized sales that meet the territoriality requirements of patent exhaustion and, further, that Rambus's [redacted]

[39] Respondents Broadcom and Motorola had also asserted this defense, but these two respondents have since been terminated from the investigation or are in the process of being terminated. (*See* Order No. 60 (terminating Broadcom from the investigation on the basis of settlement agreement; *see Joint Motion to Partially Terminate Investigation on the Basis of Settlement Agreement* (Motion Docket No. 753-106) filed on February 28, 2012 (as of the date of this Final Initial Determination, responses to the joint motion were still outstanding).)

licenses meet the territoriality requirement. (RIB at 275-278.) Staff agrees that the sales to respondent [redacted] satisfy the territoriality requirement but that the sales to respondent Cisco fail to meet the requirement. (SIB at 128-131.)

Rambus argues that Cisco and [redacted] have failed to show that the allegedly exhausting sale occurred in the United States. (CRB at 60-61.) Specifically, with regard to [redacted], Rambus argues that [redacted] has failed to show that the [redacted] (CRB at 61.) Rambus further argues that the sales are not "authorized" because the Samsung/Elpida license is limited to DRAM patent claims and do not include the memory controller claims of the Barth Patents. (CIB at 128.)

The ALJ finds the evidence shows that Samsung and Elpida *are authorized to sell* JEDEC-complaint memory devices under the '353 and '109 Patents. However, the evidence shows that only sales to [redacted] take place in the United States.

The evidence shows that the agreements at issue here appear to broadly grant Samsung/Elpida the right to [redacted]. (RX-4079C, Samsung Agreement at § 2.1(a).) The agreements define "Rambus Applicable Patent Claims" as [redacted]

1.45 [redacted]

1.46 [redacted]"

1.47 "[redacted]

[redacted]

(CX-4339C.0008; *see also* RX-4075C.0013 (substantially similar definitions). EDEC requires that such devices be "used" in an infringing manner by dictating the control methodology that must be used to properly interface with a JEDEC-compliant memory device. For at least these reasons, the Samsung/Elpida agreements grant those companies a license to [redacted] per the express definition of "Rambus Applicable Patent Claims." Therefore, the ALJ finds that Samsung and Elpida were authorized to [redacted].

Nevertheless, despite being authorized to sell the license memory devices, only [redacted] was able to show that its sales satisfied the territoriality requirement. Cisco was unable to satisfy this requirement and, therefore, failed to show that patent exhaustion applied to its products. *See TransCore*, 563 F.3d at 1278.

The evidence shows that the relevant sales of JEDEC-complaint memory devices from Samsung to [redacted] take place in the United States. [redacted] at Q/A 128-132; [redacted] Specifically, the evidence shows that the relevant memory devices [redacted] *See TransCore, L.P. v. Electronic Transaction Consultants Corp.*, 563 F.3d 1271, 1278 (Fed. Cir. 2009) (finding evidence as to shipment of the licensed component relevant to determining whether the sale took place in the United States for purposes of an exhaustion defense). Rambus argues that because they were [redacted]. The ALJ finds Rambus's argument unpersuasive. The evidence shows that the authorized sale was in the United States. [redacted]

[redacted] does not alter the fact that the authorized sale occurred in the United States. Furthermore, the ALJ finds that the fact that [redacted] also does not alter the fact that the authorized sale occurred in the United States. Therefore, the evidence shows some authorized sales in the United States to [redacted].

However, the ALJ finds that Cisco has failed to show that its authorized sale took place in the United States. None of the evidence cited by Cisco provides any information as to where the authorized sale took place. The cited testimony simply addresses the relative value of memory controllers in Cisco's products. (*See* RX-6290C, Vander Veen Rebuttal Q&A 66-67.) Further, the interrogatory responses Cisco seeks to rely on are to a large extent irrelevant as they discuss whether Cisco products include Samsung memory, not *where* the relevant sales to Cisco take place. Thus, the evidence does not show authorized sales in the United States to Cisco.

As for Respondents' remaining arguments, the ALJ finds them unpersuasive. Respondents argue that Rambus' [redacted] license grants to Samsung and Elpida provide an independent basis to find the territorial requirement is met. (RIB at 276.) As Staff and Rambus correctly noted, these arguments are contrary to the precedent discussed above in the legal standards section, and should therefore be rejected. Specifically, Respondents' argument, however, is contrary to *Fujifilm*. *See* 605 F.3d at 1371. In *Fujifilm*, the Federal Circuit rejected the defendants' argument that *Quanta* "created a rule of 'strict exhaustion,'" stating that *Quanta* "did not eliminate the first sale rule's territoriality requirement." *Id.* Moreover, because the *Fujifilm* court made no distinction between sales by Fujifilm with worldwide rights and sales by a licensee, Respondents have no basis for asserting that sales by a third-party licensee satisfy the exhaustion doctrine without regard to the territoriality requirement.

Therefore, the ALJ finds that Garmin has shown that certain of [redacted] products that contain the licensed Samsung/Elpida memory devices are subject to patent exhaustion. The ALJ finds that the doctrine fails to apply to the other remaining Respondents and to [redacted] other products that do not incorporate the Samsung/Elpida memory devices.

XIV. PATENT MISUSE

Patent misuse is an equitable defense to patent infringement. *See U.S. Philips Corp. v. Int'l Trade Comm'n*, 424 F.3d 1179, 1184 (Fed. Cir. 2005). It "arose to restrain practices that did not in themselves violate any law, but that drew anticompetitive strength from the patent right, and thus were deemed contrary to public policy." *Mallinckrodt, Inc. v. Medipart, Inc.*, 976 F.2d 700, 704 (Fed. Cir. 1992). The doctrine has a "narrow scope," and "[g]iven that the patent grant entitles the patentee to impose a broad range of conditions in licensing the right to practice the patent, the doctrine of patent misuse 'has largely been confined to a handful of specific practices by which the patentee seemed to be trying to extend his patent grant beyond its statutory limits.'" *Princo Corp. v. Int'l Trade Comm'n*, 616 F.3d 1318, 1329 (Fed. Cir. 2010) (en banc) (quoting *USM Corp. v. SMS Tech., Inc.*, 694 F.2d 505, 510 (7th Cir. 1982)). "[T]he key inquiry under the patent misuse doctrine is whether by imposing the condition in question, the patentee has impermissibly broadened the physical or temporal scope of the patent grant and has done so in a manner that has anticompetitive effects." *Princo*, 616 F.3d at 1328. If the licensing restrictions in question are "reasonably within the patent grant, the patent misuse defense can never succeed." *Monsanto Co. v. McFarling*, 363 F.3d 1336, 1341 (Fed. Cir. 2004) (quotation marks omitted). "[T]he essence of a patent grant is the right to exclude others from profiting by the patented invention." *Dawson Chem. Co. v. Rohm & Haas Co.*, 448 U.S. 176, 215 (1980); *see also Zenith Radio Corp. v. Hazeltine Research, Inc.*, 395 U.S. 100, 135 (1969)

("The heart of (the patentee's) legal monopoly is the right to invoke the State's power to prevent others from utilizing the State's power to prevent others from utilizing his discovery without his consent.").

Respondents argue that Rambus is committing patent misuse by naming downstream customers of memory controllers as Respondents. (RIB at 278-279.) Specifically, Respondents allege that Rambus's actions are in direct violation of its resolution of antitrust claims before the European Commission. (See RX-6272 at ¶ 64 (European Commission Decision dated September 12, 2009), ("Rambus clarified that it intends to collect royalties on the individual device, such as a DRAM or a Memory Controller from the manufacturer and commits not to seek royalties for the same device from the manufacturer's customer."); RX-4855-4857.) Respondents contend that despite this commitment, Rambus has named twenty customers in this investigation on the sole basis that they allegedly important or sell of downstream products containing accused memory controllers and that this action is a violation of Rambus's commitment to the European Commission.

There is no merit to this argument. Respondents cite no cases that hold that commitments to foreign governmental institutions can give rise to patent misuse in the United States. Setting that aside for a moment, Respondents have failed to demonstrate how Rambus has violated its commitment to the European Commission. There is absolutely no evidence that Rambus is seeking royalties from the customer respondents. The ALJ notes that the law requires Rambus to name the various downstream customers as respondents if it wishes to obtain relief against downstream products incorporating the allegedly infringing components. *See Kyocera Wireless Corp. v. Int'l Trade Comm'n*, 545 F.3d 1340 (Fed. Cir. 2008). Given this legal requirement, Rambus's naming of downstream respondents in this investigation does not establish that they

have violated their commitment to the European Commission to not seek royalties from customers. Thus, Respondents have failed to present any evidence that would establish patent misuse in this instance.

XV. DOMESTIC INDUSTRY

A. Applicable Law

As stated in the notice of investigation, a determination must be made as to whether an industry in the United States exists as required by subsection (a)(2) of section 337. Section 337 declares unlawful the importation, the sale for importation or the sale in the United States after importation of articles that infringe a valid and enforceable U.S. patent only if an industry in the United States, relating to articles protected by the patent . . . concerned, exists or is in the process of being established. There is no requirement that the domestic industry be based on the same claim or claims alleged to be infringed. 19 U.S.C. § 1337(a)(2).

The domestic industry requirement consists of both an economic prong (*i.e.,* there must be an industry in the United States) and a technical prong (*i.e.*, that industry must relate to articles protected by the patent at issue). *See Certain Ammonium Octamolybdate Isomers,* Inv. No. 337-TA-477, Comm'n Op. at 55, USITC Pub. 3668 (January 2004). The complainant bears the burden of proving the existence of a domestic industry. *Certain Methods of Making Carbonated Candy Products,* Inv. No. 337-TA-292, Comm'n Op. at 34-35, USITC Pub. 2390 (June 1991).

Thus, in this investigation Rambus must show that it satisfies the domestic industry requirement with respect to the Barth and the Dally Patents. As noted, and as explained below, it

is found that these domestic industry requirements have been satisfied for both the Barth and the Dally Patents.

A complainant in a patent-based Section 337 investigation must demonstrate that it is practicing or exploiting the patents at issue. *See* 19 U.S.C. § 1337(a)(2) and (3); *also see Certain Microsphere Adhesives, Process for Making Same, and Products Containing Same, Including Self-Stick Repositionable Notes*, Inv. No. 337-TA-366, Comm'n Op. at 8 (U.S.I.T.C., January 16, 1996) ("*Certain Microsphere Adhesives*"), *aff'd sub nom. Minn. Mining & Mfg. Co. v. U.S. Int'l Trade Comm'n*, 91 F.3d 171 (Fed. Cir. 1996) (Table); *Certain Encapsulated Circuits*, Comm'n Op. at 16. The complainant, however, is not required to show that it practices any of the claims asserted to be infringed, as long as it can establish that it practices at least one claim of the asserted patent. *Certain Point of Sale Terminals and Components Thereof*, Inv. No. 337-TA-524, Order No. 40 (April 11, 2005). Fulfillment of this so-called "technical prong" of the domestic industry requirement is not determined by a rigid formula, but rather by the articles of commerce and the realities of the marketplace. *Certain Diltiazem Hydrochloride and Diltiazem Preparations*, Inv. No. 337-TA-349, U.S.I.T.C. Pub. No. 2902, Initial Determination at 138, (U.S.I.T.C., February 1, 1995) (unreviewed in relevant part) ("*Certain Diltiazem*"); *Certain Double-Sided Floppy Disk Drives and Components Thereof*, Inv. No. 337-TA-215, 227 U.S.P.Q. 982, 989 (Comm'n Op. 1985) ("*Certain Floppy Disk Drives*").

The test for claim coverage for the purposes of the technical prong of the domestic industry requirement is the same as that for infringement. *Certain Doxorubicin and Preparations Containing Same*, Inv. No. 337-TA-300, Initial Determination at 109 (U.S.I.T.C., May 21, 1990) ("*Certain Doxorubicin*"), *aff'd*, Views of the Commission at 22 (October 31, 1990). "First, the claims of the patent are construed. Second, the complainant's article or

process is examined to determine whether it falls within the scope of the claims." *(Id.)* As with infringement, the first step of claim construction is a question of law, whereas the second step of comparing the article to the claims is a factual determination. *Markman,* 52 F.3d at 976. The technical prong of the domestic industry can be satisfied either literally or under the doctrine of equivalents. *Certain Excimer Laser Systems for Vision Correction Surgery and Components Thereof and Methods for Performing Such Surgery,* Inv. No. 337-TA-419, Order No. 43 (July 30, 1999). The patentee must establish by a preponderance of the evidence that the domestic product practices one or more claims of the patent. *See Bayer,* 212 F.3d at 1247.

The economic prong of the domestic industry requirement is defined in subsection 337(a)(3) as follows:

> (3) For purposes of paragraph (2), an industry in the United States shall be considered to exist if there is in the United States, with respect to the articles protected by the patent, copyright, trademark or mask work concerned –
>
> (A) Significant investment in plant and equipment;
>
> (B) Significant employment of labor or capital; or
>
> (C) Substantial investment in its exploitation, including engineering, research and development, or licensing.

19 U.S.C. § 1337(a)(3).

The economic prong of the domestic industry requirement is satisfied by meeting the criteria of any one of the three factors listed above.

Section 337(a)(3)(C) provides for domestic industry based on "substantial investment" in the enumerated activities, including licensing of a patent. *See Certain Digital Processors and Digital Processing Systems, Components Thereof, and Products Containing Same*, Inv. No. 337-TA-559, Initial Determination at 88 (May 11, 2007) ("*Certain Digital Processors*"). Mere ownership of the patent is insufficient to satisfy the domestic industry requirement. *Certain*

Digital Processors at 93. (citing the Senate and House Reports on the Omnibus Trade and Competitiveness Act of 1988, S.Rep. No. 71). However, entities that are actively engaged in licensing their patents in the United States can meet the domestic industry requirement. *Certain Digital Processors* at 93. In establishing a domestic industry under Section 337(a)(3)(C), the complainant does not need to show that it or one of its licensees is practicing a patent-in-suit. *See Certain Semiconductor Chips with Minimized Chip Package Size and Products Containing Same*, Inv. No. 337-TA-432, Order No. 13, at 11, (January 24, 2001) ("*Certain Semiconductor Chips*"). The complainant must, however, receive revenue, *e.g.* royalty payments, from its licensing activities. *Certain Digital Processors,* at 93-95 ("Commission decisions also reflect the fact that a complainant's receipt of royalties is an important factor in determining whether the domestic industry requirement is satisfied . . . [t]here is no Commission precedent for the establishment of a domestic industry based on licensing in which a complainant did not receive any revenue from alleged licensing activities. In fact, in previous investigations in which a complainant successfully relied solely on licensing activities to satisfy section 337(a)(3), the complainant had licenses yielding royalty payments.") (citations omitted). *See also Certain Video Graphics Display Controllers and Products Containing Same*, Inv. No. 337-TA-412, Initial Determination at 13 (May 14, 1999) (*"Certain Video Graphics Display Controllers"*); *Certain Integrated Circuit Telecommunication Chips and Products Containing Same Including Dialing Apparatus*, Inv. No. 337-TA-337, U.S.I.T.C. Pub. No. 2670, Initial Determination at 98 (March 3, 1993) (*"Certain Integrated Circuit Telecommunication Chips"*); *Certain Zero-Mercury-Added Alkaline Batteries, Parts Thereof and Products Containing Same*, Inv. No. 337-TA-493, Initial Determination at 142 (June 2, 2004) (*"Certain Zero-Mercury-Added Alkaline Batteries"*); *Certain Semiconductor Chips*, Order No. 13 at 6 (January 24, 2001); *Certain Digital*

Satellite System DSS Receivers and Components Thereof, Inv. No. 337-TA-392, Initial and Recommended Determinations at 11 (December 4, 1997) ("*Certain Digital Satellite System DSS Receivers*").

In *Certain Multimedia Display & Navigation Devices & Systems, Components Thereof, & Products Containing Same*, Inv. No. 337-TA-694, Comm'n Op. (Aug. 8, 2011) ("*Navigation Devices*"), the Commission stated that a complainant seeking to rely on licensing activities must satisfy three requirements: (1) the investment must be "an investment in the exploitation of the asserted patent;" (2) the investment must relate to licensing; and (3) the investment "must be domestic, *i.e.*, it must occur in the United States." *Id.* at 7-8. The Commission stated that "[o]nly after determining the extent to which the complainant's investments fall within these statutory parameters can we evaluate whether complainant's qualifying investments are 'substantial,' as required by the statute." *Id.* at 8.

Under the first of the three requirements, the complainant must show a nexus between the licensing activity and the asserted patent. *Id.* at 9. When the asserted patent is part of a patent portfolio, and the licensing activities relate to the portfolio as a whole, the Commission requires that the facts be examined to determine the strength of the nexus between the asserted patent and the licensing activities. *Id.* The Commission provided a non-exhaustive list of factors to consider, such as (1) whether the licensee's efforts relate to "an article protected by" the asserted patent under Section 337 (a)(2)-(3); (2) the number of patents in the portfolio; (3) the relative value contributed by the asserted patent to the portfolio; (4) the prominence of the asserted patent in licensing discussions, negotiations, and any resulting licensing agreement; and (5) the scope of technology covered by the portfolio compared to the scope of the asserted patent. *Id.* at 9-10. The Commission explained that the asserted patent may be shown to be particularly important or

valuable within the portfolio where there is evidence that: (1) it was discussed during licensing negotiations; (2) it has been successfully litigated before by the complainant; (3) it is related to a technology industry standard; (4) it is a base patent or pioneering patent; (5) it is infringed or practiced in the United States; or (6) the market recognizes the patent's value in some other way. *Id.* at 10-11.

Once a complainant's investment in licensing the asserted patent in the United States has been assessed in the manner described above, the next inquiry is whether the investment is "substantial." 19 U.S.C. § 1337(a)(3)(C). The Commission takes "a flexible approach whereby a complainant whose showing on one or more of the three section 337(a)(3)(C) requirements is relatively weak may nevertheless establish that its investment is 'substantial' by demonstrating that its activities and/or expenses are of a large magnitude." *Multimedia Display and Navigation Devices*, Comm'n Op. at 15. The Commission has indicated that whether an investment is "substantial" may depend on:

> (1) the nature of the industry and the resources of the complainant;
>
> (2) the existence of other types of "exploitation" activities;
>
> (3) the existence of license-related "ancillary" activities;
>
> (4) whether complainant's licensing activities are continuing; and
>
> (5) whether complainant's licensing activities are the type of activities that are referenced favorably in the legislative history of section 337(a)(3)(C).

Id. at 15-16. The complainant's return on its licensing investment (or lack thereof) may also be circumstantial evidence of substantiality. *Id.* at 16. In addition, litigation expenses may be evidence of the complainant's investment, but "should not automatically be considered a 'substantial investment in . . . licensing,' even if the lawsuit happens to culminate in a license." *JMA*, 2011 U.S. App. LEXIS 20128 at *13.

B. Barth Patents

Rambus argues that it satisfies the domestic industry requirement for the Barth Patents based on its licensing activities. (CIB at 281.)

Investment in the exploitation of the asserted patent

As set forth above, Rambus must show a nexus between its licensing activities and the Barth Patents. The evidence shows that Technology License Agreements license all patents necessary to practice Rambus's proprietary Concurrent Interface Technology, which include the Barth Patents. (CX-9547C, Smith Direct Q&A 67-84; CX-51C through CX-59C; CX-579C.) In this regard, testimony from Rambus employees and documentation on its Concurrent Interface Technology show that the asserted Barth Patent claims cover that technology. (CX-9544C, Hampel Direct Q&A 32-116; CX-9547C.0009-13; CX-51C through CX-59C; CX-579C).) As such, the asserted Barth Patents are licensed under the Technology License Agreements.[40]

The evidence shows that the Patent License Agreements license all patents necessary to practice various technologies, such as JEDEC-type DDR memory systems. Those agreements license, *inter alia*, DDR memory controllers, and, as set forth *supra*, Rambus has shown that DDR memory controllers practice the asserted Barth Patents. (CX-9547C Q&A 85-119; CX-38C thorugh CX-42C; CX-44C through CX-48C; CX-50C; CX-661C; CX-662C; CX-7627C; CX-7628C; CX-7629C; CX-7642C; CX7643C; CX-9543C.0219-236.) In this regard, the analysis set forth in the infringement section above shows that the asserted Barth Patent claims

[40] With respect to the patents asserted in this investigation, the Commission has notably stood by its prior domestic industry finding as to the Barth Patents in light of *Multimedia Display and Navigation Devices* standard. (*See* Commission DI Letter.) The Commission's position on this issue is consistent with the fact that the *Multimedia Display and Navigation Devices* opinion favorably cited the domestic industry finding in the 661 investigation for a number of different points in its discussion of the nexus requirement. For example, the Commission indicated that evidence that the patent license is tied to a particular technology (as opposed to a license of all patents in a broad field) suggests a nexus between a licensing activity and the asserted patent. *See Multimedia Displays and Navigation,* Comm'n Op. at 10 (citing 661 DI Opinion at 7-9).

indeed cover those systems.[41] As such, the asserted Barth Patents are also licensed under the Patent License Agreements.

The evidence further shows a strong nexus between the Barth Patents and the Technology License Agreements and the Patent License Agreements. According to the Commission, such evidence includes:

> In our assessment of the strength of the nexus between a complainant's licensing activities and an asserted patent included in a large patent portfolio . . . [t]he Commission may also consider other factors including, but not limited to, (1) the number of patents in the portfolio, (2) the relative value contributed by the asserted patent to the portfolio, (3) the prominence of the asserted patent in licensing discussions, negotiations and any resulting license agreement, and (4) the scope of technology covered by the portfolio compared to the scope of the asserted patent.

Multimedia Display and Navigation Devices at 9-10.

According to the Respondents, "Rambus has no evidence that any of its licensees actually practice the asserted patents." (RIB at 282.) The evidence shows that former respondent nVidia took a license under those patents so that it may continue to import what would otherwise be excluded products. (RX-7267C (nVidia License Agreement); Kaplan, Tr. 1878:08-1879:06.) Furthermore, the evidence shows that third party Samsung is a current licensee under the Barth I patents and is selling licensed JEDEC-complaint memory devices to Respondent Garmin. *See supra* Section XIII.) Thus, the evidence shows that at least Samsung, nVidia, and certain of their customers actually practice the asserted Barth Patents.

a) Size of the Licensed Portfolios

The evidence shows that the portfolio licensed by the Technology License Agreements is fairly small, with the Barth Patent family making up more than half of patents in that particular portfolio. (SX-0007C at 6 (First Supplemental Response to Interrogatory No. 78). Specifically,

[41] A similar analysis resulted in the violation finding on the Barth I patents in the 661 ID. (*See* 661 ID at 20-31.)

there are [redacted] applicable patents included in the Concurrent Interface Technology, over half of which are in the Barth family, including the asserted Barth Patents. Thus, this factor strongly weighs in favor of a domestic industry finding based at least on the Technology License Agreements.

Focusing on Rambus's overall patent portfolio, the Respondents argue that the fact that the *licensed* groups of patents (*e.g.*, the Concurrent RDRAM group which includes the Barth I patents) on which Rambus relies are of much smaller size than the portfolio as a whole is irrelevant because Rambus is relying on the amount of the entire licensed portfolio. (RIB at 283.) While Rambus has not allocated its expenditures to particular sub-portfolios or sub-groups *per se*, the evidence provides at least some circumstantial evidence of correspondingly significant investments in those portfolios. For example, in 2008, [redacted] was attributable to royalties from patent license agreements that grant rights to the Barth Patents. (CX-7617C.0004; *see also* CX-9547C, Smith Direct Q/A 154-156 (testifying as to CX-7617C).) In addition, approximately [redacted] in revenue was attributable to Concurrent RDRAM royalties, which also relate to the Barth Patents. (CX-7616C.0003; *see also* CX-9547C, Smith Direct Q/A 151-153 (testifying as to CX-7616C).[42] This revenue information is at least strong circumstantial evidence that Rambus's investments in the asserted sub-portfolios/sub-groups are substantial as well.[43]

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42 While the analysis set forth above was based on the information available for 2008, similar approximations can be done for other years using revenue information provided within the same set of documents.

43 *See Certain Cigarettes & Pkg. Thereof*, Inv. No. 337-TA-424, Order No. 59, 2000 ITC LEXIS 120 (Mar. 1, 2000) (allocating expenditures based as a percentage of sales revenue); *Certain Laminated Floor Panels*, Inv. No. 337-TA-545, Order No. 17, 2006 ITC LEXIS 157 (Mar. 2, 2006) (same).

b) Relative Value Contributed By The Barth I Patents

With respect to the relative value contributed by an asserted patent, the Commission has explained:

> [T]he asserted patent may be shown to be particularly important or valuable within the portfolio where there is evidence that (1) it was discussed during the licensing negotiation process, (2) it has been successfully litigated before by complainant, (3) it relates to a technology industry standard, (4) it is a base patent or a pioneering patent, (5) it is infringed or practiced in the United States, or (6) the market recognizes its value in some other way.

Multimedia Display And Navigation Devices at 10-11. Several of these points are applicable here. For example, the evidence shows that the Barth I patents were discussed during licensing negotiations with prospective licensees. (CX-9547C, Smith Direct Q&A 162-192; CX-69C through 80C; CX-5659C; CX-5665C; CX-5666C; CX-5694C; CX-5703C; CX-7613C; CX-7615C.) The May 4, 2010 licensing-presentation to former Respondent Freescale is illustrative and includes full page slides on the asserted '353 and '405 Patents:

(CX-7608C.0005; *see also* CX-7608C.0006 ('405 patent); Kaplan, Tr. 1869:07-1870:11.) This licensing-presentation also correctly notes that the Barth Patents were successfully litigated in

[redacted]

Finally, the evidence shows that the Barth Patents relate to JEDEC's DDR memory standards as previously discussed in the infringement section of this brief and in the 661 ID. (Kaplan, Tr. 1865:08-20; 661 ID at 22-30.) Thus, this factor weighs in favor of finding a licensing-based domestic industry as to the Barth Patents.

Respondents argue that "Rambus should be precluded from arguing that any of its patents are especially valuable" because a corporate witness, Mr. Smith, testified that Rambus "has no core patents" and because the "structure" and "timing" of the license agreements downplays the significance of the asserted patents in particular. (RIB 283.) However, Respondents fail to provide any further explanation and further fail to address the factors that the Commission considers in making the determination as to whether or not the patents are relatively valuable to the portfolio." (RIB a t284.) As set forth above, the evidence shows, however, that in determining the relative value of an asserted patent, the Barth and Dally Patents are of high relative value. Thus, this factor supports finding a licensing-based domestic industry in this investigation.

c) Prominence of the Barth Patents

For at least the reasons discussed above with respect to the relative value factor, the evidence shows that the Barth I patents were prominent in licensing discussions and negotiations, and have been successfully licensed by Rambus.

The Respondents argue that neither the Barth I patents nor the Dally patents are "prominent" under *Multimedia Display and Navigation Devices* because "[n]one of the license agreements Rambus relies upon as proof of its domestic industry actually mention any of the Asserted Patents" and because, while "[e]ighteen presentations over five years" do explicitly identify the asserted patents, "Rambus exaggerates the role of the asserted patents in those presentations . . . ." (RIB at 285.) The ALJ finds Respondents arguments unpersuasive.

With respect to the license agreements, Respondents fail to point to any Commission precedence that requires the explicit identification of the asserted patents in the license agreement. Indeed, the Concurrent RDRAM technology agreements were found in the 661 investigation to *support* a domestic industry finding despite the fact that none of the agreements list specific patents.[44]

As for the licensing presentations, Respondents argue that the asserted patents are buried in "long lists of patents" that "Rambus had to add circles around . . . to ensure that they could be located" by witnesses that testified as to these presentations at trial. (RIB at 285.) Respondents fail to address the presentations in which full slides were devoted entirely to the asserted patents, often including a summary of relevant reexamination and litigation proceedings, claim charts

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[44] *See Certain Semiconductor Chips Having Synchronous Dynamic Random Access Memory Controllers And Products Containing Same*, Inv. No. 337-TA-661, Order No. 21 at 5-6 (Oct. 7, 2009) (unreviewed ID) ("661 DI Opinion") ("The license agreements do not list the specific patent numbers that are subject to the license agreement, but instead license the portfolio of patents covering the defined 'Licensed Products,' which would include products practicing the asserted patents.").

comparing asserted claims to potential infringing products, etc. (CX-7608.0005 to 0006 (licensing presentation to former Respondent Freescale); CX-5694C.0033 to 0038 and 0048 to 0055 (licensing presentation to Respondent Broadcom); CX-5703C.0006, 0009, 0010 and 0016-0018 (licensing presentation to Respondent Broadcom); CX-7615C.0002 to 0008 (licensing presentation to Respondent STM); Kaplan, Tr. 1869:07-1870:11.) Consistent with the page long slides highlighting the asserted patents in detail, the fact that some of Rambus's licensing presentations were made *after* institution of the 661 Investigation and explicitly discuss patents asserted in that investigation shows that the Barth Patents were indeed the subject of considerable focus during the corresponding licensing negotiations. (CX-5659C (May 2010 presentation to Respondent Freescale); CX-5694C (December 2009 presentation to Respondent Broadcom); CX-5703C (March 2010 presentation to Respondent Broadcom); CX-7613C (March 2010 presentation to non-party Panasonic); CX-7615C (July 2009 presentation to Respondent STM).) Thus, the evidence shows that the Barth Patents were frequently and repeatedly highlighted to prospective licensees.

d) The Scope of Technology Covered by the Portfolios Compared to the Scope of the Barth I Patents

For at least the reasons discussed above with respect to the size of the licensed portfolio factor, the evidence shows that the scope of the Barth Patents is similar to the scope of technology covered by the relevant portfolios. Namely, the evidence shows that the Technology License Agreements include only a small number of patents, of which the Barth Patents make up more than half. With respect to the Patent License Agreements, the evidence shows that the licensed technology has essentially the same scope as the asserted Barth Patents, which collectively cover the use of memory controllers in conjunction with JEDEC-compliant memory

devices. Thus, this factor weighs in favor of finding a licensing-based domestic industry as to the Barth I patents.

Respondents argue that the Asserted Patents at most cover a narrow slice of Rambus' portfolio and that Rambus' technology licenses include many things other than the asserted Patents: cell designs, trade secrets, other (unspecified patents, know-how, etc.)" and that Rambus's patent licenses "include ***all*** Rambus patents that read on any integrated circuit." (RIB at 286 (emphasis in original).) The ALJ finds Respondents' argument unpersuasive.

Respondents erroneously fail to address the particular groupings of patents (and associated licenses) within Rambus's overall portfolio that are at issue in this investigation. As set forth *supra*, the Barth Patents make up a significant portion of these smaller groupings of patents. Respondents fail to truly take into consideration how the Barth Patents fit within their respective groupings of patents as to the technologies covered by those groupings. *See Multimedia Display and Navigation Devices* at 12 ("Evidence showing how the asserted patents fit together congruently with other patents in the portfolio covering a specific technology may demonstrate a stronger nexus to the licensing activity than evidence indicating that the patents cover a wide variety of technologies bearing only a limited relationship to one another."). The evidence shows that the Barth Patents are the breadth and critical to the technology covered by its respective groupings (*i.e.*, the Concurrent RDRAM, patent license, and SerDes groups) and its relationship to other patents within those groups.

Investment relates to licensing

Rambus's investments are for Rambus's licensing efforts, and Rambus is not relying on litigation expenses. (CX-9547C.0003-09.)

Respondents also argue that the evidence of record as to Rambus's investments in its licensing-based domestic industry should be discounted because the company has a "litigation-driven business model" rather than a licensing-driven business model. (RIB at 287.) However, this position is contrary to the Respondents' prior statements in which they characterized Rambus as a licensing entity – *not* a litigation entity:

> Rambus' principal business consists of licensing. Indeed, it is this licensing activity that provides the sole basis for Rambus' claim that it has a domestic industry in the technology covered by the patents it is asserting. As such, Rambus' day-to-day business activities include identifying potential licensees, assessing the relationship between Rambus' intellectual property and the potential licensees' products, and negotiating licenses.
>
> * * *
>
> *As a licensing entity, Rambus' assessment of potential licensees and their products is purely a business function-not a legal one.*

Respondents' Memorandum in Support of Motion to Compel Production of Licensing Documents, Mtn. Dkt. No. 753-056, EDIS Doc. ID 454832 at 1 (July 19, 2011) (emphasis added); *see also id.* at 2 ("A central feature of Rambus' business model is the monetization of its intellectual property *through licensing . . . activities*.") (emphasis added); *id.* at 3 ("Rambus' organization reflects the fact that it engages in *licensing-related business activities*-activities that do not involve lawyers or traditional legal work, such as litigation or even contract drafting.") (emphasis added). Respondents' cannot change positions and arguments to fit the argument of the day.

Moreover, even assuming that Rambus relies in part on litigation related expenses to support its domestic industry contentions, recent Federal Circuit precedent confirms that such expenses can properly be considered as part of a licensing-based domestic industry analysis. *See John Mezzalingua Associates, Inc. v. U.S. Int'l Trade Comm'n*, --- F.3d --- , 2011 U.S. App. LEXIS 20128 at *13-20 (Fed. Cir. Oct. 4, 2011) ("*JMA*") (affirming a finding of no licensing-

based domestic industry in an investigation in which the Administrative Law Judge used a "flexible framework" to analyze the extent to which complainant's litigation investments related to a domestic industry showing). Thus, the evidence of record as to Rambus's investments in its licensing-based domestic industry is relevant and must be considered.

Investment in the United States.

There is no dispute that Rambus's licensing activities are directed from its California headquarters. (CX-9547C.0005.)

Investments are substantial

The evidence further shows that Rambus's domestic investments in licensing its Barth Patents by way of the Technology License Agreements and the Patent License Agreements were substantial. (CX-9547C, Smith Direct Q/A 15-29, 149-156.) The evidence shows that Rambus has over 30 employees involved in its U.S. based licensing practice at an expense of over [redacted] for the time period from 2006 through the first half of 2010. (*id.* at Q&A 17, 18, 27, 29.) Rambus's technology license agreements that encompass the Barth Patents have generated over [redacted] in royalties since 2002. (*id.* at Q&A 153.) Rambus's patent license agreements that encompass the Barth Patents have generated over [redacted] in royalties in this same timeframe. (*id.* at Q/A 156.)[45]

[45] Respondents argue that Rambus relies on some licenses that predate the filing of the Barth I patents to show its investment. RPB at 418. But Respondents fail to recognize that the license agreements relied upon here license the Barth I family and all Rambus patents filed or allowed after execution of the agreements, such as the asserted Barth I patents. *See, e.g.,* CX-51C, CX-52C, CX-53C, CX-54C, CX-55C, CX-57C, CX-58C, CX-59C, and CX-579C. Thus, relying on these investments is entirely proper.

Since 2006, Rambus has had over 30 U.S. employees directly involved in one or more of the following functions related to Rambus's overall licensing operations: promoting Rambus's patented technology to potential licensees and the public, negotiating license agreements, drafting license agreements, ensuring compliance with those agreements, conducting market analysis for licensing opportunities, conducting patent and licensing strategy, and providing technical licensing support. (CX-9547C.0003-04.)

While the Respondents may dispute the extent to which Rambus has invested in the asserted patents *in particular*, the Respondents do not appear to dispute the magnitude of Rambus's overall domestic investments or the revenue resulting from those investments. Instead, the Respondents fault Rambus for relying on "firm-wide licensing efforts" that are not specific to a given portfolio (*e.g.*, Rambus's Concurrent RDRAM and SerDes portfolios) or to particular patents (*e.g.*, the asserted patents) within such a portfolio. (RIB at 281 ("Rambus has provided no evidence that would permit even a rough estimation of the proportion of its firm-wide activities related to the Asserted Patents or the alleged portfolios containing them.").) Respondents' arguments fail.

The Commission does not require, as the Respondents concede, "strict mathematical proof of the investment in licensing certain patents among others in a portfolio may not be possible." *See Multimedia Display and Navigation Devices*, at9-13. In this regard, the Commission has explained:

> Depending on the facts in each investigation, a complainant may be able to establish the strength of the nexus between the asserted patent and its licensing activities by means of evidence showing that its licensing activities are particularly focused on the asserted patent among the group of patents in the portfolio or through other evidence that demonstrates the relative importance or value of the asserted patent within the portfolio. For example, in *Coaxial Cable Connectors Remand*, at 24-25, the evidence of record showed that one of the patents was clearly more important and more valuable than the other. In our

> assessment of the strength of the nexus between a complainant's licensing activities and an asserted patent included in a large patent portfolio, a potentially important consideration is whether the licensee's efforts relate to "an article protected by" the asserted patent under section 337(a)(2)-(3). For example, if a licensee's product is an "article protected by" the patent, then the license is by definition connected to that patent. The Commission may also consider other factors including, but not limited to, (1) the number of patents in the portfolio, (2) the relative value contributed by the asserted patent to the portfolio, (3) the prominence of the asserted patent in licensing discussions, negotiations and any resulting license agreement, and (4) the scope of technology covered by the portfolio compared to the scope of the asserted patent.

Multimedia Display and Navigation Devices, at 9-10. Therefore, in light of the foregoing evidence, the ALJ finds that Rambus's investments are substantial.

C. Dally Patents

As for the Dally Patents, the evidence shows that a licensing-based domestic industry also exists as to the asserted Dally Patents.

Investment in the exploitation of the patent

The evidence shows that Rambus has entered into several agreements that license all patents necessary to practice various Serializer-Deserializer (SerDes) technologies. (CX-9547C, Smith Direct Q/A 59-61, 120-148; CX-4326C; CX-4329C; CX-4330C; CX-4334C; CX-4338C; CX-7134C.) The evidence further shows that the asserted Dally Patent claims cover technologies that are licensed in those agreements. (CX-9548C, Sobelman Direct Q&A 14-15, 18, 28-114; CX-9524C, Singer Direct Q/A 544-550.) In addition, certain of the agreements on which Rambus relies expressly identify the Dally patent family as being licensed. (CX-9547C, Smith Direct Q/A 130, 132; CX-4329C; CX-4338C.) Rambus's September 2004 agreement with Alliance is representative in this regard, and reads in part:

[redacted]

[redacted]

(CX-4338C.0003 (underlining in original, italics added for emphasis).) This section explicitly mentions [redacted][46] [redacted].

The evidence further shows that Rambus is currently paying royalties to MIT for licensees' use of those patents. (Smith, Tr. 560:05-561:10.) The breadth of the asserted Dally Patent coupled with the analysis of licensed SerDes cores shows that the asserted Dally Patents are among the Dally Patents being practiced by Rambus licensees. (CX-9548C, Smith Direct (comparing claims from the '857 and '494 patents to licensed SerDes designs).)

The evidence further shows a strong nexus between the Dally Patents and the SerDes portfolio.

[46] The agreement refers to [redacted]

a) Size of the Licensed Portfolio

The evidence show that Rambus's SerDes portfolio has [redacted] in total, ten of which are from the Dally patent family. (SX-0007C at 3-5 (First Supplemental Response To Interrogatory No. 78).) The Dally patents are also licensed by Rambus's patent license agreement with Samsung. (CX-9547C.0024 (citing CX-4339C).) Rambus has paid MIT [redacted] in royalties for this license to the Dally patents alone (including [redacted] in ongoing royalty payments), demonstrating the value of the Dally patents. (HTr. 560-61; CX-4342C.0009-10.)

Respondents argue that fact that the *licensed* groups of patents (*e.g.*, the SerDes group which includes the Dally patents) on which Rambus relies are of much smaller size than the portfolio as a whole is irrelevant because "Rambus is not relying upon the dollars invested only in licensing its 'SerDes' portfolio or its 'concurrent interface' portfolio." As with the Barth Patents, the evidence shows significant investments in this portfolio. Specifically, the evidence shows that [redacted] was attributable to royalties from technology license agreements which license technology related to the Dally Patents. (CX-4342C.0003; *see also* CX-9547C, Smith Direct Q/A 157-159 (testifying as to CX-4342C).)

b) Relative Value Contributed By The Dally Patents

The evidence shows that the Dally patents were discussed during the licensing negotiation process with prospective licensees. (CX-9547C, Smith Direct Q/A 160-163, 168-169, 181-185, 193-198; CX-7612C.0007; CX-7613C.0009.) The September 29, 2010 presentation (CX-7612C) to Respondent Broadcom is representative:

(CX-7612C.0007.) In addition, the evidence shows that the asserted Dally Patents relate to at least the PCI Express and DisplayPort standards as previously discussed in the infringement section of this brief. In fact, the Respondents effectively concede this point in arguing that Rambus has an obligation to license the asserted Dally patents due FRAND obligations arising out of a Rambus predecessor's participation in the standard-setting organization that promulgated the PCI Express standards. (*See supra* Section XI; Kaplan, Tr. 1832:05-1833:16.)

c) Prominence of the Dally Patents

As set forth above, the evidence also shows that the Dally Patents were prominent in licensing discussions and negotiations, and resulted in consummated license agreements. In addition, the evidence shows that nVidia sought out a license as to the asserted Dally patents before becoming aware that Rambus had obtained exclusive license rights as to those patents. (CX-10764C, Singer Rebuttal Q/A 428-429; Kaplan, Tr. 1853:06-1855:03.) Furthermore, the evidence shows that half of the technology license agreements relied upon by Rambus explicitly reference the Dally Patent family, defining that family to include the asserted Dally Patents. (CX-9547C.0019-22 (citing CX-4013C, CX-4329C, CX-4338C).)

As for the licensing presentations, Respondents argue that the asserted patents are buried in "long lists of patents" that "Rambus had to add circles around . . . to ensure that they could be located" by witnesses that testified as to these presentations at trial. (RIB at 285.) However, as set forth abovie, certain of the agreements relied upon by Rambus in this investigation explicitly

list at least the Dally Patent family. While the asserted Dally Patents may not be listed *by number*, they clearly fall within the umbrella of the Dally Patent family, which is explicitly listed. This further demonstrates the prominence of the Dally patents in Rambus's licensed portfolio.

d) The Scope of Technology Covered by the Portfolios Compared to the Scope of the Dally Patents

The evidence shows that the Dally Patents have scope similar to the scope of technology covered by the portfolios. (CX-9548C.0002-50; *see also* CX-9542C.0506; CX-9547C.0018-23.) For example, the evidence shows that the SerDes portfolio includes only a small number of patents, of which the Dally patent family makes up a significant portion. (SX-0007C at 3-5 (First Supplemental Response to Interrogatory No. 77).)

Investment relates to licensing

As with the Barth Patents, the evidence shows that Rambus's investments are for Rambus's licensing efforts, and Rambus is not relying on litigation expenses. (CX-9547C.0003-09.)

Respondents' argument that there is no nexus because certain licenses were signed before issuance of the Dally patents is contrary to the law. (RIB at 283.) *See Certain Video Game Sys. and Controllers*, Inv. No. 337-TA-743, Comm'n Op. at 6 (Apr. 14, 2011) (stating that section 337(a)(3)(C) "is broad enough to cover 'investments' made before issuance of the patent"). Respondents' own expert agreed that it would make sense that technology license agreements might be signed before a patent covering that technology had finally issued from the PTO. (HTr. 1820-21.) That Rambus has not received royalties for one agreement is of no import, as a domestic industry does not even require consummated licenses, let alone licenses that result in royalties. *See Stringed Musical Instruments and Components Thereof*, Inv. No. 337-TA-586, Comm'n Op., 2009 ITC Lexis 2250, at *43 (Dec. 2009).

Investment in the United States

As with the Barth Patents, there is no dispute that Rambus's licensing activities are directed from its California headquarters. (CX-9547C.0005.)

Investments are substantial

The evidence also shows that Rambus's investments in licensing the asserted Dally Patents were and continue to be substantial. As with the Barth Patents, the evidence shows that Rambus has made substantial investments in licensing. (CX-9547C, Smith Direct Q/A 15-29, 149, 150, 157-159.) Rambus has over 30 employees involved in its U.S. based licensing practice at an expense of over [redacted] for the time period from 2006 through the first half of 2010. (*Id.* at Q&A 17, 18, 27, 29.) As for the Dally Patents specifically, Rambus's technology license agreements that encompass the Dally Patents have generated over [redacted] in royalties. (*Id.* at Q/A 159.) Rambus has also paid MIT, the owner of record for the Dally patents, over [redacted] in royalties attributed to the Dally patent family. (*Id.* at Q/A 49-54.)

For at least these reasons, the evidence fails to support the Respondents' arguments against finding a licensing-based domestic industry as to the Dally patents.

Having made the foregoing findings on numerous issues covering infringement, validity, unenforceability, standing, and other affirmative defenses, the ALJ finds that the disposition of these material issues satisfies Commission Rule 210.42(d).[47] The ALJ's failure to discuss any

[47] Commission Rule 210.42(d) states:

> (d) Contents. The initial determination shall include: an opinion stating findings (with specific page references to principal supporting items of evidence in the record) and conclusions and the reasons or bases therefor necessary for **the disposition of all material issues of fact, law, or discretion presented in the record**; and a statement that, pursuant to §210.42(h), the initial determination shall become the determination of the Commission unless a party files a petition for

other matter raised by the parties, or any portion of the record, does not indicate that it has not been considered. Rather, any such matter(s) or portion(s) of the record has/have been deemed immaterial.

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review of the initial determination pursuant to §210.43(a) or the Commission, pursuant to §210.44, orders on its own motion a review of the initial determination or certain issues therein.

(emphasis added).

CONCLUSIONS OF LAW

1. The Commission has personal jurisdiction over the parties, and subject-matter jurisdiction over the accused products.
2. The importation or sale requirement of section 337 is satisfied.
3. The accused products literally infringe the asserted claims of the '353, '405 and '109 Patent.
4. The accused products literally infringe the asserted claims of the '857 and '494 Patent.
5. Respondents induce infringement of the asserted claims of the Barth and the Dally Patents.
6. Respondents contribute to the infringement of the asserted claims of the Barth and the Dally Patents.
7. Claims 11-13 of the '353 Patent and claims 1, 20 and 24 of the'109 Patent are invalid under 35 U.S.C. § 102 for anticipation.
8. Claims 1, 4-6, 9-10, 24-28, 35-36, 38-44, 47 and 53 of the '857 Patent and claims 1,2,6 and 8 of the '494 Patent are invalid under 35 U.S.C. § 102 for anticipation.
9. Claims 11-13 of the '353 Patent, claims 11-13, 15 and 18 of the '405 Patent and claims 1, 2, 4, 5, 12, 13, 20, 21 and 24 of the '109 Patent are invalid under 35 U.S.C. § 103 for obviousness.
10. Claims 2, 11-13, 31-34, and 39-52 of the '857 Patent and claims 3, 25, 26, 30, 39, 40 and 42 of the '494 Patent are invalid under 35 U.S.C. § 103 for obviousness.
11. The Barth Patents and the Dally Patents are not invalid for failure to satisfy the written description requirement under 35 U.S.C. § 112.

12. The Barth Patents and the Dally Patents are not invalid for failure to satisfy the definiteness requirement under 35 U.S.C. § 112.

13. The Barth Patents are not invalid for failure to satisfy the utility requirement under 35 U.S.C. § 101.

14. The Barth Patents are not unenforceable due to inequitable conduct.

15. The Barth Patents and the Dally Patents are not unenforceable due to prosecution laches.

16. The Barth Patents are unenforceable due to unclean hands.

17. Rambus is not equitably estopped from asserting the asserted the Barth Patents against Respondents.

18. Rambus is not precluded from seeking injunctive relief for the Barth and the Dally Patents.

19. Rambus has standing to assert the Dally Patents.

20. The doctrine of patent exhaustion applies to those [redacted] products that incorporate the licensed Samsung/Elpida memory devices.

21. The Barth and the Dally Patents are not unenforceable due to patent misuse.

22. It has been established that a domestic industry exists for the Barth and the Dally Patents.

23. It has not been established that a violation exists of section 337 with respect to the '353 Patent, the '405 Patent and the '109 Patent.

24. It has not been established that a violation exists of section 337 with respect to the '857 Patent and the '494 Patent.

XVI. INITIAL DETERMINATION AND ORDER

Based on the foregoing, it is the Initial Determination of this ALJ that no violation of section 337 of the Tariff Act of 1930, as amended, 19 U.S.C. § 1337, has occurred in the importation into the United States, the sale for importation, or the sale within the United States after importation of certain semiconductor chips and products containing same by reason of infringement of one or more of claims 11-13, 15, and 18 of U.S. Patent No. 6,470,405, claims 11-13 of U.S. Patent No. 6,591,353, claims 1-6, 11- 13, 20-22, and 24 of U.S. Patent No. 7,287,109, claims 1, 2, 4-6, 9-13, 24-28, 31-36, 39-44, 47 and 49-53 of U.S. Patent No. 7,602,857 and claims 1-3, 6, 8, 25, 26, 30, 39, 40 and 42 of U.S. Patent No. 7,715,494. Further, this Initial Determination, together with the record of the hearing in this investigation consisting of:

(1) the transcript of the hearing, with appropriate corrections as may hereafter be ordered, and

(2) the exhibits received into evidence in this investigation, as listed in the attached exhibit lists in Appendix A,

are CERTIFIED to the Commission. In accordance with 19 C.F.R. § 210.39(c), all material found to be confidential by the undersigned under 19 C.F.R. § 210.5 is to be given *in camera* treatment.

The Secretary shall serve a public version of this ID upon all parties of record and the confidential version upon counsel who are signatories to the Protective Order (Order No. 1.) issued in this investigation, and upon the Commission investigative attorney.

RECOMMENDED DETERMINATION ON REMEDY AND BOND

I. Remedy and Bonding

The Commission's Rules provide that subsequent to an initial determination on the question of violation of section 337 of the Tariff Act of 1930, as amended, 19 U.S.C. § 1337, the administrative law judge shall issue a recommended determination containing findings of fact and recommendations concerning: (1) the appropriate remedy in the event that the Commission finds a violation of section 337, and (2) the amount of bond to be posted by respondents during Presidential review of Commission action under section 337(j). *See* 19 C.F.R. § 210.42(a)(1)(ii).

A. General Exclusion Order

Under Section 337(d), the Commission may issue either a limited or a general exclusion order. A limited exclusion order instructs the U.S. Customs and Border Protection ("CBP") to exclude from entry all articles that are covered by the patent at issue and that originate from a named respondent in the investigation. A general exclusion order instructs the CBP to exclude from entry all articles that are covered by the patent at issue, without regard to source.

A general exclusion order may issue in cases where (a) a general exclusion from entry of articles is necessary to prevent circumvention of an exclusion order limited to products of named respondents; or (b) there is a widespread pattern of violation of Section 337 and it is difficult to identify the source of infringing products. 19 U.S.C. § 1337(d)(2). The statute essentially codifies Commission practice under *Certain Airless Paint Spray Pumps and Components Thereof,* Inv. No. 337-TA-90, Commission Opinion at 18-19, USITC Pub. 119 (Nov. 1981) ("*Spray Pumps*"). *See Certain Neodymium-Iron-Boron Magnets, Magnet Alloys, and Articles Containing the Same,* Inv. No. 337-TA-372 ("*Magnets*"), Commission Opinion on Remedy, the

Public Interest and Bonding at 5 (USITC Pub. 2964 (1996)) (statutory standards "do not differ significantly" from the standards set forth in *Spray Pumps*). In *Magnets*, the Commission confirmed that there are two requirements for a general exclusion order: a "widespread pattern of unauthorized use;" and "certain business conditions from which one might reasonably infer that foreign manufacturers other than the respondents to the investigation may attempt to enter the U.S. market with infringing articles." The focus now is primarily on the statutory language itself and not an analysis of the *Spray Pump* factors. *Ground Fault Circuit Interrupters and Products Containing Same*, Inv. No. 337-TA-615, Comm'n Op. at 25 (March 9, 2009); *Hydraulic Excavators and Components Thereof*, Inv. No. 337-TA-582, Comm'n Op. at 16-17 (January 21, 2009).

Rambus argues that a tailored general exclusion order directed at all products containing Respondents' Accused Products is necessary because a limited exclusion order will be easily circumvented and there is a widespread pattern of violation and it is difficult to identify the source of the infringing product. (CIB at 291-292.) Specifically, Rambus argues that Respondents will easily be able to evade a limited exclusion order because the products and downstream products are sold to foreign customers and are imported into the U.S. through unknown entities. (CIB at 292.)

Rambus further argues that there is widespread pattern of unauthorized use of Rambus's technology as evidenced by the importation of infringing products by the many named Respondents in this Investigation, as well as the seventeen Respondents found in violation in the 661 Investigation. (CIB at 293.) Rambus argues that Respondents have many additional customers that distribute the Accused Products throughout the world, and those products eventually end up in the United States, but that many Respondents refused to provide

information regarding the identity of customers during discovery, which is further evidence of the difficulty in identifying sources of infringing products.

Respondents argue that Rambus has failed to show that a general exclusion order is warranted. (RIB at 290.) Respondents argue that (1) Rambus has failed to show that Respondents have or ever would seek to circumvent a limited exclusion order; (2) Rambus has faield to offer any evidence that a pattern of violation exists or that there is any difficulty in finding the source of the allegedly infringing goods; and (3) Rambus has failed to present any evidence that the Customer Respondents purchase or otherwise have available to them equivalent generic semiconductor chips that would not be subject to a limited exclusion order. (RIB at 290-293.)

Staff argues that a general exclusion order is not warranted. (SIB at 225-226.) Specifically, Staff argues that the evidence fails to shows that fails to show that it is difficult to identify the source of the infringing products or that circumvention of a limited exclusion order is likely or that there is a widespread pattern of unauthorized use. (SIB at 225-226.)

The ALJ finds that Rambus has failed to show that a general exclusion order is warranted in this investigation. The evidence fails to show that it is sufficiently difficult for Rambus to identify the source of infringing products to justify imposing a general exclusion order under this subsection. This is particularly true in light of the large number of Respondents identified by Rambus in its Complaint. The evidence also fails to show that a general exclusion order is necessary to prevent circumvention of an exclusion order limited to products of the named Respondents. 19 U.S.C. § 1337(d)(2)(A). That certain memory controller and interface chips implicated by this investigation may be manufactured overseas and incorporated into downstream products prior to being imported into the United States is irrelevant because this was

a pre-existing practice known to Complainant. *Semiconductor Chips* at 66-67 (holding a pre-existing practice of manufacturing accused chips overseas and incorporating them into downstream products prior to being imported into the United States cannot be the basis for a conclusion that a general exclusion order is needed to preclude circumvention). Therefore, the ALJ recommends that the Commission not issue a general exclusion order should a violation be found.

B. Limited Exclusion Order

Under Section 337(d), the Commission may issue either a limited or a general exclusion order. A limited exclusion order directed to respondents' infringing products is among the remedies that the Commission may impose, as is a general exclusion order that would apply to all infringing products, regardless of their manufacturer. *See* 19 U.S.C. § 1337(d).

Rambus argues that to the extent that the EPROMs factors apply to Respondents' own infringing products that are "downstream," those factors support excluding all of Respondents' Accused Products. (CIB at 294.) Rambus argues that all of the EPROMs factors support an exclusion order. (CIB at 294-296.)

Respondents argue that the scope of the LEO should not extend beyond the Respondents' accused chips to any downstream products and to the extent that any downstream product does not contain a semiconductor chip from the accused Supplier Respondent, those downstream products should not be excluded. (RIB at 293-294.) Respondents argue that excluding downstream products will provide little relief to Rambus and will disrupt legitimate trade in the United States. (RIB at 294.) Respondents argue that the EPROM factors and public interest factors weigh against issuing a LEO excluding downstream products. (RIB at 294-297.) Staff agrees that the LEO should not include any products that do not contain a semiconductor chip

from the Supplier Respondents, but should include downstream products that contain the accused semiconductor chips from Supplier Respondents. (SIB at 227-228.)

Should the Commission find a violation, the ALJ recommends that the limited exclusion order should apply to any downstream products that contain the accused semiconductor chips but should not include any products that do not contain an accused semiconductor chip from the Supplier Respondents. *See Certain Erasable Programmable Read-Only Memories, Components Thereof, Products Containing Such Memories, and Processes for Making Such Memories*, Inv. No. 337-TA-276, USITC Pub. 2196 (May 1989). The evidence shows that: (1) the importance of the accused chips to operation of the downstream products is high; (2) a limited exclusion order (as proposed by the Staff) would issue only as to the named Respondents; (3) Rambus would be denied effective relief if downstream products were not included as the accused chips are almost always imported as part of a larger product; (4) licensed products are available as alternatives to the accused chips; (5) there is a high likelihood that the downstream products of the named Respondents include the accused chips; (6) an appropriate certification provision can be added to reduce the risk that legitimate trade would be disrupted as well as the burden on Customs to identify products not covered by the exclusion order; and (7) the relative value of the infringing component is high in certain accused products. Therefore, the ALJ finds that the evidence supports the inclusion of downstream relief as to the named Respondents only under the EPROM factors.

Should Respondents ASUS, Audio Partnership, Cisco, HP, Motorola, Oppo Digital, Seagate, and/or others attempt to rely on the testimony of Dr. Vander Veen as purportedly demonstrating that exclusion of certain downstream products is not warranted, such reliance is misplaced. *See generally* RX-6290C, Vander Veen Rebuttal. Dr. Vander Veen admitted at trial

that he performed solely a quantitative analysis in determining the value of the infringing components relative to the value of the downstream products, and thus could not opine on the extent the infringing components contribute to the operation and functionality of the downstream products. Vander Veen, Tr. 1782:11-1783:25. In addition, Dr. Vander Veen's quantitative analysis is suspect given his: (1) use of inflated pricing information (Vander Veen, Tr. 1785:22-1791:13); (2) failure to distinguish certain downstream products (*e.g.*, motherboards, server cards, hard drives, etc.) that are imported without being incorporated into larger downstream products (*e.g.*, computers, servers, etc.) (Vander Veen, Tr. 1798:09-1801:07); and (3) assumption (without evidentiary support) that certain products for which he lacked pricing information can be treated the same as other products for which limited pricing information was provided (Vander Veen, Tr. 1801:08-1803:12). For at least these reasons, the evidence fails to support the Respondents' view that certain downstream products should be exempted from a limited exclusion order.

C. Cease and Desist Order

Section 337 provides that in addition to, or in lieu of, the issuance of an exclusion order, the Commission may issue a cease and desist order as a remedy for violation of section 337. *See* 19 U.S.C. § 1337(f)(1). The Commission generally issues a cease and desist order directed to a domestic respondent when there is a "commercially significant" amount of infringing, imported product in the United States that could be sold so as to undercut the remedy provided by an exclusion order. *See Certain Crystalline Cefadroxil Monohydrate*, Inv. No. 337-TA-293, USITC Pub. 2391, Comm'n Op. on Remedy, the Public Interest and Bonding at 37-42 (June 1991); *Certain Condensers, Parts Thereof and Products Containing Same, Including Air Conditioners for Automobiles*, Inv. No. 337-TA-334, Comm'n Op. at 26-28 (Aug. 27, 1997).

Rambus argues that a cease and desist order against all Respondents. (CIB at 296.) Specifically, Rambus argues that the evidence shows that respondents Asus, [redacted], Hitachi, LSI, Oppo, and Seagate currently maintain significant inventory of accused products in the United States. (CIB at 296-297.) Rambus argues that a cease and desist order recommend entry of a cease and desist order prohibiting Respondents from importing, marketing, advertising, demonstrating, sampling, warehousing inventory for distribution, offering for sale, selling, distributing, licensing, or use of any semiconductor chips that include memory controllers and/or peripheral interfaces and products containing said semiconductor chips that infringe any claim of the Asserted Patents. (CIB at 297.) Staff agrees that a cease and desist order should be issued against these listed respondents. (SIB at 229-230.)

Respondents argue that Rambus has failed to show that the downstream Customer Respondents maintain a commercially significant inventory of accused products. (RIB at 298.) Respondents argue that any cease and desist order against the downstream products will provide little relief to Rambus. (RIB at 298.)

[redacted] Therefore, cease and desist orders are appropriate as to these Respondents.

D. Bond During Presidential Review Period

The Administrative Law Judge and the Commission must determine the amount of bond to be required of a respondent, pursuant to section 337(j)(3), during the 60-day Presidential

review period following the issuance of permanent relief, in the event that the Commission determines to issue a remedy. The purpose of the bond is to protect the complainant from any injury. 19 C.F.R. § 210.42(a)(1)(ii), § 210.50(a)(3).

When reliable price information is available, the Commission has often set the bond by eliminating the differential between the domestic product and the imported, infringing product. *See Certain Microsphere Adhesives, Processes for Making Same, and Products Containing Same, Including Self-Stick Repositionable Notes*, Inv. No. 337-TA-366, Comm'n Op. a 24 (1995). In other cases, the Commission has turned to alternative approaches, especially when the level of a reasonable royalty rate could be ascertained. *See, e.g., Certain Integrated Circuit Telecommunication Chips and Products Containing Same, Including Dialing Apparatus*, Inv. No. 337-TA-337, Comm'n Op. at 41 (1995). A 100 percent bond has been required when no effective alternative existed. *See, e.g., Certain Flash Memory Circuits and Products Containing Same*, Inv. No. 337-TA-382, USITC Pub. No. 3046, Comm'n Op. at 26-27 (July 1997)(a 100% bond imposed when price comparison was not practical because the parties sold products at different levels of commerce, and the proposed royalty rate appeared to be *de minimis* and without adequate support in the record).

Rambus argues that the bond should be set at 100% of the entered value. (CIB at 297.) Rambus argues that a reasonable royalty rate is insufficient because it would be manifestly unfair to Rambus's legitimate licensees to merely charge Respondents essentially the same royalty rate. (CIB at 297.)

Respondents the bond should be determined as a percentage of a "reasonable royalty" which should be no more than what Rambus has set for other similar technology in the past. (RIB at 299.) Staff agrees. (SIB at 230-231.)

The ALJ recommends that the Commission set a bond at a reasonable royalty rate of the entered value of the accused products. Rambus's argument that the bond should be set at 100% of the entered value because a reasonable royalty would be unfair to Rambus's licensees is tantamount to punishing Respondents for past infringing acts. The Commission is not the appropriate forum for such punitive redress.

II. Conclusion

In accordance with the discussion of the issues contained herein, it is the RECOMMENDED DETERMINATION ("RD") of the ALJ that the Commission should issue a limited exclusion order directed at Respondents products found to infringe the Barth Patents and the Dally Patents, including downstream products that contain the accused products. The Commission should also issue a cease and desist order directed toward respondents Asus, Garmin, Hitachi, LSI, Oppo, and Seagate who currently maintain significant inventories of Accused Products in the United States that prohibits the sale of any commercially significant quantities of the Accused Products. Furthermore, if the Commission imposes a remedy following a finding of violation, Respondents should be required to post a bond set at a reasonably royalty rate of the entered value of the accused products during the Presidential review period.

Within seven days of the date of this document, each party shall submit to the office of the Administrative Law Judge a statement as to whether or not it seeks to have any portion of this document deleted from the public version. The parties' submissions must be made by hard copy by the aforementioned date.

Any party seeking to have any portion of this document deleted from the public version thereof must submit to this office (1) a copy of this document with red brackets indicating any

portion asserted to contain confidential business information by the aforementioned date and (2) a list specifying where said redactions are located. The parties' submission concerning the public version of this document need not be filed with the Commission Secretary.

SO ORDERED.

Theodore R. Essex
Administrative Law Judge

CERTAIN SEMICONDUCTOR CHIPS AND PRODUCTS CONTAINING SAME **Inv. No. 337-TA-753**

PUBLIC CERTIFICATE OF SERVICE

I, James R. Holbein, hereby certify that the attached **INITIAL DETERMINATION** has been served by hand upon, the Commission Investigative Attorney, **Daniel L. Girdwood, Esq.,** and the following parties as indicated on **March 16, 2012.**

James R. Holbein, Secretary
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