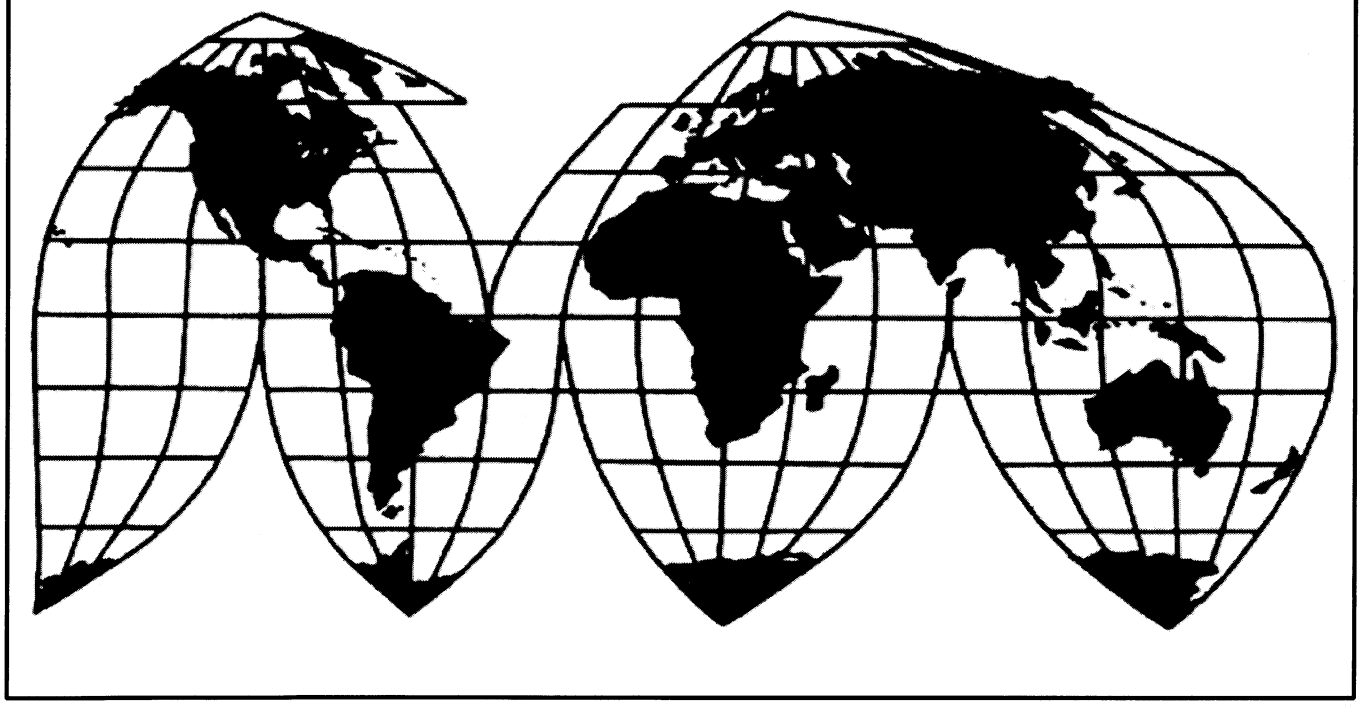
In the Matter of

Certain Flash Memory Devices, and Components Thereof, and Products Containing Such Devices and Components

Investigation No. 337-TA-552

Publication 4010 **June 2008**

U.S. International Trade Commission



Washington, DC 20436

U.S. International Trade Commission

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Irving A. Williamson*
Dean A. Pinkert*

---

*Commissioner Irving A. Williamson was sworn in on February 7, 2007, and Commissioner Dean A. Pinkert was sworn in on February 26, 2007; they did not participate in this investigation. Commissioner Stephen Koplan, whose term ended on February 6, 2007, and Commissioner Jennifer A. Hillman, whose term ended on February 23, 2007, did participate in this investigation.

Address all communications to
Secretary to the Commission
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Washington, DC 20436

U.S. International Trade Commission

Washington, DC 20436
www.usitc.gov

In the Matter of

Certain Flash Memory Devices, and Components Thereof, and Products Containing Such Devices and Components

Investigation No. 337-TA-552

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UNITED STATES INTERNATIONAL TRADE COMMISSION
Washington, D.C.

In the Matter of **CERTAIN FLASH MEMORY DEVICES, AND COMPONENTS THEREOF, AND PRODUCTS CONTAINING SUCH DEVICES AND COMPONENTS**	**Investigation No. 337-TA-552**

NOTICE OF COMMISSION DECISION NOT TO REVIEW THE ADMINISTRATIVE LAW JUDGE'S FINAL INITIAL DETERMINATION THAT THERE IS NO VIOLATION OF SECTION 337; TERMINATION OF INVESTIGATION

AGENCY: U.S. International Trade Commission.

ACTION: Notice.

SUMMARY: Notice is hereby given that the United States International Trade Commission has determined not to review an initial determination ("ID") issued by the presiding administrative law judge ("ALJ") finding no violation of section 337 of the Tariff Act of 1930, as amended, and to terminate the investigation.

FOR FURTHER INFORMATION CONTACT: Jean Jackson, Esq., Office of the General Counsel, U.S. International Trade Commission, 500 E Street, S.W., Washington, D.C. 20436, telephone (202) 205-3104. Copies of non-confidential documents filed in connection with this investigation are or will be available for inspection during official business hours (8:45 a.m. to 5:15 p.m.) in the Office of the Secretary, U.S. International Trade Commission, 500 E Street, S.W., Washington, D.C. 20436, telephone (202) 205-2000. General information concerning the Commission may also be obtained by accessing its Internet server at *http://www.usitc.gov*. The public record for this investigation may be viewed on the Commission's electronic docket (EDIS) at *http://edis.usitc.gov*. Hearing-impaired persons are advised that information on this matter can be obtained by contacting the Commission's TDD terminal on (202) 205-1810.

SUPPLEMENTARY INFORMATION: The Commission instituted this investigation on November 4, 2005, based on a complaint filed by Toshiba Corporation of Tokyo, Japan ("Toshiba") under section 337 of the Tariff Act of 1930, as amended, 19 U.S.C. § 1337. 70 *Fed. Reg.* 67192-193 (November 4, 2005). The complainant alleged violations of section 337 in the importation and sale of certain flash memory devices and components thereof, and products containing such devices and components, by reason of infringement of claims 1-4 of U.S. Patent No. 5,150,178 ("the '178 patent"); claims 1, 6 and 7 of U.S. Patent No. 5,270,969 ("the '969 patent"); and claims 1 and 4 of U.S. Patent No. 5,517,449 ("the '449 patent"). The complainant

named Hynix Semiconductor of Ichon-si, Republic of Korea, and Hynix Semiconductor America, Inc. of San Jose, California (collectively "Hynix") as respondents.

On November 21, 2005, Toshiba moved for leave to amend the complaint to add claim 5 of the '178 patent. On December 2, 2005, the ALJ issued an ID (Order No. 4) granting the motion to amend the complaint. The Commission determined not to review this ID.

An evidentiary hearing was held from July 5, 2006, through July 13, 2006. On November 6, 2006, the ALJ issued his final ID and recommended determination on remedy and bonding. The ALJ concluded that there was no violation of section 337. Specifically, he found that the asserted claims of the '178, '969, and '449 patents are not infringed and are not invalid, and that there is no domestic industry involving the three patents.

On November 17, 2006, complainant Toshiba, the Commission investigative attorney, and respondent Hynix petitioned for review of various portions of the final ID. On November 28, 2006, all parties filed responses to the petitions for review.

Having examined the record of this investigation, including the ALJ's final ID, the petitions for review, and the responses thereto, the Commission has determined not to review the ALJ's ID, and has terminated the investigation.

The authority for the Commission's determination is contained in section 337 of the Tariff Act of 1930, as amended (19 U.S.C. § 1337), and in section 210.42 - 45 of the Commission's Rules of Practice and Procedure (19 C.F.R. § 210.42-45).

By order of the Commission.

Marilyn R. Abbott
Secretary to the Commission

Issued: December 22, 2006

CERTAIN FLASH MEMORY DEVICES AND COMPONENTS THEREOF, AND PRODUCTS CONTAINING SUCH DEVICES AND COMPONENTS **337-TA-552**

CERTIFICATE OF SERVICE

I Marilyn R. Abbott, hereby certify that the attached **NOTICE OF COMMISSION DECISION NOT TO REVIEW THE ADMINISTRATIVE LAW JUDGE'S FINAL INITIAL DETERMINATION THAT THERE IS NO VIOLATION OF SECTION 337; TERMINATION OF INVESTIGATION** has been served on upon all parties and Commission Investigative Attorney Bryan F. Moore, Esq., via first class mail and air mail where necessary on d December 22, 2006.

Marilyn R. Abbott, Secretary
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UNITED STATES INTERNATIONAL TRADE COMMISSION
Washington, D.C.

In the Matter of	)	
	)	
CERTAIN FLASH MEMORY DEVICES AND COMPONENTS THEREOF, AND PRODUCTS CONTAINING SUCH DEVICES AND COMPONENTS	)	Investigation No. 337-TA-552

Notice To The Parties

The Final Initial and Recommended Determinations were filed on November 6, 2006. Attached are the title page, the conclusions of law and the order, which are not confidential and which form a portion of said determinations. If a party wants to pick up a copy of the Final Initial and Recommended Determinations from the Secretary's Office, it should telephone the Secretary's Office after 11:00 am on November 7 to determine when the filing will be so available.

Counsel for complainant, respondents and the staff received a copy of this notice on November 6, 2006.

Paul J. Luckern
Administrative Law Judge

Issued: November 6, 2006

PUBLIC VERSION

UNITED STATES INTERNATIONAL TRADE COMMISSION
Washington, D.C.

In the Matter of	)	
	)	
CERTAIN FLASH MEMORY DEVICES	)	Investigation No. 337-TA-552
AND COMPONENTS THEREOF, AND	)	
PRODUCTS CONTAINING SUCH	)	
DEVICES AND COMPONENTS	)	

Final Initial and Recommended Determinations

This is the administrative law judge's Final Initial Determination, under Commission rule 210.42. The administrative law judge, after a review of the record developed, finds that there is jurisdiction; that the claims in issue of U.S. Patent No. 5,150,178, No. 5,270,969 and No. 5,517,449 are not invalid; that the asserted claims are not infringed; and that there is no domestic industry involving said patents. Thus, he finds no violation of section 337 of the Tariff Act of 1930, as amended.

This is also the administrative law judge's Recommended Determination on remedy and bonding, pursuant to Commission rules 210.36(a) and 210.42(a)(1)(ii). Should the Commission find a violation, the administrative law judge recommends that the Commission issue a limited exclusion order directed to infringing NAND flash chips originating in any way from respondents, and to certain downstream products containing said chips. He also recommends a cease and desist order. He further recommends that any bond, during the Presidential review period, be in the amount of 100 percent of the entered import value of the infringing chips.

CONCLUSIONS OF LAW

1. The Commission has in rem jurisdiction and in personam jurisdiction.

2. There has been an importation of accused NAND flash chips which are the subject of the alleged unfair trade allegations.

3. An industry does not exist in the United States that exploits the '178, '969 and '449 patents in issue, as required by subsection (a)(2) of section 337.

4. Respondents' accused products do not infringe the asserted claims of the '178, '969 and '449 patents.

5. The asserted claims of the '178, '969 and '449 patents are not invalid.

6. There is no violation of section 337.

7. Should the Commission determine that there is a violation, the record supports (1) issuance of a limited exclusion order directed to infringing NAND flash chips produced by respondents, as well as certain downstream products produced by third parties and containing said chips, (2) the issuance of a cease and desist order and (3) the imposition of a bond in the amount of 100 percent of the entered value of any infringing chips, during the Presidential review period.

ORDER

Based on the foregoing, and the record as a whole, it is the administrative law judge's Final Initial Determination that there is no violation of section 337 in the importation into the United States, sale for importation, and the sale within the United States after importation of certain flash memory devices and components thereof. It is also the administrative law judge's recommendation, should the Commission determine that there is a violation, that (1) a limited

exclusion order should issue directed to infringing NAND flash chips produced by respondents, as well as certain downstream products produced by third parties containing said chips, (2) a cease and desist order should issue, and (3) a bond of 100 percent of the entered value of any infringing NAND flash chips should be imposed during the Presidential review period.

The administrative law judge hereby CERTIFIES to the Commission his Final Initial and Recommended Determinations together with the record consisting of the exhibits admitted into evidence. He also CERTIFIES ALJ Exh. 1 (9/12/06 OG publication relating to terminal disclaimer of the '449 patent). The pleadings of the parties filed with the Secretary, and the transcript of the pre-hearing conference and the hearing, as well as other exhibits, are not certified, since they are already in the Commission's possession in accordance with Commission rules.

Further, it is ORDERED that:

1. In accordance with Commission rule 210.39, all material heretofore marked in camera because of business, financial and marketing data found by the administrative law judge to be cognizable as confidential business information under Commission rule 201.6(a), is to be given in camera treatment continuing after the date this investigation is terminated.

2. Counsel for the parties shall have in the hands of the administrative law judge those portions of the final initial and recommended determinations which contain bracketed confidential business information to be deleted from any public version of said determinations, no later than November 30, 2006. Any such bracketed version shall not be served via facsimile on the administrative law judge. If no such bracketed version is received from a party, it will mean that the party has no objection to removing the confidential status, in its entirety, from

these initial and recommended determinations.

3. The initial determination portion of the Final Initial and Recommended Determinations, issued pursuant to Commission rule 210.42(h)(2), shall become the determination of the Commission forty-five (45) days after the service thereof, unless the Commission, within that period shall have ordered its review of certain issues therein, or by order, has changed the effective date of the initial determination portion. The recommended determination portion, issued pursuant to Commission rule 210.42(a)(1)(ii), will be considered by the Commission in reaching a determination on remedy and bonding pursuant to Commission rule 210.50(a).

Paul J. Luckern
Administrative Law Judge

Issued: November 6, 2006

CERTAIN FLASH MEMORY DEVICES AND COMPONENTS THEREOF, AND PRODUCTS CONTAINING SUCH DEVICES AND COMPONENTS

Investigation No. 337-TA-552

CERTIFICATE OF SERVICE

I, Marilyn R. Abbott, hereby certify that the attached **Notice To The Parties** was served by hand upon Commission Investigative Attorney Bryan F. Moore, Esq. and upon the following parties via first class mail, and air mail where necessary, on **November 7, 2006.**

Marilyn R. Abbott

Marilyn R. Abbott, Secretary
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CERTAIN FLASH MEMORY DEVICES AND COMPONENTS THEREOF, AND PRODUCTS CONTAINING SUCH DEVICES AND COMPONENTS

Investigation No. 337-TA-552

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CERTAIN FLASH MEMORY DEVICES AND COMPONENTS THEREOF, AND PRODUCTS CONTAINING SUCH DEVICES AND COMPONENTS

Investigation No. 337-TA-552

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PUBLIC VERSION

UNITED STATES INTERNATIONAL TRADE COMMISSION
Washington, D.C.

In the Matter of	)	
	)	
CERTAIN FLASH MEMORY DEVICES AND COMPONENTS THEREOF, AND PRODUCTS CONTAINING SUCH DEVICES AND COMPONENTS	)	Investigation No. 337-TA-552

Final Initial and Recommended Determinations

This is the administrative law judge's Final Initial Determination, under Commission rule 210.42. The administrative law judge, after a review of the record developed, finds that there is jurisdiction; that the claims in issue of U.S. Patent No. 5,150,178, No. 5,270,969 and No. 5,517,449 are not invalid; that the asserted claims are not infringed; and that there is no domestic industry involving said patents. Thus, he finds no violation of section 337 of the Tariff Act of 1930, as amended.

This is also the administrative law judge's Recommended Determination on remedy and bonding, pursuant to Commission rules 210.36(a) and 210.42(a)(1)(ii). Should the Commission find a violation, the administrative law judge recommends that the Commission issue a limited exclusion order directed to infringing NAND flash chips originating in any way from respondents, and to certain downstream products containing said chips. He also recommends a cease and desist order. He further recommends that any bond, during the Presidential review period, be in the amount of 100 percent of the entered import value of the infringing chips.

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e. "an insulating film formed to define grooves" . . . 145

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ABBREVIATIONS

CBr	Complainant's Post-hearing Brief
TFF	Complainant's Proposed Finding
TORPFF	Complainant's Objection To Respondent's Proposed Finding
TOSPFF	Complainant's Objection To Staff's Proposed Finding
TRSPFF	Complainant's Proposed Rebuttal Finding To SPFF
CRBr	Complainant's Post-hearing Reply Brief
TRRPFF	Complainants' Proposed Rebuttal Finding to RPFF
CX	Complainant's Exhibit
JX	Joint Exhibit
RBr	Respondents' Post-hearing Brief
RX	Respondents' Exhibit
RPFF	Respondents' Proposed Finding
ROSPFF	Respondents' Objection To Staff's Proposed Finding
ROTFF	Respondents' Objection To Complainant's Proposed Finding
RRTFF	Respondent's Proposed Rebuttal Findings To TFF
RRSPFF	Respondents' Proposed Rebuttal Finding to SFF
RRBr	Respondents' Post-hearing Reply Brief
SBr	Staff's Post-hearing Brief
SRBr	Staff's Post-hearing Reply Brief
SPFF	Staff's Proposed Finding

Tr. Transcript Of Pre-hearing Conference and Hearing

I. Procedural History

By notice, which issued on October 31, 2005 the Commission instituted an investigation, pursuant to subsection (b) of section 337 of the Tariff Act of 1930, as amended, to determine whether there is a violation of subsection (a)(1)(B) of section 337 in the importation into the United States, the sale for importation into the United States, or the sale within the United States after importation of certain flash memory devices or components thereof, or products containing such devices or components, by reason of infringement of one or more of claims 1-4 of U.S. Patent No. 5,150,178 ('178 patent), claims 1 and 6-7 of U.S. Patent No. 5,270,969 ('969 patent), and claims 1 and 4 of U.S. Patent No. 5,517,449 ('449 patent), and whether an industry in the United States exists as required by subsection(a)(2) of section 337.

The complaint was filed with the Commission on September 29, 2005, under section 337 of the Tariff Act of 1930, as amended, 19 U.S.C. § 1337, on behalf of Toshiba Corporation of Tokyo, Japan (Toshiba). A supplemental letter was filed on October 20, 2005. Complainant requested in the complaint that the Commission issue a permanent exclusion order and permanent cease and desist orders.

The following were named in the notice of investigation as respondents and were served with the complaint:

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Kyoungki-do, Korea and

Hynix Semiconductor America, Inc.
3101 North First Street
San Jose, California 95134[1]

Order No. 3, which issued on December 2, 2005, set a target date of January 4, 2007, which meant that any final initial determination on violation (ID) should have been filed no later than the close of business on October 4, 2006. Order No. 23, which issued on September 29, extended the target date to February 5, 2007. The extension meant that any ID should be filed no later than the close of business on Monday, November 6, 2006.

Order No. 4, which issued on December 2, 2005, granted complainant's Motion No. 552-1 to add claim 5 of the '178 patent to the investigation. The Commission, in a notice dated December 28, determined not to review Order No. 4.

Order No. 12, which issued on May 19, 2006, referenced a stipulation of the private parties regarding imports.

Order No. 13, which issued on May 22, 2006, granted complainant's Motion No. 552-9 that it satisfied the economic prong of the domestic industry requirement. The Commission determined not to review Order No. 13 in a notice dated June 12.

On June 26, 2006, there was filed "Complainant Toshiba Corporation's Motion In Limine To Preclude Hynix's Untimely Best Mode And Indefiniteness Arguments With Respect To the '178 Patent" (Motion No. 552-25.) On June 27, there were filed "Complainant Toshiba Corporation's Motion In Limine Seeking Order Binding Respondents To Certain Representations Made By Their Counsel to The Court" (Motion No. 552-27) and "Toshiba Corporation's Motion In Limine To Preclude Respondents For Arguing That Their Representative Products Are Not

[1] The named respondents are referred to as "Hynix".

Representative of Their 120NM Design Rule Products." (Motion No. 552-28.) On June 27, there was also filed "Respondents Hynix Semiconductor Inc. and Hynix Semiconductor America Inc.'s Motion In Limine "(1) to preclude Toshiba from relying on its schematics, (2) to preclude complainant's William Huber from offering testimony, and (3) to preclude Toshiba from relying on certain SEM and TEM images." (Motion No. 552-29.)

Arguments were heard on June 30, 2006 on the motions in limine. At the pre-hearing conference on July 5, Motion No. 552-25 was denied although complainant was given the opportunity to supplement their prehearing statement as to indefiniteness. (Tr. at 41-42.) A ruling on Motion No. 552-27 was reserved. (Tr. at 42-48.) However the motion has been mooted on the ground that no party later indicated a need for a ruling. Motion No. 552-28 was mooted (Tr. at 48-49.) Regarding Motion No. 552-29, item (1) thereof was denied. (Tr. at 50.) Item (2) thereof was denied although respondents were given the opportunity to depose Huber. (Tr. at 50-59.) Item (3) thereof was mooted. (Tr. at 50.)

A pre-hearing conference was conducted on July 5, 2006, with the hearing also commencing on that date and continuing to July 13. In issue at the hearing were claims 1, 2, 3, 4, and 5 of the '178 patent, claims 1, 6 and 7 of the '969 patent and claims 1 and 4 of the '449 patent. All parties participated in the hearing. Post-hearing submissions have been filed.[2] In

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[2] By letter dated August 3, 2006, from respondents' counsel to the administrative law judge, it was stated:

> During the hearing, the Court authorized each of the private parties to file a motion to strike certain portions of the record. I am pleased to report that the parties have met and conferred and agreed to not further burden the record with additional motions.

On August 2, 2006, the staff moved to file an unopposed motion for leave to file its post-

addition the administrative law judge has acted on a letter dated September 26, 2006 from complainant's counsel to the administrative law judge relating to respondents' affirmative defense of double patenting involving the '449 patent. See Section X on "Validity ('449 Patent - Double Patenting)" infra. The matter is now ready for a final decision.

The Final Initial and Recommended Determinations herein are based on the record compiled at the hearing and the exhibits admitted into evidence. The administrative law judge has also taken into account his observation of the witnesses who appeared before him during the hearing. Proposed findings of fact submitted by the parties not herein adopted, in the form submitted or in substance, are rejected as either not supported by the evidence or as involving immaterial matters and/or as irrelevant. Certain findings of fact included herein have references to supporting evidence in the record. Such references are intended to serve as guides to the testimony and exhibits supporting the finding of fact. They do not necessarily represent complete summaries of the evidence supporting said findings.

II. Jurisdiction

The administrative law judge finds that the complaint and notice of investigation state a cause of action under section 337 of the Tariff Act of 1930, as amended. Morever, the importation requirement has been satisfied. See JX 38C where respondents stipulated that they

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hearing findings of fact and conclusions of law one day late. (Motion Docket No. 552-35.) Motion No. 552-35 is granted. On August 2 also Hynix moved for leave to file a corrected post-hearing brief. (Motion Docket No. 552-34.) Motion No. 552-34 is granted. On August 10, Hynix moved for leave to file corrected proposed rebuttal findings of fact. (Motion Docket No. 552-37). Motion No. 552-37 is granted. On August 10 Hynix also moved for leave to file response to proposed findings of fact and conclusion of law of the staff one day late. (Motion Docket No. 552-36). Motion No. 552-36 is granted. On August 11,2006, respondents moved for leave to file corrected exhibit lists. (Motion Docket No. 552-38.) Motion No. 552-38 is granted.

have imported NAND Flash products into the United States and do not contest importation for purposes of jurisdiction in this investigation. Thus, the Commission has in rem jurisdiction over the subject matter of this investigation. See Certain Automated Mechanical Transmission Systems for Medium-Duty and Heavy-Duty Trucks and Components Thereof, Inv. No 337-TA-503, Final Initial and Recommended Determination at 4, Notice of Commission Nonreview (February 24, 2005) (Transmissions). Also, respondents Hynix have appeared in this investigation. Hence, the Commission has in personam jurisdiction. See Transmissions at 4

III. Parties

See FF 1-8.

IV. Experts

Dr. Dimitri Antoniadis has a Ph.D. in physics, and was qualified as an expert witness for Toshiba in areas pertaining to semiconductor devices. (Tr. at 409.)

Mr. John Reed has a Masters Degree in electrical engineering, and was qualified as an expert witness for Toshiba in areas pertaining to semiconductor circuit design and the circuit design of memory chips. (Tr. at 1013-14; CX-281.)

Dr. William Huber has a Ph.D in electrical engineering and was qualified as an expert witness for Toshiba in the field of memory circuit design. (Tr. at 750-53.)

Dr. John Bravman is professor of materials science and engineering, and was qualified as an expert witness for Hynix in areas pertaining to semiconductor device processing and structure. (Tr. at 2147; RX-19.)

Dr. Vivek Subramanian has a Ph.D. in electrical engineering, and was qualified as an expert witness for Hynix in areas pertaining to semiconductor memory design. (Tr. at 1706;

RX-1124.)

Dr. Richard Pashley has a Ph.D. in physics, and was qualified as an expert witness for Hynix in areas pertaining to nonvolatile memory. (Tr. at 2463; RX-1126.)

Dr. Seth Kaplan has a Ph.D. in economics, and was qualified as complainant's expert in the area of international trade and border remedies. (Tr. at 1556, 1560.)

V. The Technology, Products And Patents In Issue

The technology claimed by the '178 patent relates to a multistage gate structure such as a stack gate transistor having an upper control gate and a lower floating gate separated by an insulating layer on a semiconductor substrate. The substrate is divided into element regions with a field oxidation region between each pair of element regions. The floating gates are separated from one another on the substrate. The insulating layer, which separates the control gate from the floating gate, forms a groove in the gap between each pair of floating gates. The control gate, which is made of polysilicon and a high-temperature silicide layer, is on the insulating layer above the substrate and fills the grooves in the gap between each pair of floating gates with the region above the groove being substantially flat. (JX-1.)

The technology claimed by the '969 patent and the '449 patent relates to a nonvolatile memory array in which each memory cell in the array comprises a string of serially-connected storage transistors. Each storage transistor has a floating gate to store charges. One end of each cell is connected to a reference voltage and to a data programming means and readout circuit. Also, during programming, the charge state of the storage transistor is changed. (JX-4; JX-7.)

The accused Hynix products are NAND flash memory devices. (Complaint, ¶ 17.)

(SPFF 10 (undisputed).) NAND flash memory devices are a non-volatile form of EEPROM (Electrically Erasable Programmable Read-Only Memory) that allows multiple memory locations to be erased or written in one programming operation. A flash memory stores information in an array of floating gate transistors, called "cells," each of which traditionally stores one bit of information but may store more than one bit in a multi-level cell configuration. Each cell has a gate stack structure that includes a polysilicon floating gate layer on top of a thin gate oxide layer. (Complaint, ¶ 17; JX-4.) (SPFF 11 (undisputed).)

Complainant relies on certain families of Toshiba/San Disk products to satisfy the technical prong of the domestic industry requirement with respect to the '178 patent. Other NAND products are relied on to satisfy said technical prong as to the '969 and '449 patents.

On September 22, 1992, the '178 patent titled "Gate Structure for a Semiconductor Memory Device," was issued. (JX-1.) The named inventor of the '178 patent is Seiichi Mori. (JX-1.) Complainant Toshiba is the owner by assignment of the '178 patent. (JX-1.) The '178 patent has a total of twelve claims. Asserted claims 1-5 are directed to a semiconductor memory of multistage gate structure. (JX-1). The '178 patent is based on U.S. Appl. No. 690,660 filed April 24, 1991 which in turn claims priority to Japanese application No. 2-106 377 filed April 24, 1990.

The '969 patent titled "Electrically Programmable Nonvolatile Semiconductor Memory Device with NAND Cell Structure," was issued on December 14, 1993. (JX-4.) The named inventor of the '969 patent is Hiroshi Iwahashi. (JX-4.) Toshiba is the owner by assignment of the '969 patent. (JX-4.) The '969 patent has a total of 88 claims. Claims 1, 6, and 7, which are asserted against the accused devices, are directed to a non-volatile memory device. (JX-4.)

The '969 patent is based on U.S. Appl. No. 913,452 filed July 15, 1992. Said application is a continuation of Ser. No. 685,650 filed Apr. 16, 1991, (Pat. No. 5,148,394), which is a continuation of Ser. No. 212,649 filed June. 28, 1988, (Pat. No. 5,008,856.) (JX-4.)

The '449 patent, titled "Memory Cell of Nonvolatile Semiconductor Memory Device," was issued on May 14, 1996. (JX-7.) Hiroshi Iwahashi is the named inventor. Toshiba is owner by assignment of the '449 patent. (JX-7.) The '449 patent has a total of 28 claims. Claims 1 and 4, which are asserted against the accused devices, are directed to a non-volatile memory device. (JX-7.) The '449 patent is based on U.S. Appl. No. 433,072 filed May 3, 1995. Said application is a continuation of Ser. No. 288,219, filed August 9, 1994, (Pat. No. 5,448,517), which is a continuation of Ser. No. 115,100, filed September 2, 1993, (abandoned), which is a continuation of Ser. No. 913,451 filed July 15, 1992, (the '969 patent in issue) which is a continuation of Ser. No. 685,650, Apr. 16, 1991, (Pat. No. 5,148,394 which is involved in respondents' affirmative defense of double patenting) which is a continuation of Ser. No. 212,649 filed June, 28, 1988, (Pat. No. 5,008,856.) (JX-7.)

VI. Level Of Ordinary Skill In The Art

The same person is not necessarily qualified to be a person of ordinary skill in the art with respect to the '178 patent on the one hand and the '969 and '449 patents on the other hand because while the '178 patent deals with process technology, the '969 and '449 patents deal with circuits. (Subramanian, Tr. at 1716; Reed, Tr. at 1037.) For the '969 and '449 patents, the administrative law judge finds that a person of ordinary skill in the art would have the equivalent of a bachelors degree in electrical engineering, material science or a like discipline and at least five years experience in semiconductor memory circuit design. (Reed, Tr. at 1030-

39.)

For the '178 patent, the administrative law judge finds that a person of ordinary skill in the art would have the equivalent of a bachelors degree in electrical engineering , material science or a like discipline and at least five years experience in integrated device fabrication, e.g. problems with steps, etching at steps and cracking at steps. (Antoniadis, Tr. at 423-24.)

VII. Claim Interpretation

Claim interpretation is a question of law. Markman v. Westview Instruments, Inc., 52 F.3d 967, 979 (Fed. Cir. 1995) (en banc), aff'd, 517 U.S. 370 (1996); see Cybor Corp. v. FAS Techs., Inc., 138 F.3d 1448, 1455 (Fed. Cir. 1998). In construing claims, a court should look to intrinsic evidence consisting of the language of the claims, the specification and the prosecution history as it "is the most significant source of the legally operative meaning of disputed claim language." Vitronics Corp. v. Conceptronic, Inc., 90 F.3d 1576, 1582 (Fed. Cir. 1996); see Bell Atl. Network Servs., Inc. v. Covad Comm. Group, Inc., 262 F.3d 1258, 1267 (Fed. Cir. 2001).

The claims themselves "provide substantial guidance as to the meaning of particular claim terms." Phillips v. AWH Corp., 415 F.3d 1303, 1314 (Fed. Cir. 2005), citing Vitronics, 90 F.3d at 1582. It is essential to consider the claim as whole when construing each term, because the context in which a term is used in a claim "can be highly instructive." Id. This requirement is consistent with the Federal Circuit's guidance that a claim term can only be understood "with a full understanding of what the inventors actually invented and intended to envelop with the claim." Phillips, 415 F.3d at 1316, citing Renishaw PLC v. Marposs Societá per Azioni,158 F.3d 1243, 1250 (Fed. Cir. 1998). Claim terms "are generally given their ordinary and accustomed meaning." Vitronics, 90 F.3d at 1582.

In Pause Technology, Inc. v. TIVD, Inc., 419 F.3d 1326 (Fed. Cir. 2005) the Court stated:

> . . . in clarifying the meaning of claim terms, courts are free to use words that do not appear in the claim so long as "the resulting claim interpretation . . . accord[s] with the words chosen by the patentee to stake out the boundary of the claimed property." Cf. Renishaw PLC v. Marposs Societá per Azioni, 158 F.3d 1243, 1248 (Fed. Cir. 1998) (noting that "[w]ithout any claim term susceptible to clarification . . . there is no legitimate way to narrow the property right").

Id. 419 F.3d at 1333. Also, claim terms are presumed to be used consistently throughout the patent, such that the usage of the term in one claim can often illuminate the meaning of the same term in other claims. Research Plastics, Inc. v. Federal Packaging Corp. 421 F.3d 1290, 1295 (Fed. Cir. 2005).

The ordinary meaning of a claim term may be determined by reviewing a variety of sources, which may include the claims themselves, dictionaries and treatises, and the written description, the drawings and the prosecution history. Ferguson Beauregard/Logic Controls v. Mega Sys., LLC, 350 F.3d 1327, 1338 (Fed. Cir. 2003).

The use of a dictionary however may extend patent protection beyond what should properly be afforded by a patent. Also, there is no guarantee that a term is used in the same way in a treatise as it would be by a patentee. Phillips 415 F.3d at 1322. Moreover, the presumption of ordinary meaning will be "rebutted if the inventor has disavowed or disclaimed scope of coverage, by using words or expressions of manifest exclusion or restriction, representing a clear disavowal of claim scope." ACTV, Inc. v. Walt Disney Co., 346 F.3d 1082, 1091 (Fed. Cir. 2003). In Terlap v. Brinkmann Corp. 418F.3d 1379, 1384 (Fed. Cir. 2005), the Court concluded that the district court "attached appropriate weight" to the dictionary definitions in the context of

the intrinsic evidence in reaching its construction of a claim term "clear."

The presence of a specific limitation in a dependent claim raises a presumption that the limitation is not present in the independent claim. Phillips, 415 F.3d at 1315. This presumption is especially strong when the only difference between the independent and dependant claims is the limitation in dispute. SunRace Roots Enter. Co., Ltd v. SRAM Corp., 336 F.3d 1298, 1303 (Fed. Cir. 2003). Differences between the claims are helpful in understanding the meaning of claim terms. Phillips, 415 F.3d at 1314. "[W]here the limitation that is sought to be 'read into' an independent claim already appears in a dependent claim, the doctrine of claim differentiation is at its strongest." Liebel – Flarsheim Co. v. Medrad, Inc., 358 F.3d 898, 910 (Fed. Cir. 2004). An independent claim usually covers a scope "broader than the preferred embodiment, especially if the dependent claims recite the precise scope of the preferred embodiment." RF Delaware v. Pacific Keystone Tech., 326 F.3d 1255, 1264 (Fed. Cir. 2003).

The specification of a patent "acts as a dictionary" both "when it expressly defines terms used in the claims" and "when it defines terms by implication." Vitronics, 90 F.3d at 1582. For example, the specification "may define claim terms by implication such that the meaning may be found in or ascertained by a reading of the patent documents." Phillips, 415 F.3d at 1323, quoting Iredto Access, Inc. v. Echostar Satellite Corp., 383 F.3d 1295, 1300 (Fed. Cir. 2004). Importantly, "the person of ordinary skill in the art is deemed to read the claim term not only in context of the particular claim in which the disputed term appears, but in the context of the entire patent, including the specification." Phillips, 415 F.3d at 1314. The Federal Circuit has explained that "although the specification often describes very specific embodiments of the invention, we have repeatedly warned against confining the claims to those embodiments."

Phillips, 415 F.3d at 1323.

A patentee may deviate from the conventional meaning of a particular claim term by making the intended meaning of a particular claim term clear (1) in the specification or (2) during the patent's prosecution history. Lear Siegler, Inc. v. Aeroquip Corp., 733 F.2d 881, 889 (Fed. Cir. 1984) (Lear Siegler). If using a definition that is contrary to the definition given by those of ordinary skill in the art, however, the patentee's specification must communicate a deliberate and clear preference for the alternate definition. Kumar v. Ovonic Battery Co., Inc., 351 F.3d 1364, 1368 (Fed. Cir. 2003) (Kumar), (citing Apple Computers, Inc. v. Articulate Sys., Inc., 234 F.3d 14,21 n.5 (Fed. Cir. 2000)). In ascribing an alternative definition than the ordinary meaning, the intrisinc evidence must "clearly set forth" or "clearly redefine" a claim term so as to put one reasonably skilled in the art on notice that the patentee intended to so redefine the claim term. Bell Atlantic Network Services, Inc. v. Covad Communications Group, Inc., 262 F.3d 1258, 1268 (Fed. Cir. 2001) (Bell Atlantic).

The prosecution history, including "the prior art cited," is "part of the 'intrinsic evidence.'" Phillips, 415 F3d at 1317. The prosecution history "provides evidence of how the inventor and the PTO understood the patent." Id. Thus, the prosecution history can often inform the meaning of the claim language by demonstrating how an inventor understood the invention and whether the inventor limited the invention in the course of prosecution, making the claim scope narrower than it would otherwise be. Vitronics, 90 F.3d at 1582-83; see also Chimi v. PPG Indus., Inc., 402 F.3d 1371, 1384 (Fed. Cir. 2005) ("The purpose of consulting the prosecution history in construing a claim is to exclude any interpretation that was disclaimed during prosecution"), quoting ZMI Corp. v. Cardiac Resuscitator Corp., 844 F.2d 1576, 1580

(Fed. Cir. 1988); Southwall Techs., Inc. v. Cardinal IG Co., F.3d 1570, 1576 (Fed. Cir. 1995). The prosecution history includes any reexamination of the patent. Intermatic Inc. v. Lamson & Sessions Co., 273 F.3d 1355, 1367 (Fed. Cir. 2001).

In addition to the intrinsic evidence, the administrative law judge may consider extrinsic evidence when interpreting the claims. Extrinsic evidence consists of all evidence external to the patent and the prosecution history, including inventor testimony and expert testimony. This extrinsic evidence may be helpful in explaining scientific principles, the meaning of technical terms, and terms of art. See Vitronics Corp., 90 F.3d at 1583; Markman, 52 F.3d at 980. However, "[e]xtrinsic evidence is to be used for the court's understanding of the patent, not for the purpose of varying or contradicting the terms of the claims." Markman, 52 F.3d at 981. Also, the Federal Circuit has viewed extrinsic evidence in general as less reliable than the patent and its prosecution history in determining how to read claim terms. Phillips, 415 F.3d at 1318. In addition, while extrinsic evidence may be useful, it is unlikely to result in a reliable interpretation of patent claim scope unless considered in the context of the intrinsic evidence. Phillips, 415 F.3d at 1319. However, in Tap Pharmaceutical Products, Inc. v. Owl Pharmaceuticals, LLC 419 F.3d 1346 (Fed. Cir. 2005), the Court concluded that:

> In light of the two different possible meanings for the term "containing," it was entirely reasonable for the district court to look to the specification as well as extrinsic evidence to determine the manner in which the term was used in three patents at issue.

Id. 419 F.3d at 1354. In Nystrom v. Trex Company 424 F.3d 1136 (Fed. Cir. 2005), the Court stated:

> . . . as explained in Phillips, Nystrom is not entitled to a claim construction divorced from the context of the written description

> and prosecution history. The written description and prosecution history consistently use the term "board" to refer to wood decking materials cut from a log. Nystrom argues repeatedly that there is no disavowal of scope of the written description or prosecution history. Nystrom's argument is misplaced. Phillips, 415 F.3d at 1321 ("The problem is that if the district court starts with the broad dictionary definition in every case and fails to fully appreciate how the specification implicitly limits that definition, the error will systematically cause the construction of the claim to be unduly expansive."). What Phillips now counsels is that in the absence of something in the written description and/or prosecution history to provide explicit or implicit notice to the public– i.e., those of ordinary skill in the art– that the inventor intended a disputed term to cover more than the ordinary and customary meaning revealed by the context of the intrinsic record, it is improper to read the term to encompass a broader definition simply because it may be found in a dictionary, treatise, or other extrinsic source. Id.

Id. 424 F.3d at 1144, 1145. In Free Motion Fitness Inc. v. Cybex International, Inc. 423 F.3d 1343 (Fed. Cir. 2005), the Court concluded that:

> under Phillips, the rule that 'a court will give a claim term the full range of its ordinary meaning', Rexnord Corp. v. Laitram Corp., 274 F.3d 1336, 1342 (Fed.Cir. 2001), does not mean that the term will presumptively receive its broadest dictionary definition or the aggregate of multiple dictionary definitions. Phillips, 415 F.3d at 1320- 1322. Rather, in those circumstances, where references to dictionaries is appropriate, the task is to scrutinize the intrinsic evidence in order to determine the most appropriate definition.

423 F.3d at 1348,49. In Network Commerce, Inc. v. Microsoft Corp. 422 F.3d 1353 (Fed. Cir. 2005), the Court concluded:

> As we recently reaffirmed in Phillips, "conclusory, unsupported assertions by experts as to the definition of a claim term are not useful to a court." Phillips, 415 F.3d at 1318. Here [expert] Coombs does not support his conclusion [the "download component" need not contain the boot program] with any references to industry publications or other independent sources. Moreover, expert testimony at odds with the intrinsic evidence must be disregarded. Id. ("[A] court should discount any expert

> testimony that is clearly at odds with the claim construction mandated by . . . the written record of the patent." (internal quotations and citation omitted). That is the case here.

Id., at 1361.

Patent claims should be construed so as to maintain their validity. However, that maxim is limited to cases in which a court concludes, after applying all the available tools of claim construction, that the claim is still ambiguous. Phillips, 415 F.3d at 1327. If the only reasonable interpretation renders the claim invalid, then the claim should be found invalid. See, e.g., Rhine v. Casio, Inc., 183 F.3d 1342, 1345 (Fed. Cir. 1999).

A. Asserted Claims Of The '969 Patent

1. A nonvolatile semiconductor memory device comprising:

a memory cell array comprising memory cells arranged in matrix form having rows and columns and row lines and column lines, each memory cell including cell transistors connected in series, and each of the cell transistors having a control gate, a floating gate, a channel region and an insulation film between the floating gate and the channel region, for electrically storing data by using charges stored in the floating gate, each memory cell having a first terminal and a second terminal, the first terminals of the memory cells in the same column being commonly connected to one of the column lines, the second terminals of the memory cells being connected to a reference potential, and the control gates of the cell transistors in the same row being commonly connected to one of the row lines;

row selection means for designating one of the rows of the memory cells in response to a row selection signal;

column selection means for designating one of the columns of the memory cells in response to a column selection signal;

data latching means for storing data, connected to each of the column lines; and

data programming means for selectively programming the cell transistors, wherein a selected cell transistor is programmed in accordance with data corresponding to the stored data of the data latching means, the cell transistor holds an injected state of electrons which are injected through the insulation film into the floating gate by utilizing a tunnel effect by the data programming means when the stored data of the data latching means is a first logic level, and the cell transistor

holds an emitted state of electrons which are emitted through the insulation film from the floating gate by utilizing a tunnel effect by the data programming means when the stored data of the data latching means is a second logic level.

6. A nonvolatile semiconductor memory device according to any one of claims 1 to 5, further comprising selection transistors respectively inserted between the first terminals of the memory cells and the column lines, gates of the selection transistors being connected to one of the row lines.

7. A nonvolatile semiconductor memory device according to any one of claims 1 to 5, further comprising switching means respectively inserted between the second terminals of the memory cells and the reference potential, and controlled so as to be in an off state when the data programming means stores data.

1. Claim 1

a. "data"

In issue is the claimed phrase "data" which is found in the phrases "data programming means" and "data latching means" of independent claim 1 of the '969 patent, the only asserted independent claim of the '969 patent. (JX-4 at 23:10, 12.)

Complainant argued that the term "data" should be interpreted consistent with its ordinary meaning in the field of nonvolatile memory devices as "the information that comes into memory, passes through the latch or other circuitry of the memory device, and ultimately is programmed into the memory cells." (CBr at 24; TFF 368-370.) Complainant relied upon the testimony of its expert, Reed, for the proposition that the ordinary meaning of "data" in the field is "what comes into the memory to be programmed and what might be subsequently read out of the memory after programming." (CBr at 24; Reed, Tr. at 1048-49.) It is also argued that under the interpretation advanced by Reed, information that is presented at the I/O pins of a nonvolatile memory device and then is programmed or stored into the memory cells of the device is "data" at both of those points and at each point in between. (CBr at 24.)

Complainant further argued that the ordinary meaning of "data" that Reed relied on in conducting his analysis is completely consistent with the use of that term in the claims and the specification of the '969 patent. (CBr at 24-25; TFF 368-370.) Complainant, in support, relied on the testimony of Kanazawa (FF 9-11) and Quader (FF 17-18), and argued that Kanazawa and Quader were individuals who are skilled in the relevant art, and that they used the word "data" throughout their hearing testimony in a manner that was consistent with complainant's proposed interpretation. (CBr at 25; TFF 360-367.) In addition, complainant argued that its interpretation is consistent with how respondents' engineers, who work on NAND flash products, use the term "data" for example, (1) "the data input path" from the "IOPAD" to the input buffer, (2) the "cell data input path" from the input buffer to the data buffer, (3) the "data-in-cycle path" from the data buffer to the page buffer, and (4) the final programming of what admittedly is "data" in the cell array of a NAND flash device. (CBr at 25; CRBr at 16; TFF 372-374.)

Respondents argued that "data," in the context of nonvolatile memory, refers to final target memory states for the cell transistors being programmed. (RBr at 42.) Respondents also argued that both respondents' expert Subramanian and complainant's expert Reed, agree that "data" should receive its ordinary meaning in the art. (RBr at 38; RPFF 1221.) Respondents further argued that one of Reed's definitions of "data" is consistent with Subramanian's definition of "data" as the "final target memory states for the cell transistors being programmed." (RBr at 38; RPFF 1222.)

Respondents argued that the intrinsic evidence and the extrinsic evidence, including the plain and ordinary meaning of "data" supports limiting the meaning of "data" to "the final target memory states for the cell transistors being programmed." (RBr at 39-42; RPFF 1221-22, 1225,

1227-41.) Respondents, in support, relied on the testimony of their expert, Subramanian, and the IEEE Standard Dictionary of Electrical and Electronic Terms, from 1988, for the proposition that the ordinary meaning of "data" in the field, is "the final binary representation of the information that is stored in or read out of a memory array." (RBr at 38, 41; Subramanian, Tr. at 1755:16-18; RX-143 at 236.) Additionally, respondents argued that their engineers' use of the word "data" is a "colloquial use of the term 'data,'" and that the term "data", as found in the claims and the specification of the '969 patent, is different than the "colloquial use of the term 'data.'" (RBr at 42; Subramanian, Tr. at 1960:16-21, 1962:11-16.)

The staff argued that data is a common English word that should not be given a narrow definition unless it is expressly limited by the specification or the prosecution history.[3] (SBr at 21; SPFF 98.) The staff also argued that "data" should be interpreted to mean "the information that can be stored in a data latch or memory array or the like." (SBr at 21; SPFF 99.)

The staff argued that both complainant's and respondents' interpretations are overly narrow as they improperly import limitations into the claim (SBr at 21); and that respondents' proposed interpretation imposes an unrealistic restriction on the meaning of "data" by adding the concept of "final target state," which is not found in the dictionaries on which respondents relied on. (SBr at 21-22; RDX-21; SPFF 100.) Thus, the staff argued that the specification does not clearly limit "data" to a final target state. (SBr at 22; SPFF 101.) The staff also argued that the claim language itself makes it clear that the value or type of data in the "data latching means"

[3] The finding of fact that the staff relied on for its statement that "data" is a common English word that should not be given a narrow definition unless it is expressly limited by the specification or the prosecution history, namely SPFF 98, is not found in the staff's Proposed Finding of Facts and Conclusions of Law submission. Hence the staff has provided no evidentiary support for said statement.

need not be identical to final stored state, as respondents would require. (SBr at 22.) For example, the staff argued that a subsequent "wherein" clause of claim 1 of the '969 patent provides "a selected cell transistor is programmed in accordance with data corresponding to the stored data of the data latching means." (SBr at 22; JX-4 at 23:13-16; SPFF 101 (emphasis added).) The staff further argued that that clause indicates that the type of "data" in the latching means need not be identical to the data in the cell; that complainant's interpretation recites "instructions and commands,"[4] which are not recited in the specification; and that data is a representation of information and nothing in the specification limits how that data is to be represented. (SBr at 22; SPFF 103.)

All the parties agreed that the term "data" should be given its ordinary meaning, as one of ordinary skill in the art of nonvolatile memory would define "data," and that the claims and specification of the '969 patent does not depart from the ordinary meaning of "data," as understood by one of ordinary skill in the art. (CBr at 23-29; RBr at 38-42; SBr at 20-22.) However, respondents argued that the intrinsic evidence, while consistent with the ordinary meaning to a skilled artisan of "data," provides a definition of "data" that is inapposite to the meaning ascribed by the "colloquial use of 'data.'" (RBr at 41-42.)

Referring first to the IEEE Standard Dictionary of Electrical and Electronic Terms,[5] that

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[4] The staff referred to complainant's pre-hearing statement where complainant argued that data should be interpreted to mean "the intended value in a memory cell transistor, including, for example, instructions or command information related to that intended value." (SBr at 20; SPFF 88.)

[5] The Federal Circuit has held that the sequence of steps used in consulting various sources is not important:

> In Vitronics, this court grappled with the [problem of determining

dictionary defines "data" as the following:

> a representation of facts, concepts, or instructions in a formalized manner suitable for communication, interpretation or processing by humans or by automatic means.

(IEEE Standard Dictionary of Electrical and Electronic Terms, Seventh Edition at 267, Institute of Electrical and Electronics Engineers, Inc, Published 2000.)[6] The administrative law judge

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> whether a person of skill in the art would understand the embodiments to define the outer limits of the claim term or merely to be exemplary in nature] and set forth guidelines for reaching the correct claim construction and not imposing improper limitations on claims. The underlying goal of our decision in Vitronics was to increase the likelihood that a court will comprehend how a person of ordinary skill in the art would understand the claim terms. In that process, we recognized that there is no magic formula or catechism for conducting claim construction. Nor is the court barred from considering any particular sources or required to analyze sources in any specific sequence, as long as those sources are not used to contradict claim meaning that is unambiguous in light of the intrinsic evidence. For example, a judge who encounters a claim term while reading a patent might consult a general purpose or specialized dictionary to begin to understand the meaning of the term, before reviewing the remainder of the patent to determine how the patentee has used the term. The sequence of steps used by the judge in consulting various sources is not important; what matters is for the court to attach the appropriate weight to be assigned to those sources in light of the statutes and policies that inform patent law.

(Phillips, 415 F.3d at 1324 (citations omitted) (emphasis added).)

[6] The administrative law judge finds that, although the seventh edition of IEEE Standard Dictionary of Electrical and Electronic Terms was published after 1987, the priority date of the invention-at-issue, viz. the definition of "data" to people with ordinary skill in the art has not changed. Thus, respondents' expert testified:

> Q: And the person of skill in the art in 1987 with respect to the understanding of data is the same as it would be today; is that correct?
> A: In terms of their expertise?

finds that this definition does not limit "data" to any final target memory state of memory being programmed. The administrative law judge also finds that the testimony of complainant's expert Reed infra, on the ordinary meaning of data in the art of nonvolatile memory is consistent with the IEEE Standard Dictionary definition:

> Q. Before we leave the data latching means for storing data term, there's also been discussion of the term "data." How do you construe the term "data" in that term?
>
> A. I was deposed on the subject, and I believe my answer was consistent with everything I heard from Mr. Kanazawa yesterday, and Dr. Quader, that data is the, you can basically call it the fodder of memories. It's what memories do, they store data, and so my concept of data is what comes into the memory to be programmed and what might be subsequently read out from the memory after programming.

(Reed, Tr. at 1048:23-1049:10 (emphasis added).) Hence, based on extrinsic evidence, the administrative law judge finds that the ordinary meaning of "data" is not restricted to the "final target memory states for the cell transistors being programmed," but rather is "what comes into the memory to be programmed and what might be subsequently read out from the memory after programming."

With respect to intrinsic evidence, the following are portions of the asserted claim 1 of

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> Q: No. In terms of their understanding of the term data. Somebody who is skilled in the art in 1987 would have the same understanding of data in this context as somebody would today? It hasn't changed over time, has it?
> A: The analysis would not change, provided we were considering the '969 and '449 patents.

(Subramanian, Tr. at 1915-16 (emphasis added).)

the '969 patent that use the term "data:"

> each of the cell transistors having a control gate, a floating gate, a channel region and an insulation film ... for electrically storing data by using charges stored in the floating gate (JX-4 at 22:59-63);
>
> data latching means for storing data (JX-4 at 23:10-11);
>
> data programming means ... wherein a selected cell transistor is programmed in accordance with data corresponding to the stored data of the data latching means ... the cell transistor holds an injected state of electrons ... when the stored data of the data latching means is a first logic level ... and the cell transistor holds an emitted state of electrons ... when the stored data of the data latching means is a second logic level (JX-4 at 23:12-26);

(emphasis added.) The administrative law judge finds nothing in the claim language, supra, which limits the "term" data to the final target state of the memory being programmed. Thus, he finds that the portion of the claim "for electrically storing data by using charges stored in the floating gate..." merely states that the nonvolatile memory device uses the charges stored in the floating gate to electrically store data, and does not require that the data take the form of the final memory state. The administrative law judge also finds that the portion of claim 1 of the '969 patent:

> "data programming means ... wherein a selected cell transistor is programmed in accordance with data corresponding to the stored data of the data latching means ... the cell transistor holds an injected state of electrons ... when the stored data of the data latching means is a first logic level ... and the cell transistor holds an emitted state of electrons ... when the stored data of the data latching means is a second logic level"

(emphasis added) states that "data" can take the form of a first logic level or second logic level and that while "data" is related to the final target state of the cell transistor (i.e. final target state of the memory), the language does not require that "data" be exactly what is programmed into the

cell transistor (i.e. final target state of the memory). Thus the administrative law judge finds that the claimed language "in accordance with" and "corresponding to" do not restrict the nature of the data to the final target state of the memory, and that all of the other portions of claim 1 of the '969 patent merely require that data be stored electrically and that said other portions of the claim also do not restrict the definition of "data" to the final target memory state of the memory.

Referring to the specification of the '969 patent (JX-4), the administrative law judge finds that references to "data" in the specification of the '969 patent do not limit the definition of data. Thus a representative sampling of portions of the patent specification of the '969 patent that describes the nature of "data" states:

> it should be understood that the memory cell is different from an ordinary memory cell and can store data of four bits (the number of bits corresponds to that of cell transistors having current paths connected in series.) (JX-4 at 4:41-45);
>
> FIG. 3 is a timing chart showing the case where data is sequentially read out from cell transistors CT4 to CT1. More specifically, data is read out from cell transistor CT4 ... from cell transistor CT3 ... from cell transistor CT2 ... from cell transistor CT1 ... Then, data is read out from cell transistor CT1. If data has been programmed as described before... and thus data can be read out from cell transistor CT1 (JX-4 at 5:3-40);
>
> Data is determined depending on whether or not current flows in the selected cell transistor whose gate is set at "0". (JX-4 at 11:5-8);
>
> [describing the programming process including injecting electrons into the floating gates and then performing selective emission] Thus, data can be programmed. (JX-4 at 4:47-68);
>
> Signal X1 is set at a high voltage level in the programming mode, and at this time, potentials of the drains of transistors ST are set at different levels according to the programming data. For example, in a case where electrons are emitted from the floating gate of a

> cell transistor connected to a first one of transistors ST and electrons are injected into the floating gate of a cell transistor connected to the other or second transistor ST, the drain of the first transistor ST is set a high potential and the drain of the second transistor ST is set at a low potential. (JX-4 at 6:63-7:5);
>
> Column decoder 54 generates signals Y1 to Ym to selectively activate column selection MOSFETs Q1 to Qm so that data to be programmed can be supplied to one of memory cell blocks B1 to Bm through data input/output lines IO1 to IO8 or data can be read out from one of the memory cell blocks through the input/output lines. (JX-4 at 9:4-10);
>
> Data to be programmed can be latched in latch circuit 89, and the column lines can be selectively set at high voltage or 0 V according to the latched data for one row of memory cells so that the all memory cells connected to one line of row lines can be programmed. (JX-4 at 12:25-29)

(emphasis added.) The administrative law judge finds that none of those portions, supra, limit the definition of "data" to the final target state of the memory being programmed and that the use of the term "data" in the '969 patent is consistent with the ordinary meaning of "data," as understood by one skilled in the art of nonvolatile memory, viz. information that comes into the memory to be programmed and information that might be subsequently read out from the memory after programming. Hence, in light of the extrinsic and intrinsic evidence and the fact that the intrinsic does not implicitly or explicitly limit the extrinsic evidence, the administrative law judge interprets the term "data" as the information that comes into a memory device, passes through the latch or other circuitry of said memory device, and ultimately is programmed into memory cells.

The administrative law judge finds that the definition that respondents point to in IEEE Standard Dictionary of Electrical and Electronic Terms to support their interpretation of "data" is

labeled "test pattern language" and thus the context of said definition is memory testing, not the storing of data in nonvolatile memory. (RDX-21.) Respondents argued that the expert testimony and documents that complainant referenced to support its argument of the common meaning of "'data" is improper extrinsic evidence which the Federal Circuit had stated is less useful than intrinsic evidence such as the claims of the patent, the patent specification and the patent prosecution history. (RBr at 41-42; Reed, Tr. at 1054:5-15; RX-863C; see also Phillips, 415 F.3d at 1313.) However, reliance on expert testimony and other extrinsic evidence to determine the ordinary meaning of a term that one skilled in the art would understand is part of "those sources available to the public that show what a person of skill in the art would have understood disputed claim language to mean." See Phillips, 415 F.3d at 1314. Moreover the administrative law judge finds that the intrinsic evidence is not in conflict with the extrinsic evidence

Respondents argued that in the context of the '969 patent, "data" has a specific meaning that is different from the "colloquial use of 'data.'" (RBr at 42; Subramanian, Tr. at 1960:16-21, 1962:11-16.) Thus, respondents implicitly argued that even if the ordinary meaning of "data" is not restricted to the final target state of the memory, the context of the '969 patent specifically departed from the ordinary meaning by imposing a restricted meaning of the term "data." Specifically respondents point to both the claims and the specification of the '969 patent as restricting the meaning of "data" to "the final target state of the memory." (RBr at 39-42; RRBr at 29-30.) However, the administrative law judge finds that respondents do not cite any portion, either in the claims or the specification of the '969 patent, that departs from the common meaning of "data" and restricts the meaning to the final target state of the memory being programmed.

Respondents noted in their post-hearing brief that respondents' proposed interpretation for "data" should be given weight because it is exactly the interpretation that this administrative law judge adopted in Certain NAND Flash Memory Circuits, Inv. No. 337-TA-526, Final Init. Determ., slip op. at 21 (Oct. 19, 2005), appeal pending sub nom. SanDisk Corp. v. ITC, Fed. Cir. Docket No. 2006-1187 (docketed Jan. 23, 2006). (RBr at 39, n. 3.) Certain NAND Flash Memory Circuits however is inapposite for the following reasons. First, while it is arguable that the technology is similar in both cases, the asserted patents-in-issue and claims-at-issue were different in Certain NAND Flash Memory Circuits. Second, this administrative law judge's interpretation of data in that case was based on a finding of fact that was undisputed by the parties, and thus, the issue of the proper interpretation of "data" was not before this administrative law judge in that case. Third, respondents have not proffered any analysis of the patents or claims that were asserted in Certain NAND Flash Memory Circuits that would show why this administrative law judge's interpretation in that case has any relevance to the patents-in-issue and claims-in-issue in this case. Finally, as complainant observed, this administrative law judge's interpretation of "data" in that case is not in evidence. (TORPFF1224.)

b. "data programming means"

In issue is the claimed phrase "data programming means" which is found in the following clause of claim 1 of the '969 patent, the only independent claim of the '969 patent:

> data programming means for selectively programming the cell transistors, wherein a selected cell transistor is programmed in accordance with data corresponding to the stored data of the data latching means, the cell transistor holds an injected state of electrons which are injected through the insulation film into the floating gate by utilizing a tunnel effect by the data programming means when the stored data of the data latching means is a first

logic level, and the cell transistor holds an emitted state of electrons which are emitted through the insulation film from the floating gate by utilizing a tunnel effect by the data programming means when the stored data of the data latching means is a second logic level

(JX-4 at 23:12-26 (emphasis added).)

i. function

Complainant, with respect to the recited function for the "data programming means," argued that, based on the testimony of its expert Reed, the function for the "data programming means" in claim 1 of the '969 patent is "for selectively programming the cell transistors." (CBr at 35, 40; TFF 398-400.) It is argued that Reed did not improperly "ignore" a portion of the claim language for the "data programming means" limitation of the '969 patent, but instead focused on the claim language "selectively programming the cell transistors," which comes after the "means for" clause and before the "wherein" clause in claim 1 of the '969 patent. (CBr at 41.) Finally, complainant argued that this interpretation is consistent with the Federal Circuit's decisions in Lockheed Martin Corporation v. Space Systems/Loral, Inc., 324 F.3d 1308, 1315 (Fed. Cir. 2003) and Texas Instruments v. U.S.I.T.C., 988 F.2d 1165, 1171-72 (Fed. Cir. 1993), which held that the proper construction of the recited function of a means-plus-function claim should focus on the language immediately following the "means for" clause, when the claim recites function following that clause but then uses a word such as "whereby" to signal that the remaining language describes the result of the function rather than the function itself." (CBr at 41; TFF 411.)

It is argued that one of ordinary skill in the art would understand "programming" to mean selectively changing the state held by some cell transistors to hold the same state that they were

in prior to programming. (CBr at 36; TFF 401, 402.) Complainant argued that the claims do not include any language that limits "selectively programming" either to injection of electrons into the floating gate or emission of electrons from the floating gate, and instead, that the language is clear in claiming "selectively programming," as provided for in claim 1 of the '969 patent, either by injection or emission, and claim 1 of the '969 patent is "agnostic" as to which of those alternatives should be used. (CBr at 36; CRBr at 23.) Complainant pointed to the Background of Invention section in the specification of the '969 patent and argued that the specification clearly discloses that in EEPROM devices "data can be programmed by injecting or emitting electrons into or from the floating gate via an oxide film." (CBr at 37; CRBr at 23; JX-4 at 1:22-24.) Complainant also argued that the language in said specification further directs the reader to the 1980 Frohman-Benchkowsky reference for more detail on the subject of programming by injection and emission into and from the floating gate, and that said reference specifically describes an embodiment in which injection of electrons into the floating gate is used to accomplish "selectively programming." (CBr at 37; TFF 406.) Finally, complainant pointed to testimony of respondents' expert Pashley to support its argument that, by 1987, it was well understood in the field of nonvolatile memory, and in particular in the subfield of EEPROM devices, that "selectively programming" could be performed either by injection or by emission, and that whether injection or emission was used for "selectively programming," the other could then be used to erase or initialize the cell transistors in advance of programming. (CBr at 37; TFF 405A, 405B.)

Respondents argued that the claimed function is the entire limitation "data programming means ... a second logic level," rather than the truncated phrase "selectively programming the

cell transistors" as complainant's Reed testified; that the "programming" construction is set forth in the specification, which defines it as a two-step process of blanket injection followed by selective emission; that because the claims use the conjunction "and" rather than "or," Toshiba cannot ignore the requirement for selective emission, especially if it would render the claim indefinite; and that the "wherein" clause, which is an integral part of the function, requires a strict relationship between the cell transistor's data and the content of the data latching means. (RBr at 18.)

Respondents argued that at the time the '969 patent was filed, the term "programming" did not have a settled meaning for NAND flash devices. (RBr at 19.) It is argued that Momodomi, an employee of complainant, confirmed that there was no clear definition of "programming" for nonvolatile memory. (RBr at 19; JX-73C at 93:22-94:6.)

Respondents also argued that the intrinsic record shows there are two key requirements to "programming:" (1) "programming" requires a two-step process (blanket injection and selective emission) and (2) "programming requires selective emission." (RBr at 19-24.) Respondents pointed to the claim language of the "data programming means" in claim 1 of the '969 patent to support their argument that "programming" requires both electron injection and emission, rather than just one half of this process. (RBr at 20; RRBr at 23; JX-4 at 23:12-16.) Respondents also pointed to the specification of the '969 patent, specifically Figure 2 of the patent, to support their argument that "programming" requires both injection and emission. (RBr at 21-22, 56-57; RRBr at 21-22; JX-4 at 4:18-20, 5:18-20; RPFF 1001, 1028, 1030, 1389-1391.) Respondents further pointed to the testimony of Reed, complainant's expert, that the '969 patent does not disclose any method of programming other than selective emission to support respondents' argument that

"programming" requires selective emission. (RBr at 23-24; RRBr at 16-17; RPFF 1031, 1034, 1036; RRTFF 396A-H.) Respondents in addition pointed to the specification of the '969 patent, specifically Figure 2, to support their argument that the specification only discloses selective emission structures. (RRBr at 19-21; RPFF 1028.) Additionally, respondents argued that the prosecution history of the '856 patent (from which the '969 patent claims priority) demonstrates that selective injection is a wholly different process and one that was disclaimed during said prosecution. (RRBr at 17-19; RPFF 2166; RRTFF406F, 406K.)

Respondents argued that the claim language of the "wherein" clause of the "data programming means requires that when the latch is equal to the first logic level, the cell transistor must be in an injected state, and when the latch is equal to the second logic level, the cell transistor must be in an emitted state. (RBr at 25-26; RPFF 1082.) Respondents also argued that this strict relationship is also consistent with the specification of the '969 patent, pointing to the language "[the data] to be programmed can be latched in latch circuit 89, and the column lines can be selectively set at high voltage or 0 V according to the latched data for one row of memory cells so that the all memory cells connected to one line of row lines can be programmed." (RBr at 26; RPFF 1083.)

The staff appeared to take no position regarding whether the language within the "wherein" clause recited function. (See SBr at 29-30.) The staff, with respect to the recited function for the "data programming means," did argue that if the administrative law judge found that the language after the "wherein" clause is not part of the function of "data programming means," then no corresponding structure needs to be identified for that language. (SBr at 29-30; SPFF 141.) The staff further argued the language in the "wherein" clause does not require a

strict one-to-one relationship between the state of the data latching means and the cell transistor, but that the final target memory state (injected or emitted) of the cell transistor must be "in accordance with" the logic level (first or second) of the "data latching means." (SBr at 27-29; SPFF 133-139).

Referring to the function of "data programming means," in issue is whether the function is limited to the claimed language "for selectively programming the cell transistors," as complainant argued, or whether the function, as respondents argued, not only includes said claimed language but also includes the wherein clause, viz.:

> "wherein a selected cell transistor is programmed in accordance with data corresponding to the stored data of the data latching means, the cell transistor holds an injected state of electrons which are injected through the insulation film .. when the stored data of the data latching means is a first logic level ... and the cell transistor holds an emitted state of electrons which are emitted through the insulation film from the floating gate ... when the stored data of the data latching means is a second logic level"

(JX-4 at 23:16-26.)

Addressing the wherein clause, the administrative law judge finds that the wherein clause that follows the term "for selectively programming the cell transistors" is part of the recited function of the "data programming means" limitation and is an additional limitation of "selectively programming" because the wherein clause is not merely a result that is inherent to "selectively programming" but instead further defines how the cell transistors are programmed by imposing additional language. See Griffin v. Bertina, 285 F.3d 1029, 1033 (Fed. Cir. 2002) (holding that the wherein clause contained limiting effect to the claimed limitation because it clarified what is required by said claim limitation). The administrative law judge finds that the

plain language of the claim viz. "a selected a cell transistor holds an injected state . . . or an emitted state" corresponding to the stored data of the "data latching means" is not inherent to the programming process and not a mere result of the programming process. Instead, the administrative law judge finds that said language used in the wherein clause clarifies and further defines the term "programming." In other words said language adds additional limitations to the act of programming with respect to the data being programmed into the cell transistors corresponding to the stored data of the data latching means. The administrative law judge finds Lockheed and Texas Instruments, relied on by complainant, are not relevant because in those cases the whereby clauses clearly recited a result inherent to the claimed function rather than a limitation to said function.[7]

Complainant argued that the following testimony of respondents' expert Subramanian is consistent with complainant's position that the wherein clause recited a result and not a function:

> Q. So the structures you've identified as corresponding to the data programming means element, I take it you'd be fair to say that they do selectively program cell transistors, is that correct?
>
> A. Figure 7, 8, and 9, yes, they definitely selectively

---

[7] The administrative law judge notes the row selection means limitation of claims 1 and 4 of the '449 patent has a thereby clause in the following claim language:

> row selection means for applying a signal to one of the first row lines and applying a signal to one of the second row lines in response to a row selection signal, thereby selecting a cell transistor connected to the first row line and a selection transistor connected to one of the second row lines;

(JX-7 at 22:12-17, 24:19-24 (emphasis added).) However complainant argued that said function for the "row selection means" included the thereby clause instead of excluding said thereby clause from the function. (CBr at 46.)

program cell transistors.

Q. And I take it you would agree with me that they do so in a way that the selective cell transistor is programmed in accordance with the data that they provide?

A. That is correct. Otherwise, I would not have selected them as corresponding structure.

Q. And the result of their selective programming is all consistent with the description that follows the wherein clause in this element, is that correct?

A. There is certainly consistency between what they do and what follows the wherein clause. Specifically, within the function, these are the parts that implemented this ... process required by the selectively programming required by the data programming means.

(Subramanian, Tr. at 2001:8 - 2002:8 (emphasis added).) However, the administrative law judge finds that Subramanian in said testimony was not responding to whether the wherein clause recited a result or a function but whether the identified structures implement the limitations called for within the wherein clause.

Inherent in the administrative law judge's finding that the function includes the claimed wherein clause, in issue is the interpretation of certain language within the "data programming means" clause, viz.

> "selectively programming the cell transistors, wherein a selected cell transistor is programmed in accordance with data corresponding to the stored data of the data latching means, the cell transistor holds an injected state of electrons . . when the stored data of the data latching means is a first logic level, and the cell transistor holds an emitted state of electrons . . . when the stored data of the data latching means is a second logic level."

Referring to the plain language of claim 1 of the '969 patent, with respect to the issue of whether programming is a two-step process that requires blanket injection followed by selective emission, as respondents argued, and the issue of whether programming is limited to selective emission, as respondents also argued, the language of said claim 1 does not reference "blanket injection" and does not define programming as requiring blanket injection as a precondition to selective emission. (JX-4 at 23:12-26.) Additionally, the language of claim 1 of the '969 patent only states that it requires injection and emission based on the stored data of the data latching means. The administrative law judge finds that said language does not state whether in "selectively programming," the injection is selective, the emission is selective, or both injection and emission are selective. (JX-4 at 23:12-26.) Notably, the wherein clause of claim 1 of the '969 patent, while requiring both emission and injection based on the stored data of the data latching means, does not require emission to be selective, injection to be selective, or both to be selective. Thus the term "selectively" modifies the term "programming," not the terms "emitted" or "injected." In fact, the specification of the '969 patent never uses the terms "selective injection," "selective emission," "blanket injection," or "blanket emission."

The wherein clause contains the language "the cell transistor holds an injected state of electrons which are injected ... and the cell transistor holds an emitted state of electrons which are emitted..." (JX-4 at 23:16-23 (emphasis added).) Said wherein clause also states that whether programming is done through injection or emission is based whether the stored data of the data latching means is a first logic level or a second logic level. (JX-4 at 23:19-26.) Thus, the administrative law judge finds that the use of said word "and" in claim 1 of the '969 patent restricts the interpretation of programming to require both injection to the floating gate and

emission from the floating gate based on whether the stored data of the data latching means is a first logic level or second logic level. The patentee could have used, but did not use, "or" to express that programming should be interpreted as either injection to the floating gate or emission from the floating gate, but the patentee chose to use the word "and." Hence, the administrative law judge finds that the plain language of claim 1 of the '969 patent requires programming to include both injection into the floating gate and emission from the floating gate based on the stored data of the data latching means.

The Federal Circuit has stated that "[t]here is a "heavy presumption" that the terms used in claims "mean what they say and have the ordinary meaning that would be attributed to those words by persons skilled in the relevant art." SuperGuide Corp. v. DirecTV Enters., Inc., 358 F.3d 870, 873 (Fed. Cir. 2004) (quoting Tex. Digitial Sys., Inc. v. Telegenix, Inc., 308 F.3d 1193, 1202 (Fed. Cir. 2002)). (SuperGuide) The Court went on to state that "claim terms take on their ordinary and accustomed meanings unless the patentee demonstrated an intent to deviate from the ordinary and accustomed meaning of a claim term by redefining the term by characterizing the invention in the intrinsic record using words or expressions of manifest exclusion or restriction, representing a clear disavowal of claim scope." Id. Finally, the Court stated that "the written description, however, is not a substitute for, nor can it be used to rewrite, the chosen claim language." Id. With respect to the prosecution history, the Court stated that "[a]lthough it is correct that the prosecution history is always relevant to claim construction, it is also true that the prosecution history may not be used to infer the intentional narrowing of a claim absent the applicant's clear disavowal of claim coverage." Id. at 875.

In Certain Audio Processing Integrated Circuits and Products Containing Same, Inv. No.

337-TA-538, Com'n Opinion (June 19, 2006) (Certain Audio Circuits), the Commission held that the use of the specification and prosecution history could not be used to trump the plain meaning of the claim language. (Id. at 6-7.) In Certain Audio Circuits, the claim-at-issue contained the following portion: "producing the system clock control signal and the power supply control signal based on a processing transfer characteristic of a computation engine" (Id. at 6 (emphasis added).) The specification provided three instances where only the system clock control signal were produced. (Id. at 7.) Likewise, the prosecution history included an argument by the inventors where they distinguished that power consumption may be optimized by producing the system clock control signal or by producing the power supply control signal. (Id.) However, the Commission concluded that the clear language of the claim required that both the system clock control signal and the power supply control signal be produced stating that "the inventors know how to express adjusting one or the other or both, namely by using the phrase 'and/or' [but] the inventors did not ... use this phrase in the asserted claims, rather the inventors used the conjunctive word 'and.'" (Id. at 11.)

In determining whether programming is a two-step (blanket injection and selective emission process) or whether programming is limited to selective emission, with respect to the specification of the '969 patent, the Background of the Invention section contains the following text in describing data programming in the context of EEPROM with respect to the prior art:

> With a memory cell in the EEPROM, data can be programmed by injecting or emitting electrons into or from the floating gate via an oxide film with a thickness of approx. 100 Å which is extremely thinner than a gate oxide film by use of the tunnel effect.

(JX-4 at 1:22-27 (emphasis added).) Said specification further makes reference to the prior art

U.S. Patent No. 4,203,158, (the '158 patent) by Frohman-Benchkowsky which discloses programming by injection:

> The first commercial floating gate memories employed avalanche injection as a mechanism for transferring charge to the floating gate, thus allowing electrical programming.
>
> * * *
>
> To program the device of FIG. 1, that is, to place a charge on the gate 17, a positive potential of approximately 20 volts is applied to line 27 while lines 26 and 28 are grounded. This potential provides an electrical field across the thin oxide 22 of sufficient magnitude to tunnel electrons from the region 14a to the conductive floating gate 17. (Some electrons will come from the substrate under the thin oxide which surrounds the region 14a.) Sufficient capacitive coupling exists between the gates 17 and 18 such that most of the electric field associated with the potential applied to the gate 18 occurs across the thin oxide layer 22. Once electrons have been tunneled into the gate 17, the threshold voltage of the memory device becomes more positive.

(JX-12 at 1:35-38; 4:32-45 (emphasis added); TFF 406 (undisputed).) Respondents' expert Subramanian also agreed that the Frohman-Benchkowsky reference disclosed programming by injection:

> Q. And are you aware of the type of programming that's reflected in the Frohman-Bentchkowsky article?
>
> A. I believe so.
>
> Q. And does that show programming by injection, selective injection of electrons into the floating gate of EEPROM devices?
>
> A. I believe it does. I don't recall specifically at this time, but that's what the patent language says, so I am going to go ahead and believe it.

(Subramanian, Tr. at 2006:23 - 2007:8 (emphasis added); TFF 406 (undisputed).) Said specification of the '969 patent further contains the following text in describing data programming in the context of EEPROM within the first embodiment of the invention:

> FIG. 2 is a timing chart of various signals in the programming mode in the circuit of FIG. 1. First, signal RE is set to "0" level to turn off transistor 14. At time t0, signals X1 and W1 to W4 are set a high voltage level to inject electrons into the floating gates of cell transistors CT1 to CT4.
>
> * * *
>
> If output signals D1 and D2 of data input circuit 11 are respectively set at "1" and "0" levels when signals W1 to W4 are set to 0 V, transistors 12 and 13 are respectively turned on and off, causing a high voltage from high voltage power source Vpp to be applied to the drain of a corresponding transistor ST so that electrons can be emitted from the floating gate of the respective cell transistors.
>
> * * *
>
> Thus, data can be programmed.

(JX-4 at 4:49-68 (emphasis added).) However, said specification indicates that this is only a preferred embodiment of the invention, and the administrative law judge finds that "selectively programing" is not limited to the limitation of the preferred embodiment. While claims must be construed in light of the specification, Markman, 52 F.3d at 979, limitations from the specification are not to be read into the claims, Comark Communications, Inc. v. Harris Corp., 156 F.3d 1182, 1186 (Fed. Cir. 1998), unless the patentee has demonstrated an intent to deviate from the ordinary and accustomed meaning of a claim term by redefining the term or by characterizing the invention in the intrinsic record using words or expressions of manifest exclusion or restriction, representing a clear disavowal of claim scope. Teleflex, Inc. v. Ficosa N. Am. Corp., 299 F.3d 1313, 1327 (Fed. Cir. 2002). Here, the administrative law judge finds

that the language in claim 1 of the '969 patent and the language in the specification of the '969 patent does not represent the patentee's intent to deviate from the ordinary and accustomed meaning of "programming" to require its programming process to have a preliminary step of blanket injection, or require its programming process to only use selective emission.

The administrative law judge finds that these portions (said Background of the Invention section of the '969 patent and subsequent portions of the specification of the '969 patent as well as the prior art '158 patent referenced by the '969 patent referred to supra) describe data programming through either the injection of electrons into the floating gate or the emission of electrons from the floating gate. The administrative law judge finds that either the process consisting of blanket injection followed by selective emission, or the process consisting of blanket emission followed by selective emission fall within the definition of "programming" as one would understand the claim language and the specification of the '969 patent as long as the data programmed into the cell transistors corresponds to the stored data of the data latching means as defined by the wherein clause of claim 1 of the '969 patent. Hence, the administrative law judge finds that the specification of the '969 patent supports the interpretation that "programming" is not limited to a two-step process consisting of a first step of blanket injection and a second step of selective emission, and that "programming" is not limited to selective emission but that "programming" is:

> changing the charge state of a selected cell transistor through injecting electrons into the floating gate of said cell transistor when the stored data of the data latching means is a first logic level and emitting electrons from the floating gate of said cell transistor when the stored data of the data latching means is a second logic level.

With respect to the prosecution history, the administrative law judge finds that the process of selective injection was not disclaimed during the prosecution of the '856 patent (from which the '969 patent claims priority). The following is the relevant text from the IDS which applicant filed during the prosecution of the '856 patent with respect to Japanese Patent Disclosure, No. 57-71587:

> The assignee advises that this reference discloses a semiconductor memory device including NAND type memory cells as in the present invention. In the memory cells, electrons are released from floating gate into the control gate to allow data to be written. According to the present invention, the writing of data is achieved by releasing electrons from the floating gate into a drain of the memory cell.

(RX-468 at HY0002535 (emphasis added).) As show by the emphasized text, the applicant was not disclaiming selective injection in light of a prior art reference that disclosed selective injection, but instead disclaimed emitting (releasing) electrons from the floating gate to the control gate in light of the prior art reference. Hence, the administrative law judge finds that the prosecution history does not limit the scope of "data programming means" to merely selective emission.

With respect to the relationship between the stored data of the data latching means and the programmed data of the cell transistor, the wherein clause also contains the following language:

> [A] selected cell transistor is programmed in accordance with data corresponding to the stored data of the data latching means, the cell transistor holds an injected state of electrons ... when the stored data of the data latching means is a first logic level .. and holds an emitted state of electrons ... when the stored data of the data latching means is a second logic level.

(JX-4 at 23:14-26 (emphasis added).) The administrative law judge gives the plain and ordinary meaning to the terms "in accordance" and "corresponding" and finds that the data that is programmed into the cell of the transistor must relate to the stored data of the data latching means. The administrative law judge further finds that the relationship is further defined by the wherein clause to mean that when the stored data of the data latching means is a first logic level, the cell transistor must hold an injected state, and when the stored data of the data latching means is a second logic level, the cell transistor must hold an emitted state. The administrative law judge however finds that the claim language is silent as to at what point in the "data programming" process the cell transistor needs to hold either an injected state or emitted state.

With respect to whether the wherein clause requires a strict one-to-one relationship between the stored data in the "data latching means" and the data programmed in the cell transistors, the specification of the '969 patent states that:

> Data to be programmed can be latched in latch circuit 89, and the column lines can be selectively set at high voltage or 0 V according to the latched data for one row of memory cells so that the all [sic] memory cells connected to one line of row lines can be programmed.

(JX-4 at 12:25-29 (emphasis added).) The administrative law judge finds that this portion of the specification of the '969 patent only requires that the cell transistors be programmed according to the latched data in the "data latching means." Thus, he finds nothing in this portion of the specification of the '969 patent which restricts the relationship between the stored data of the "data latching means" and the data programmed in the cell transistors to a one-to-one relationship.

Based on the foregoing, the administrative law judge interprets the function for the "data

programming means" as recited in claim 1 of the '969 patent as:

> "selectively programming the cell transistors, wherein a selected cell transistor is programmed in accordance with data corresponding to the stored data of the data latching means, the cell transistor holds an injected state of electrons which are injected through the insulation film into the floating gate by utilizing a tunnel effect by the data programming means when the stored data of the data latching means is a first logic level, and the cell transistor holds an emitted state of electrons which are emitted through the insulation film from the floating gate by utilizing a tunnel effect by the data programming means when the stored data of the data latching means is a second logic level."

Additionally, the administrative law judge interprets the language "selectively programming the cell transistors [etc.]" of said function as:

> "changing the charge state of a selected cell transistor by: injecting electrons through the insulation film into the floating gate, by utilizing a tunnel effect by the data programming means, so that the cell transistor holds an injected state of electrons, when the stored data of the data latching means is a first logic level; and by emitting electrons through the insulation film from the floating gate, by utilizing a tunnel effect by the data programming means, so that the cell transistors holds an emitted state of electrons, when the stored data of the data latching means is a second logic level."

(emphasis added.)

Complainant argued that claim 1 of the '969 patent does not include any language that limits "programming" either to injection of electrons into the floating gate or emission of electrons from the floating gate, and that the claim language, properly interpreted, demonstrates that programming can be accomplished either by injection or emission of electrons into or from the floating gates of memory cell transistors. (CBr at 36; CRBr at 23.) However, the administrative law judge finds complainant failed to show how the clear and plain use of the conjunction "and" between injection and emission allows for a broad interpretation of "injection

or emission" in accordance with data corresponding to the stored data of the data latching means. Similarly, the administrative law judge finds that complainant failed to show how the proper interpretation allows for both injection to and from the floating gate, and emission to and from the floating gate, where the clear and plain language call only for injection to the floating gate and emission from the floating gate.

Complainant also argued that the specification of the '969 patent clearly discloses that in EEPROM devices "data can be programmed by injecting or emitting electrons into or from the floating gate via an oxide film." (CBr at 37; JX-4 at 1:22-24.) It is argued that the specification of the '969 patent directs the reader to a reference which reference specifically describes an embodiment in which injection of electrons into the floating gate is used to accomplish selective programming, and that combined with the embodiment illustrated in the patent specification that requires

> "a two step process, by first injecting electrons onto the floating gates of all cell transistors being programmed, and then selectively emitting electrons from the floating gates of selected memory cells,"

the specification of the '969 patent supports the broad interpretation of programing as "emitting electrons to or from the floating gate or injecting electrons to or from the floating gate." However, the administrative law judge finds nothing in the intrinsic evidence that requires that the plain meaning of the conjunctive form "and" within the language of claim 1 of the '969 patent be interpreted to mean "and/or." See Super Guide Corp. and Certain Audio Circuits, supra.

Respondents argued that the text of claim 1 of the '969 patent requires the following link between the state of the cell transistors and the content of the data latch, viz. when the latch

equals a first logic level, then the cell transistor is in an injected state and when the latch equals a second logic level, then the cell transistor is in an emitted state. (RBr at 26.) Respondents also argued that the strict relationship is also consistent with the specification because the specification states that the "[d]ata to be programmed can be latched in latch circuit 89, and the column lines can be selectively set at high voltage or 0 V according to the latched data for one row of memory cells so that the all memory cells connected to one line of row lines can be programmed." (RBr at 26; RPFF 1083.) However, as found supra, the specification merely states that the data to be programmed can be latched in the latch circuit 89 and does not impose a one-to-one relationship that the stored data in the data latching means must match the programmed data in the cell transistors at all times of the "data programming" process.

Respondents argued that the '969 patent teaches that "programming" involves a two step process of electron injection and emission and that these two concepts do not occur separately according to the intrinsic evidence, and instead are two integral steps of the same "programming" operation. (RBr at 20.) Thus respondents first argued that claim 1 of the '969 patent requires a two step process because of the claim language that calls for "an injected state of electrons which are injected..." and "an emitted state of electrons which are emitted." (RBr at 20.) However, as found supra, merely because the claim calls for a cell transistor to hold both an injected state of electrons and an emitted state of electrons based on the stored data of the data latching means does not require "programming" to mean "blanket injection followed by selective emission." Respondents also argued that the specification confirms their argument by using "programming" to describe this two step process of blanket injection followed by selective emission, and to indicate that a cell is programmed only after the completion of the selective emission step.

However, as found supra, the two-step process of blanket injection and selective emission is a limitation that is found within the specification, not the claim. The administrative law judge finds nothing in the plain language of the claim which limits programming to blanket injection and selective emission. Respondents also argued that complainant's expert Reed conceded under oath that electron injection in Figure 2 between t0 and t1 is an integral part of the of the '969 patent programming operation:

> Q. In fact, you took the position that the t0 to t1 erasure was part of programming; isn't that correct?
>
> A. I don't recall taking that position. Show me what I said.
>
> Q. May I have Mr. Reed's deposition at page 30, line 20, through page 31, line 1.
>
> Question: So does that tell you that, during the period of t0 to t1, the patentee is referring to erasure as programming?
>
> Answer: The timing chart of figure 2 where he says the timing chart of various signals in the programming mode basically describes the overall operation of programming, yes.
>
> Question: Okay. So the patent also discloses injection as a form of programming; is that correct?
>
> Answer: In my opinion, both injection and emission are part of programming of the cell in the patent.
>
> Question: And that's shown in figure 2, correct?
>
> Answer: That's correct.
>
> * * *
>
> A. Okay. And what I said was, in my opinion both

> injection and emission are part of the programming. And in the patent that means that, as part of the programming, they're all erased by injection. And then they're emitted to selectively program them to the opposite state. So in that sense injection and emission are part of the programming process of the patent.

(Reed, Tr. at 1311:16 - 1312:13, 1314:22 - 1315:4 (emphasis added).) However the administrative law judge finds that Reed never characterized the electron injection step between t0 and t1 in Figure 2 as an "integral part of the patent's programming operation", but instead that injection and emission are merely part of the programming process of the '969 patent, which is consistent with the language of claim 1 of the '969 patent.

Respondents, in addition, argued that it was clear from the intrinsic evidence that the claimed "programming" only means selective emission and not selective injection. (RBr at 23.) Respondents pointed to Reed's "admission in his 'final answer' that the word 'programming' within the patent claim means selective emission:"

> [JUDGE LUCKERN:] Again, the question is: Just so we're crystal clear, this is your final answer, both injection and emission are part of programming as disclosed in the '969 and '449 patents, correct?
>
> THE WITNESS: In terms of reading the claim, the word programming within the claim only finds emission in the patent.
>
> BY MR. CORDELL:
>
> Q: Another way of saying that is that the structures disclosed in the patent only do emission as programming, correct.
>
> A: That's what I just said.

(Reed, Tr. at 1316:9-20.) However, as found supra, the written description of the specification cannot be used to rewrite chosen claim language. Thus, the administrative law judge finds that

the statement of complainant's expert Reed that the structures disclosed in the '969 patent only use emission to "program" does not limit the clear language of the claim that calls for both injection and emission.

Respondents further argued that the '969 patent does not disclose a single embodiment that can program by selective injection, and that neither complainant, nor Reed, ever offered a structure that can program through selective injection. (RBr at 23-24; RPFF 1031-1038.) However, as found supra, the '969 patent does disclose in the Background of the Invention section that programming is done by either injection or emission, and the patent references prior art that discloses programming by injection. Respondents also argued that the asserted claims are in means-plus-function format and the proper construction of data programing means is limited to the structures disclosed in the patents and equivalents thereof. (RRBr at 16-17; RPFF 1031-1034, 1036; RRTFF 396A-H.) Respondents further argued that there is no corresponding structure for selective injection in the '969 patent. However, in claim 1 of the '969 patent, the claimed function, as found supra, is not to selectively inject and to selectively emit, but to "selectively program" through emission and injection. Thus, the issue of whether or not the '969 patent disclosed corresponding structure for selective injection does not resolve the question of identifying and interpreting the function of the "data programming means" because the claim language does not include "selective injection" but merely "selectively programming."

ii. structure

Complainant argued that its expert Reed properly identified transistor 81 as a corresponding structure for the "data programming means" in embodiments that use the latch of Fig. 18A of the '969 patent rather than the entire circuit of Fig. 18A. (CBr at 42.) It is argued

that transistor 81 is the means for the function of "selectively programming the cell transistors" (claim 1 of the '969 patent) because when a latch such as that illustrated in Fig. 18A of the '969 patent is included in an embodiment of the Iwahashi circuit patents, data is loaded from the I/O pins into latches corresponding to potentially thousands of each cell transistors, and each column line can be selectively set at high voltage or low voltage according to the latched data in each latch, and when all of the latches are loaded, programming of all the cell transistors in a row or other grouping can occur simultaneously simply by opening transistor 81 and allowing the appropriate voltage to be applied selectively to each of the column lines, in accordance with the data latched in the latches. (CBr at 42-43; TFF 341, 341A, 343, 408, 409, 411, 413; JX-4 at 12:25-29.)

Complainant also argued the Federal Circuit specifically has held that not every structure that enables or is necessary for completion of a recited function constitutes corresponding structure, but rather, only the structures that actually perform and are the means for the recited function so qualify. (CBr at 44; CRBr at 32-34, TFF 4198; see RDX-1008 and citing; Asyst Technologies, Inc. v. Empak, Inc. 268 F.3d 1364, 1369-74. (Fed. Cir. 2001). Complainant further argued that limiting the corresponding structures to transistor 81 is appropriate because it does not include corresponding structure for other elements in the '969 patent (such as the latch, column line, selected row in low state and selection transistor). (CBr at 45; CRBr 32-34.)

Complainant further argued that the specification confirms that transistor 81 triggers "the programming mode" when programming is done using a latch, and, alternatively, ends that mode and permits initiation of the "reading mode." (CRBr at 30; JX-4 at 12:13-16.)

Respondents argued that the parties' experts agree that circuit 10 in Fig. 1 of the '969

patent, along with its alternative embodiments shown in Figures 7, 8 and 9 of the '969 patent, are alternative corresponding structures for the "data programming means." (RBR at 28.) Respondents also argued that said four structures, as their expert Subramanian explained, are the only circuits clearly linked to the properly interpreted claimed function. (RBr at 28; RPFF 1107; RDX-12; RDX-23.) In support, respondents argued that this conclusion was evident from the specification of the '969 patent. (RBr at 28-29; RPFF 1107-1109.)

The staff, relying only on complainant's prehearing statement, agreed with complainant that the "data programming means" corresponding structures are in Figs. 7, 8, and 9 of the '969 patent and transistor 81 of Fig. 18A of said patent. (SBr at 26.)[8]

In issue is whether any of the following structures are corresponding structures for the "data programing means" function: programming circuit 10 of Figure 1 of the '969 patent, the circuit in Figure 7 of the '969 patent, the circuit in Figure 8 of the '969 patent, the circuit in Figure 9 of the '969 patent, or transistor 81 in Figure 18A of the '969 patent. Figure 1 shows a programming circuit and readout circuit according to a first embodiment of the invention. (JX-4 at 4:4-7.) Figure 7 shows a second construction of the data programming circuit 10 in the circuit of Figure 1. (JX-4 at 6:17-19.) Figure 8 shows a third construction of data programming circuit 10 in the circuit of Figure 1. (JX-4 at 7:43-44.) Figure 9 shows a fourth construction of data programming circuit 10 in the circuit of Figure 1. (JX-4 at 7:67-68.) Figure 18A is a circuit diagram that illustrates a latch circuit connected to a column line, through a transistor, and a booster circuit connected to said column line. (See JX-4 at 12:9-13.)

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[8] As indicated supra complainant in its posthearing submission only argued that transistor 81 was the corresponding structure for the "data programming means"of claim 1 of the '969 patent.

The administrative law judge finds that programming circuit 10 of Figure 1, the circuit in Figure 7, the circuit in Figure 8, and the circuit in Figure 9 are not corresponding structures for the "data programming means" for claim 1 of the '969 patent because those structures do not make use of the latch circuit 89 of Figure 18A of the '969 patent and the use of the "data latching means" for the "data programming means" is required to practice claim 1 of the '969 patent. Transistor 81 however makes use of the latch circuit 89 of Figure 18A of the '969 patent. Thus, the issue that remains is whether merely transistor 81 is appropriate corresponding structure or whether the entire circuit of Figure 18A of the '969 patent is the appropriate corresponding structure for the "data programming means" of claim 1 of the '969 patent.

The following paragraph is the only paragraph in the specification of the '969 patent where transistor 81 is described:

> Further, it is possible to connect a latch circuit shown in FIG. 18 to each column line (the drain of selection transistor ST). In this case one end of MOSFET 81 and input and output terminals of booster circuit 82 are connected to each column line. The gate of MOSFET 81 is connected to receive signal LA/PR which is set at "1" level in the latching operation and programming mode, and set at "0" level in the read mode. The other end of MOSFET 81 is connected to an output terminal of CMOS inverter 85 constituted by P-channel MOSFET 83 and N-channel MOSFET 84 and an input terminal of CMOS inverter 88 constituted by P-channel MOSFET 86 and N-channel MOSFET 87.

(JX-4 at 12:9-21 (emphasis added).) In the same paragraph of the specification of the '969 patent, the following section addresses "programming:"

> Data to be programmed can be latched in latch circuit 89, and the column lines can be selectively set at a high voltage or 0V according to the latched data for one row of memory cells so that the all memory cells connected to one line of row lines can be programmed.

(JX-4 at 12:25-29 (emphasis added).) The administrative law judge finds that said paragraph of the specification of the '969 patent is the entire extent of discussion of transistor 81 as it relates to "data programming means".

Based on the specification of the '969 patent, as shown infra, the administrative law judge finds that said specification does not clearly link the transistor 81 to the recited function of the "data programming means" of claim 1 of the '969 patent because it does not disclose transistor 81 as having, on its own, the components necessary to generate a sufficient voltage to facilitate injection of electrons to the cell transistor or emission of electrons from the cell transistor, whereas said specification does so clearly link the data programming circuit 10 of Fig. 1, and the circuits as shown in Figs. 7, 8 and 9 by disclosing the components necessary to generate sufficient voltage to facilitate injection or emission of electrons.

The administrative law judge finds further that the specification of the '969 patent discloses the necessary structure within the data programming circuit 10 of Fig. 1 and the circuits shown in Figures 7, 8 and 9 to facilitate programming, while the specification fails to disclose this necessary structure within transistor 81 of Fig. 18A. Said specification describes the components of data programming circuit 10 shown in Figure 1 and the components of the alternative constructions of data programming circuit 10 as shown in Figures 7, 8 and 9 and describes how the individual portions of the data programming circuit are connected to power sources Vcc and Vpp, how the individual portions of the data programming circuit are interconnected, and how the individual portions of the data programing circuit are connected to the selection transistor ST so that it can generate sufficient voltage to the selection transistor ST to facilitate either injection of electrons to the floating gate, or emission of electrons from the

floating gate. (JX-4 at 4:9-68, 6:17-7:5, 7:42-66, 7:67-8:60.)

The administrative law judge finds that the specification of the '969 patent discloses the necessary structure to facilitate injection or emission of electrons and sufficiently links the programming circuit 10 of Figure 1 to the recited function of "data programming means." Said specification describes that the data programming circuit 10, as shown in Figure 1, is constituted by input circuit 11 and N-channel MOSFETs 12 and 13; that the gate of MOSFET 12 is connected to high voltage power source Vpp; that MOSFET 13 is connected to node N1; and that node N1 is connected to selection transistor ST. (JX-4 at 4:9-23.) The specification goes on to describe how those components of the data programming circuit 10 of Fig. 1 facilitates programming:

> FIG. 2 is a timing chart of various signals in the programming mode in the circuit of FIG. 1. First, signal RE is set to "0" level to turn off transistor 14. ... If output signals D1 and D2 of data input circuit 11 are respectively set at "1" and "0" levels when signals W1 to W4 are set to 0 V, transistors 12 and 13 are respectively turned on and off, causing a high voltage from high voltage power source Vpp to be applied to the drain of a corresponding transistor via transistor 12 and selection transistor ST so that electrons can be emitted from the floating gate of the respective cell transistors. ... Thus, data can be programmed.

(JX-4 at 4:49-68 (emphasis added).)

The administrative law judge further finds that the specification of the '969 patent discloses the necessary structure to facilitate injection or emission of electrons and sufficiently links the data programing circuit of Figure 7 to the recited function of "data programming means." Said specification describes that the data programming circuit, as shown in Figure 7, is constituted by MOSFETs 25, 26, 28, 29, 30, 31 and 32; that the programming data Din is

supplied to CMOS inverter 27 formed of P-channel MOSFET 25 and N-channel MOSFET 26; that the N-channel MOSFET 28 is connected to power source Vcc, that the P-channel MOSFET 29 is connected to power source Vpp; that MOSFET 28 is connected to P-channel MOSFET 30 and N-channel MOSFET 31; that MOSFET 30 is connected to the power source Vpp; that MOSFET 30 is connected to MOSFET 31; that MOSFET 31 is connected to MOSFET 32; that a connection node between MOSFETs 30 and 31 is connected to MOSFET 29 and MOSFET 33; and that MOSFET 33 is connected to node N1. (JX-4 at 6:17-46.) Said specification also discloses that:

> With the above construction, signal PR is set at "1" level in the data programming mode to turn on MOSFET 33. In this case, high voltage Vpp is generated from data programming circuit 10 when input data Din is at "1" level, and a signal of a level equal to the threshold voltage Vth of MOSFET 32 is generated as programming data when input data Din is at "0" level.
>
> * * *
>
> For example, in a case where electrons are emitted form the floating gate of a cell transistor connected to a first one of transistors ST and electrons are injected into the floating gate of a cell transistor connected to the other or second transistor ST, the drain of the first transistor ST is set at a high potential and the drain of the second transistor ST is set at a low potential.
>
> * * *
>
> As shown in Fig. 7, if the drain of transistor ST which is set at a low potential to inject electrons into the floating gate is connected to the ground terminal through MOSFET 32, the above described problem will not occur.

(JX-4 at 6:47-7:26 (emphasis added).)

The administrative law judge finds the specification of the '969 patent discloses the necessary structure to facilitate injection or emission of electrons and sufficiently links the data

programing circuit of Figure 8 to the recited function of "data programming means." Said specification also states that the data programming circuit, as shown in Figure 8, performs the substantially same operation as the data programming circuit shown in Figure 7 and only differs from the data programming circuit shown in Figure 7 in the following ways: depletion type MOSFET 34 is used as a load instead of P-channel MOSFET 30, and a plurality of diode connected MOSFETs 32-1 to 32-n are provided where the number of MOSFETs 32-1 to 32-n is determined by a designed output level. (JX-4 at 7:42-66.)

Finally, the administrative law judge finds that the specification of the '969 patent discloses the necessary structure to facilitate injection or emission of electrons and sufficiently links the data programing circuit of Figure 9 to the recited function of "data programming means." Said specification describes the data programming circuit shown in Figure 9 is constituted by MOSFETS 35 - 47, 49, and 50 - 51; that the inverted signal !Din[9] of data Din is supplied to the gates of P-channel MOSFET 35 and N-channel MOSFET 36, that the MOSFET 37 is connected to both MOSFET 35 and power source Vcc; that MOSFET 35 is connected to MOSFET 36; that a connection node between MOSFETS 35 and 36 is connected to MOSFET 38; that MOSFET 39 is connected to power source Vcc; that the connection node between MOSFETS 35 and 36 is connected to MOSFET 39; that MOSFET 40 is connected to power source Vpp; that MOSFET 39 is connected to MOSFET 40; that MOSFET 39 is connected to MOSFETS 41 and 42; that MOSFET 41 is connected to the power source Vpp; that MOSFET 41 is connected to MOSFET 42; that the connection node between MOSFETS 41 and 42 are

[9] The "!" refers to the notation of the "-" that is above "Din" in the '969 patent. See e.g. JX-4 at 8:1.

connected to MOSFETS 40 and 43; that MOSFET 43 is connected to power source Vpp; that MOSFET 43 is connected to MOSFET 44; that MOSFET 44 is connected to MOSFET 45; that data !Din is supplied to an input terminal of CMOS inverter 48 including P-channel MOSFET 46 and N-channel MOSFET 47; that an output signal of CMOS inverter 48 is supplied to P-channel MOSFET 49 and N-channel MOSFET 50; that MOSFET 49 is connected to power source Vcc; that MOSFET 49 is connected to MOSFET 51; that MOSFET 49 is connected to MOSFET 50; that a connection node between MOSFET 49 and MOSFET 50 is connected to MOSFET 52; that a connection node between MOSFET 49 and MOSFET 50 is connected to MOSFET 44; and that the connection node between MOSFET 43 and MOSFET 44 is connected to node N1. (JX-4 at 7:67-8:46.) Said specification also discloses that:

> With this construction, the same operation as that of the circuit shown in FIGS. 7 and 8 can be attained.
>
> * * *
>
> Therefore, high voltage Vpp is generated from data programming circuit 10 when input data !Din is at "0" level, and a signal at a level equal to the threshold voltage Vth of MOSFET 45 when input data Din is at "1" level.

(JX-4 at 8:47-61 (emphasis added).)

In contrast, the administrative law judge finds that the specification of the '969 patent does not disclose the necessary structure to facilitate injection or emission of electrons and does not sufficiently link transistor 81 of Figure 18A to the recited function of "data programming means." Said specification describes that transistor 81, as shown in Figure 18A, is merely connected to the latch circuit 89 and to each column line (i.e. selection transistor ST); that the gate of MOSFET 81 is connected to receive signal LA/PR; and that the other end of MOSFET 81

is connected to an output terminal of CMOS inverter 85 which is constituted by P-channel MOSFET 83 and N-channel MOSFET 84, and an input terminal of CMOS inverter 88, which is constituted by P-channel MOSFET 86 and N-channel MOSFET 87. (JX-4 at 12:9-21.) Said specification does not describe transistor 81 as consisting of any connections to power source Vpp or power source Vcc, and instead relies on the latch circuit 89 and the booster circuit 82 for connections to either Vpp or Vcc.

In addition, in referring to the data programing circuit 10 of Figure 1, the specification of the '969 patent clearly identifies the circuit as the "data programming circuit." (JX-4 at 4:9.) Likewise, in referring to Figures 7, 8, and 9, said specification identifies the structures shown as "[other constructions] of data programming circuit 10 in the circuit of FIG. 1." (JX-4 at 6:17-18, 7:43-44, 7:67-68 (emphasis added).) In contrast, said specification only identifies transistor 81 as MOSFET 81, and does not use an identification such as "data programming transistor 81" or data programming MOSFET 81." (JX-4 at 12:9-21.)

Based on the foregoing, the administrative law judge finds that the specification of the '969 patent does not clearly link transistor 81 of Figure 18A of the '969 patent to the recited function of the "data programming means" of claim 1 of the '969 patent. See Braun Medical, Inc. v. Abbott Laboratories 124 F.3d 1419 (Fed. Cir. 1997) where the Court, in affirming the district court's judgment of non-infringement, stated:

> Section 112, paragraph 6 states that a means-plus-function claim "shall be construed to cover the corresponding structure ... described in the specification." (emphasis added). We hold that, pursuant to this provision, structure disclosed in the specification is "corresponding" structure only if the specification or prosecution history clearly links or associates that structure to the function recited in the claim. This duty to link or associate structure to

> function is the quid pro quo for the convenience of employing § 112, ¶ 6. See O.I. Corp. v. Tekmar Co., 115 F.3d 1576, 1583, (Fed.Cir.1997). Our holding in this regard is also supported by our precedent stating that claims drafted in means-plus-function format are subject to the definiteness requirement of the patent law: [I]f one employs means-plus-function language in a claim, one must set forth in the specification an adequate disclosure showing what is meant by that language. If an applicant fails to set forth an adequate disclosure, the applicant has in effect failed to particularly point out and distinctly claim the invention as required by the second paragraph of section 112.
>
> In re Donaldson Co., 16 F.3d 1189, 1195, ... (Fed.Cir.1994) (in banc); see also In re Dossel, 115 F.3d 942, 946-47, ... (Fed.Cir.1997); 35 U.S.C. § 112, ¶ 2.

Id. 124 F.3d at 1424-25 (emphasis added). In Omega Engineering, Inc. v. Raytek Corporation 334 F. 3d 1314 (July 2003), the Court, referring to Braun, stated:

> Once the functions performed by the claimed means are identified, we must then ascertain the corresponding structures in the written description that perform those functions. Id. A disclosed structure is corresponding "only if the specification or the prosecution history clearly links or associates that structure to the function recited in the claim." B. Braun Med., Inc. v. Abbott Labs., 124 F.3d 1419, ... (Fed.Cir.1997). In other words, the structure must be necessary to perform the claimed function. Northrop Grumman Corp. v. Intel Corp., 325 F.3d 1346, 1352, ... (Fed.Cir.2003).

Id. 334 F.3d at 1321. See also Medtronic, Inc. v. Advanced Cardiovascular Systems, Inc. 248 F.3d 1303, 1311 (Fed.Cir. 2001); Default Proof Credit Card System, Inc. v. Home Depot U.S.A. Inc. 412 F.3d 1291, 1298. (Fed. Cir. 2005).

Moreover, the administrative law judge finds that transistor 81 cannot perform the "data programming means" function as the administrative law judge has interpreted said function. As found supra, the "data programming means" function requires injecting electrons into the floating gate of said cell transistor when the stored data of the data latching means is a first logic level

and emitting electrons from the floating gate of said cell transistor when the stored data of the data latching means is a second logic level. As the specification states, a high voltage needs to be applied to the cell transistor to facilitate either injecting electrons into the floating gate or emitting electrons from the floating gate:

> If output signals D1 and D2 of data input circuit 11 are respectively set at "1" and "0" levels when signals W1 to W4 are set to 0V, transistors 12 and 13 are respectively turned on and off causing a high voltage from high voltage power Vpp to be applied to the drain of a corresponding transistor via transistor 12 and selection transistor ST so that electrons can be emitted from the floating gate of the respective cell transistors.

(JX-4 at 4:56-64 (emphasis added).)

However, the administrative law judge finds nothing in the specification of the '969 patent which shows that transistor 81 has the capacity of providing the necessary voltage for programming as described by the specification. Transistor 81, by itself, has no connection to a high voltage Vpp necessary to program a selected cell transistor. Instead, transistor 81 is only connected to data latch circuit 89, which itself, only has a connection to Vcc, which is not sufficient voltage to program the cell transistor. (Subramanian, Tr. at 1775:13-25; Reed, Tr. at 1340:23-1341:10.) It is, in fact, booster circuit 82 (as shown in Figures 18A and 18B) that contains the connection to voltage Vpp'. (JX-4 at 12:32-43.) Thus, the administrative law judge finds that at a minimum, any alternative corresponding structure must include booster circuit 82, because without booster circuit 82, and its Vpp' connection, transistor 81 will never be able to generate the necessary voltage and apply it to the drain of a cell transistor so that the cell will be able to emit electrons as described in the specification.

With respect to the necessary voltage for programming, complainant's expert Reed

testified that transistor 81 required other structures to perform the recited function of data programming means:

Q. So lets look at 18A. Let's assume for the moment that all we have in figure 18A is transistor 81. You have no latch which is designated in the drawing as 89. And you have no booster circuit, which is designated in the drawing as 82. Isn't it a fact, Mr. Reed, that under those circumstances, nothing would ever get programmed into the cell transistors?

A. Under that hypothetical construction, you're right. No booster circuit, no latch, no program.

* * *

Q. All right. Now I'm going to give you the latch. And assume that the structure – and I'll circle – I'll put a square around what I'll call case B on figure 18A of RDX-1007. So the structure is now the latch and transistor 81. Isn't it a fact, Mr. Reed, that this structure B will not program any of the cell transistors?

A. Not as disclosed. A similar structure could if modified. But as disclosed, no, it could not.

Q. Did you say no, it could not?

A. Not – not this hypothetical, without the booster circuit.

Q. In fact, the output of what I've marked here as structure B, which would be the latch with transistor 81, could never exceed VCC; isn't that correct?

A. That's correct. In your hypothetical's construct, with VCC as the only supply to the shown circuit, nothing else on the column line other than transistor 81, no programming could occur.

* * *

Q. We've got transistor 81. We know we need that structure. We know we need a latch. We know we need a booster circuit. Isn't a fact sir, merely putting a high voltage at the end of the column line as shown in 18A will never program a cell transistor?

* * *

A. Well, you need the selected first row line in a low state at 0 volts.

* * *

Q. ... But isn't it a fact that I need the structure of the intervening column line to transmit the high voltage from the output of the booster circuit to the cell transistor that's actually going to be programmed?

* * *

A. There's definitely a column line. That's part of the claim recitation.

Q. But more importantly, sir, I have to have that column line to deliver the high voltage necessary to program the cell transistor, correct?

A. I believe that's – goes without saying, or I would have thought so.

* * *

Q. So I not only need the column line that connects 18A to a particular cell, which I'll circle, but I also need the selection transistor in order to take the high voltage from the booster circuit and deliver it to the cell transistor, correct?

A. That's correct.

(Reed, Tr. at 1339:15-25, 1340:10-1341:10, 1344:3-7, 1344:18-19, 1344:9-13, 1345:17-23 (emphasis added).) Thus, the administrative law judge finds that Reed testified that the transistor 81, by itself, is incapable of programming a selected cell transistor, and instead requires the following structures: a data latch (latch circuit 89 in Figure 18A), a booster circuit (booster circuit 82 in Figures 18A and 18B), a row line (not shown in Figure 18A), a column line (depicted in Figure 18A) and a selection transistor (not shown in Figure 18A).

Additionally, Reed testified that transistor 81 was similar to a transistor found within the entire corresponding structures identified in Figures 7, 8 and 9 of the specification of the '969 patent, yet he designated the entire circuits of Figures 7, 8 and 9 while only designating transistor 81 from the circuit shown in Figure 18A:

> Q. So I'm a little curious, Mr. Reed. You originally identified figure 7 as one embodiment of the programming means, correct?
>
> A. That's right.
>
> * * *
>
> Q. And you showed the entirety of figure 7 in the upper-right hand corner [of CDX-140-6]; isn't that right?
>
> A. That's right.
>
> Q. And by the same token, you showed the entirety of figure 8; isn't that right?
>
> A. That's right.
>
> Q. But when it came to figure 18A, you designated only transistor 81, correct?
>
> A. Well, that's right.

Q. But when we look at figure 7, isn't it a fact that transistor 33 does exactly the same thing that transistor 81 does in figure 18?

A. It could be construed as such. However, figure 7 doesn't – isn't required to also be interpreted along with a latching means that's part of figure 18A.

Q. And in fact you have another transistor 33 in figure 8 that does exactly the same thing as transistor 81 in figure 18, correct?

A. It looks to be a transistor that can be considered that way, yes.

Q. But you didn't designate either transistor 33 in figure 7 or transistor 33 in figure 8 as your data programming means, correct?

A. I listed them as alternative structures to the data programming means claim element.

Q. But, again, sir, you listed the entirety of the figure as shown here in CDX-140-6. And then — for figure 7 and 8, but were very clear that it was only transistor 81 in figure 18A, correct?

A. That's correct.

(JX-4 at 1337:6-19, 1338:8-1339:14 (emphasis added).)

Because transistor 81 cannot perform the recited function of the "data programming means" limitation of claim 1 of the '969 patent, and because the specification fails to clearly link transistor 81 to the recited function of the "data programming means" limitation of claim 1 of the '969 patent, the administrative law judge finds transistor 81 cannot be the corresponding structure for the data programming means. Instead, because the recited function of the "data programming means" limitation of claim 1 of the '969 patent requires booster circuit 82 to

supply the requisite Vpp to selectively program the cell transistors and data latch circuit 89 to supply the requisite Vcc to selectively program the cell transistors (see supra), the administrative judge finds that the entire Figure 18A structure is necessary to suffice as a corresponding alternative structure for the recited function of the "data programming means" limitation of claim 1 of the '969 patent.

Complainant argued that by positioning transistor 81 between the latched data and column line, and by associating that transistor with the label "LA/PR," the signal that triggers programming from the latch, just as the PR signals associated with transistor 33 in FIGS. 8 and 9 and the PR signal associated with transistor 52 in Fig. 9 trigger programming from those latch-less structures, Fig. 18A itself links transistor 81 to the function of "selectively programming the cell transistors." (CBr at 29-30.) Complainant further argued that the specification confirmed that transistor 81 triggers "the programming mode" when a programming is done using a latch, and alternatively, ends that mode and permits initiation of the "reading mode." (CRBr at 30; JX-4 at 12:13-16.) However, the administrative law judge finds that merely associating transistor 81 with the label "LA/PR" is insufficient for linking transistor 81 to the recited function of "data programming means" because it is not merely the signal LA/PR that is necessary to facilitate injection or emission of electrons, but it is, inter alia, the production of sufficient voltage. Additionally, the fact that transistors 33 in Figs. 7 and 8, and transistor 52 in Fig. 9 are associated with the PR signals does not show that labeling transistor 81 "LA/PR" links transistor 81 with the recited function of "data programming means" because it was not transistors 33 and 52 of Figs. 7, 8 and 9 that served as the corresponding structures, it was the entire circuits shown in Figs.7, 8 and 9.

Complainant argued that when a latch such as the latch shown in Figure 18A is included in an embodiment of the '969 patent, data is loaded from the I/O pins into said latch and each column line can then be selectively set at a high voltage or low voltage according to the latched data in each latch. (TFF 341, 341A, 343; JX-4 at 12:25-29.) It is argued that when all of the latches are loaded, programming of all the cell transistors in a row or other grouping can occur simultaneously simply by opening transistor 81 and allowing the appropriate voltage level to be applied selectively to each of the column lines, in accordance with the data latched in the latches. (TFF 341, 341A, 343, 409, 411.) Complainant also argued that transistor 81 uses voltage Vcc from the latch to cause the application of the high voltage necessary to create the high field needed to effect programming by Fowler-Nordheim tunneling. (CRRFF1146L.) Complainant further argued that the initiation of the coupling between the latch and the column line performs the recited "data programming means." (CRRFF1146M.) However, the administrative law judge finds that "initiation of the coupling between the latch and the column line" is not sufficient to perform the recited function for the data programming means because the function of "data programming means," inter alia, is to inject electrons into the floating gate of the cell transistor and emit electrons from the floating gate of the cell transistor, and that injection or emission requires a voltage Vpp to be applied to the cell. (Subramanian, Tr. at 1775; Reed, Tr. at 1339-40.) The fact that transistor 81 can be opened to allow sufficient voltage to be applied to the appropriate column line is not sufficient for only transistor 81 by itself to be the corresponding structure as transistor 81 has no way on its own of generating the sufficient level of voltage. (Id.)

Complainant also argued that even if additional structures, including the "latch," "booster circuit," "selected row in low state," "column line," and "selection transistor" are "needed for"

programming to occur using the latch of Fig. 18A, this fact is not relevant to, and certainly not determinative of, whether transistor 81 is proper or sufficient corresponding structure (CBr at 44; CRBr at 32-33), citing Asyst Technologies for the argument that the Federal Circuit has held that not every structure that enables or is necessary for completion of a recited function constitutes "corresponding structure," but rather, only the structures that "actually perform" and are the "means for" the recited function so qualify. (CBr at 44; CRBr at 32-33.) Complainant further argued that some of the additional structures, such as the latch, column line, selected row in low state, and selection transistor, are more appropriately identified as corresponding structure for other elements of the '969 patent, and, thus, it would be inappropriate to include those structures as part of the corresponding structure for the "data programming means" element (CBr at 45; TFF 416-419); and that while the booster circuit 82 does not appear to be a corresponding structure for any other limitation of the asserted claims, it supplies power to enable the pertinent structures to operate, but it does not actually perform the recited function of selective programming. (CBr at 45-46.)

As found supra, the booster circuit and the data latch do not merely enable transistor 81 to perform the recited function of selectively programming the cell transistors, because the data latch provides voltage Vcc and the booster circuit provides voltage Vpp and both of which are necessary to program a selected cell transistor. Thus, the administrative law judge finds that since the additional structures of Fig. 18A actually perform the recited function instead of merely enabling transistor 81, Asyst is inapposite to this case.

c. "connected to each of the column lines"

Claim 1 of the '969 patent states "data latching means for storing data, connected to each

of the column lines"[10] (JX-4 at 23:10-11(emphasis added).) Complainant argued that the language "connected to each of the column lines" describes a structural feature not function, and therefore is not part of the recited function of the "data latching means." (CBr at 30.) Thus, complainant argued that the use of means-plus-function claim interpretation is not called for in interpreting "connected to each of the column lines." (CBr at 30.) Complainant also argued that the language of the limitation "appears relatively straightforward and can be interpreted without further construction."

Complainant, in addition, argued that, as complainant's expert Reed explained, the language used in the claim is clear on its face and would permit one latch to be connected to two or more column lines, as long as each of the column lines is connected to a latch. (CBr at 30; TFF 387.) Complainant further argued that no technical expertise is required to understand that if two or more column lines are independently connected to a single latch, then it is proper English usage to say that the latch is connected "to each of the column lines." (CBr at 30-31.)

Complainant argued that its expert Reed did not testify that two structures are "connected" whenever there is a "metaphysical connection" or mere possibility of an electrical connection (CBr at 19-20); that in Reed's testimony on the Cioaca reference, which is relied on by respondents in challenging the validity of the '969 and '449 patents under 35 U.S.C. § 103, Reed explained that a latch or buffer that terminates at a control gate is not connected to

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[10] There is no issue as to the function and structure of "data latching means." Thus, the parties agree that the function of "data latching means" is "to store data". (CBr at 29; TFF 357; RBr at 38; RPFF 1219.) Also the parties agree that the corresponding structure of "data latching means" is latch circuit 89 of Fig. 18A of the '969 patent. (CBr at 29; TFF 357, 358; RBr at 42; RPFF 1273; SBr at 22; SPFF 104.) In addition the parties only disagree on the interpretation of "data."

structures beyond that gate, because an electrical connection cannot be made simply by turning on the transistor. (CBr at 20; TFF 1733; TRRPFF 5629.) It is argued that respondents are simply wrong in asserting that under Reed and the staff's construction "every transistor in Figure 10 would be 'connected' to every other transistor," because there plainly are many transistors in FIG. 10 of the '969 patent that are not "connected" under Reed's ordinary meaning construction of that term, including for example the ST1 and the QD transistors, because there is not an "electrical path" between them. (CBr at 20; TFF 385.)

Respondents argued that, as Subramanian opined, "connected to each of the column lines" is a structural limitation that requires that there must be one "data latching means" for every one column line, and that there must be a direct electrical connection between the "data latching means" and the column line during programming. (RBr at 43; RPFF 1279.)

Respondents also argued that the asserted claims of the '969 patent require that there be a one-to-one relationship between the latching means and the column line and that this one-to-one relationship is unmistakable from the plain text of this limitation: "data latching means for storing data, connected to each of the column lines" (RBr at 44; RPFF 1280); that the phrase "connected to each of the column lines" modifies the term "data latching means for storing data," therefore requiring that the data latching means be what is connected to each of the column lines (RBr at 44; RPFF 1281); and that the "data latching means" in question is not a multiplicity of latches but instead, the corresponding structure of the "data latching means" is just one latch 89. (RBr at 44; RPFF 1282.)

Respondents argued that claim 1 of the '969 patent does not leave to chance the number of column lines connected to latch 89, but rather specifically requires a single "column line" by

using the term "each", citing Microstrategy v. Inc. v. Business Objects, S.A., 429 F.3d 1344, 1350-51 (Fed. Cir. 2005). (RBr at 44; RPFF 1283.) Respondents also argued that connecting a single latch to each and every one of the column lines is correct because it comports with the patent teachings that "it is possible to connect a latch circuit shown in FIG. 18 to each column line (the drain of selection transistor ST) so that one row of memory cells so that the all memory cells connected to one line of row lines can be programmed," and the "advantage of having a latch connected to each column" permits programming of all column lines in a single cycle, unlike the embodiment that does not have a latch on each column line." (RBr at 44; RPFF 1284, 1286, 1287.) Respondents further argued that because its interpretation specifically covers the teachings of the patent, it is the correct interpretation. (RBr at 45.) Respondents in addition argued that complainant's use of Reed's testimony to redraw Figure 18A of the '969 patent to connect latch 89 to both an odd and even bitline sought to create written disclosure in the patent where there was none, was an improper use of expert testimony, and was contrary to the '969 patent. (RBr at 45; RPFF 1288.)

Respondents argued that the limitation that requires the "data latching means" to be "connected" to a column line cannot denote a physical joining of a column line to one of the latch's nodes, because such a construction could not read onto the disclosed embodiment in Figure 18A of the '969 patent where connecting transistor 81 stands between latch 89 and the column line (RBr at 46; RPFF 1308); that one of ordinary skill in this art instead would read the limitation as referring to a direct electrical connection between the data latching means and the column line (RBr at 46; RPFF 1309); and that while transistor 81 is off during the reading operation, it is turned on during the entire programming operation which is at the heart of the

asserted claims. (RBr at 46; RPFF 1310.) Respondents further argued that when it is on, transistor 81 becomes a conductive wire between the latch and the column line that establishes a direct electrical connection between the latch and its column line (RBr at 46; RPFF 1311); that under this condition, a "tagged" electron could pass between the column line and the latch completely unperturbed at any time during the programming operation (RBr at 46; RPFF 1312); and that this interpretation covers the disclosed embodiment and stays true to the understanding of the person skilled in this field, and thus, demonstrating that it is the correct interpretation. (RBr at 46; RRBr at 32.)

The staff argued that the limitation "connected to each of the column lines" is not a means-plus-function limitation and as such needs no finding of function or corresponding structure. (SBr at 22; SPFF 105.) It is argued that respondents' proposed construction of "connected to each of the column lines" that requires one "data latching means" for each column line and that the "data latching means" must be directly connected to the column line" imparts unnecessary limitations that are not found in the claim language. (SBr at 22-23; SPFF 106, 108.) The staff argued that the term "connected to each of the column lines" should be interpreted consistently with its plain and ordinary meaning to mean "at least one data latching means directly or indirectly connected to each of the column lines (SBr at 23; SPFF 109); and that one of respondents' two proposed limitations, i.e. "directly," is inconsistent not only with the ordinary meaning of the unmodified word "connected," which allows for intervening elements, but also with the claim language and specification, including the embodiment (illustrated in Fig. 18A) that discloses a "data latching means" connected to a "column line" through an electrical connection including an interposed transistor (LA/PR.) (SBr at 23; SPFF 111.) The staff also

argued that respondents' other proposed limitation, i.e. "one latching means for each column line", is improper because it is clear that an electrical connection allows one element of a circuit to be connected to "each of" many other elements. (SBr at 23; SPFF 112.)

The administrative law judge finds that the ordinary meaning of the language "data latching means for storing data, connected to each of the column lines" found in claim 1 of the '969 patent allows for a one-to-many relationship between the "data latching means" and the column line. (JX-4 at 23:10-11.) Thus he finds that the patentee's use of the plural term "column lines" manifests the patentee's intention for the presence of multiple column lines.[11] The administrative law judge further finds that the ordinary meaning of the language "each of" means one or more. Hence, the administrative law judge finds that the use of the language "each of the column lines" can mean one or more column lines. Thus, he finds that the ordinary meaning of the language "data latching means connected to each of the column lines" signifies a one-to-many relationship, and means "one data latching means connected to one or more column lines."

The administrative law judge also finds that the following language in the specification of the '969 patent supports this interpretation:

> Further, it is possible to connect a latch circuit shown in FIG. 18 to each column line (the drain of selection transistor ST). In this case, one end of MOSFET 81 and input and output terminals of booster circuit 82 are connected to each column line.

(JX-4 at 12:9-13 (emphasis added).) Thus the specification states that the latch circuit shown in Fig. 18A of the '969 patent is connected to "each column line." (JX-4 at 12:9-10.) Since the

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[11] The administrative law judge finds that the patentee also manifests this intent by using the term "a memory cell array compromising memory cells ... having ... rows lines and column lines. (JX-4 at 22:55-57.)

'969 patent makes clear the presence of two or more column lines by the use of the plural term "column lines" in the "memory cell array" limitation of claim 1 of the '969 patent, the administrative law judge finds that the specification states that latch circuit 89 of Fig. 18A is connected to all of the one or more column lines. (JX-4 at 22:57.) Similarly the specification supra states that one end of MOSFET 81 and input and output terminals of booster circuit 82 are connected to "each column line." (JX-4 at 12:11-13.) The administrative law judge also finds that this use of the language "each column line" is consistent with the meaning supra that MOSFET 81 and booster circuit 82 are connected to all of the two or more column lines. Finally, the administrative law judge finds that if the patentee intended to require a one-to-one correspondence between the data latch and the column line, the patentee knew how to disclose this because the specification in describing Figure 31 discloses a one-to-one relationship between a plurality of series circuits 100 and a plurality of columns lines:

> Each of series circuits 100 is connected at one end to a corresponding one of column lines C1 to Cp through E-type MOSFET 134.

(JX-4 at 15:47-49 (emphasis added).) Thus, the administrative law judge finds that because the patentee did not use similar language in describing the nature of the connection between the data latching means and each of the column lines, the patentee did not intend to impose a one-to-one restriction on the relationship. For the foregoing reasons, the administrative law judge interprets "connected to each of the column lines" to allow for a data latching means to be connected to multiple column lines.

With respect to the issue of whether the electrical connection is required to be direct, the claimed language "data latching means ... connected to each of the column lines," is silent as to

whether there must be a direct electrical connection between the "data latching means" and each of the column lines (i.e. no intervening structures that can affect the electrical connection between the "data latching means" and each of the column lines) or whether there can be an indirect electrical connection between the "data latching means" and each of the column lines (i.e. intervening structures that can affect the electrical connection between the "data latching means" and each of the column lines.) (JX-4 at 23:10-11.) However, the administrative law judge finds the specification of the '969 patent discloses a preferred embodiment where the data latch circuit 89 is indirectly connected to each column line through the intervening structure transistor 81 even though said specification describes this as "connecting a latch circuit shown in Fig. 18A to each column line." (JX-4 at 12:9-10.) Furthermore, the administrative law judge finds that Fig. 18A clearly shows that transistor 81 is interposed between the data latch circuit 89 and the column line. (JX-4.) Additionally, the administrative law judge finds other sections of the specification of the '969 patent that describes two structures as being connected, yet there is a third intervening structure between the two structures:

> As shown in FIG. 7, if the drain of transistor ST which is set at a low potential to inject electrons into the floating gate is connected to the ground terminal through MOSFET 32, the above-described problem will not occur. (JX-4 at 7:22-26);
>
> One end of series circuit 100, or the drain of cell transistor MC1 is connected to programming voltage source Vpp of high voltage, for example; 20 V though enhancement type (E-type) MOSFET 101 for application of programming voltage (JX-4 at 12: 61-65);
>
> FIG. 27 shows a circuit model in which the drain of MOSFET 120 is connected to voltage source VD through load circuit 121, and the source thereof is connected to the ground terminal. (JX-4 at 13:60-63);

> Each of series circuits 100 is connected at end to a corresponding one of column lines C1 to Cp through E-type MOSFET 134. (JX-4 at 15:47-49);
>
> Column lines C1 to Cp are connected commonly to data programming/readout node 136 through respective column selection E-type MOSFETs 32... (JX-4 at 15:57-60);
>
> Node 136 is connected programming voltage source Vpp through programming voltage applying E-type N-channel MOSFET 137... (JX-4 at 15:64-66);
>
> Node 136 is also connected to data detection node 140 through potential isolation E-type MOSFET 139... (JX-4 at 15:68-16:2)
>
> [N]ode 154 connected to voltage source Vcc through P-channel MOSFET 153... (JX-4 at 17:53-55);
>
> [N]ode 167 connected to voltage source Vcc through P-channel MOSFET 166... (JX-4 at 18:18-19);
>
> [T]he other end of each series circuit 100 is connected to the ground terminal through MOSFET 190... (JX-4 at 19:47-48)

(emphasis added.) Thus, the administrative law judge interprets "connected to each of the column lines" to allow for electrical connections through intervening structures.

For the foregoing reasons, the administrative law judge finds that a person of ordinary skill in the art would interpret "data latching means ... connected to each of the column lines" to mean "data latching means directly electrically connected, or indirectly electrically connected through intervening structure, to one or more column lines."

Respondents argued that the use of the term "each" in the "data latching means" phrase of claim 1 of the '969 patent makes clear that the patent requires that one column line be connected to each "data latching means" citing Microstrategy, 429 F.3d at 1350-51. (RBr at 44; RPFF 1283.) However, the claim language of a completely different patent in Microstrategy cannot

supercede the claim language and the specification of the '969 patent. Additionally, in Microstrategy, 429 F.3d at 1350, the phrase-in-issue was "wherein each user device subscribed to that service is associated with a device-specific style." There, the placement of "each user device" at the front of the phrase and the use of the term "device-specific" supported the Court's finding that the claim language required association of output devices with a device-specific style on an individual device-by-device basis. (Id.) Here the "data latching means" is placed before "each of the column lines" thus focusing the connection between the "data latching means" and all of the column lines. (JX-4 at 10-11.) Additionally, there is no additional language similar to "device-specific" in claim 1 of the '969 patent that implies a one-to-one relationship.

Respondents argued that a one-latch-to-one-column line is necessary to implement the disclosed embodiment. (RBr at 44.) Respondents further argued that the '969 patent teaches "it is possible to connect a latch circuit shown in Fig. 18 to each column line (the drain of selection transistor ST)" so that "one row of memory cells so that the all memory cells connected to one line of row lines can be programmed." (RBr at 44; RPFF 1286.) Respondents thus argued that the '969 patent teaches that the "advantage of having a latch connected to each column" permits programming of all column lines in a single cycle, unlike the embodiment that does not have a latch on each column line. (RBr at 44; RPFF 1287.) Respondents in addition, argued that a one-latch-to-one-column-line relationship is essential to the disclosed ability to program every cell transistors in the same row in one cycle. (RRBr at 32; RRTFF 387A-C; CDX 139-3.) Respondents argued that "accordingly," respondents' proposed interpretation squarely reads onto the disclosed embodiment and respondents' interpretation of "connected to each of" adopts the meaning ascribed by the '969 patent.

The administrative law judge finds that the fact that respondents' claim interpretation reads on the disclosed embodiment is not dispositive that respondents' claim interpretation should be adopted. The administrative law judge also finds that the text in the specification of the '969 patent "the column lines can be selectively set ... according to the latched data for one row of memory cells so that the all memory cells connected to one line of row lines can be programmed" does not describe an advantage germane to the invention as a whole that limits the scope of the claim "connected to each of the column lines" to a one-to-one relationship, but instead, describes an advantage of the disclosed embodiment. Thus, the administrative law judge finds that the limitation that the advantage is predicated on is specific to the disclosed embodiment and should not be read into the claim language.

Respondents argued that complainant's use of Reed's testimony to redraw Figure 18A to connect latch 89 to an odd and even bitline improperly sought to create written disclosure in the patent where there was none. (RBr at 45; RPFF 1288.) Respondents further argued that the '969 patent does not teach how to implement today's odd/even column lines or select transistors, as Reed admitted under cross-examination. (RBr at 45; RPFF 1289.) However, regardless of Reed's testimony, the administrative law judge finds that the specification clearly describes how to connect a latch circuit to each column line: "one end of MOSFET 81 and input and output terminals of booster circuit 82 are connected to each column line." (JX-4 at 12:11-13 (emphasis added).) The administrative law judge finds that the claim language does not limit the number of column lines that the "data latching means" is connected to. Thus, whether there is only one column line, or whether there are multiple column lines, the administrative law judge finds that the specification describes that one end of transistor 81 and the input and output terminals of

booster circuit 82 must be connected to each column line. (JX-4 at 12:11-13 (emphasis added).)

Respondents argued that one of ordinary skill in the art would read the limitation "data latching means ... connected to one of the column lines" as referring to a direct electrical connection between the data latching means and the column line. (RBr at 46; RPFF 1309.) However the administrative law judge finds that Reed's testimony disputed respondents' contention that one of ordinary skill in the art would add an additional "direct electrical connection" limitation. (Reed, Tr. at 1047:7-17.) Respondents also argued that their claimed interpretation would cover the disclosed embodiment in Figure 18A of the '969 patent because transistor 81 is turned on during the entire programming operation, and when it is on, transistor 81 becomes a direct electrical connection between the latch and the column line, thus allowing a "tagged electron" to pass between the column line and the latch completely unperturbed during the programming operation. (RBr at 46; RPFF 1310-1312.) However the administrative law judge finds no language either in claim 1 or the specification of the '969 patent that adds a limitation that the "data latching means" and the column lines are only connected during the programming operation. The administrative law judge further finds that the disclosed embodiment showing an intervening structure, transistor 81, between data latch 89 and the column line in Fig. 18A, supports the administrative law judge's interpretation of "connected to one of the column lines" that allows for electrical connections through intervening structures.

Respondents argued that complainant expert Reed's interpretation of "connected" of "an electrical path possible between the points that are connected" would render the entire limitation meaningless because every transistor in Figure 10 of the '969 patent would be "connected" to every other transistor, and any latch linked to one column line would be "connected" to all of the

other column lines in the array without regards to how remote the latch is from those lines. (RBr at 46-47; RRBr at 31.) However, the administrative law judge finds that the entire limitation is not rendered meaningless because there still must be an electrical connection between the data latching means and the column line, as demonstrated in Figure 18A of the '969 patent.

Respondents also argued that by requiring a direct electrical connection, respondents' proposed interpretation is the only interpretation that stays true to the specification's teaching that "it is possible to connect a latch circuit shown in Fig. 18A to each column line." (RBr at 47; RPFF 1315.) It is argued that complainant's proposed interpretation would disregard the importance of connecting the latch circuit to the electrical drain of the ST transistor, which permits programming of all column lines in a single cycle. (RBr at 47; RPFF 1316.) However, as found supra, the text in the specification "the column lines can be selectively set ... according to the latched data for one row of memory cells so that the all memory cells connected to one line of row lines can be programmed" does not describe an advantage germane to the invention as a whole that limits the scope of the claim "connected to each of the column lines" to a one-to-one relationship, but instead, describes an advantage of the disclosed embodiment, whose limitation should not be read into the claim language. Additionally, the administrative law judge finds that respondents have not shown how complainant's proposed interpretation disregards the importance of connecting the latch circuit to the electrical drain of the ST transistor.

d. "row selection means"

In issue is the claimed phrase "row selection means" which is found in independent claim 1 of the '969 patent, the only asserted independent claim of the '969 patent. (JX-4 at 23:3.)

i. function

Complainant argued that the recited function for the "row selection means" limitation of claim 1 of the '969 patent is "designating one of the rows of the memory cells in response to a row selection signal." (CBr at 46.) It is argued that the method of identifying the function for a means-plus-function element by identifying the appropriate language actually recited in the claim is completely consistent with Federal Circuit precedent, particularly since complainant's proposed language is understandable to one of ordinary skill in the art. (CBr at 46-47.)

Respondents argued that the function of the "row selection means" is to place in an operable state a single set of cell transistors commonly connected to the same row line, by generating and applying a row selection signal. (RBr at 52; RPFF 1355.)

The staff argued that the "row selection means" limitation should be interpreted consistently with complainant's proposed construction. (SBr at 31-32; SPFF 150, 152.)

The administrative law judge finds that the language of the "row selection means" limitation of claim 1 of the '969 patent, viz. "row selection means for designating one of the rows of the memory cells in response to a row selection signal" makes clear that the function of the "row selection means" is to "[designate] one of the rows of the memory cells in response to a row selection signal." (JX-4 at 23:4-6.) In other words, the "row selection means" must respond to a "row selection signal" by "designating" one of the "rows of the memory cells."

In issue, as to the recited function, are the phrases "one of the rows of the memory cells," "designating," and "in response to a row selection signal."

Complainant argued that the term "one of the rows of the memory cells" on its face refers to the "memory cell array" limitation of the claim, which describes "rows" of memory cells, and it is unnecessary for the administrative law judge to craft language to describe the relationship

between those two limitations and to incorporate limitations of one into the other. (CRBr at 35.)

Respondents argued that the "row selection means" limitation requires the selection and designation of "one of the rows of the memory cells." (RBr at 52.) Respondents also argued that according to the "memory cell array" limitation of claim 1 of the '969 patent, the cell strings (i.e., the "memory cells" composed of "cell transistors connected in series") are "arranged in matrix form having rows and columns and row lines and column lines, ... the control gates of the cell transistors in the same row being commonly connected to one of the row lines. (RBr at 52; RPFF 1357.) Thus, respondents argued that the plain language of the claim dictates that a "row" of a memory cell is a set of cell transistors whose control gates are 'commonly connected" to the same row line. (RBr at 52; RPFF 1358.)

Respondents further argued that the claim language is very clear that the "row selection means" must designate "one of the rows of the memory cells." (RBr at 53; RPFF 1360.) Respondents, in addition, argued that by using the plain term "one of," the limitation imposes a singularity requirement, so that the "row selection means" can only select one row of memory cell transistors. (RBr at 53.)

Respondents also argued that the phrase "designating ... in response to" should be interpreted to mean the selected row of cell transistors is placed in an operable state by being "designated" through the generation and application of a row selection signal; and that its interpretation was "in harmony" with the specification, which indicates that "[r]ow decoder 53 generates signals X1, X2. ..., signals W11, W12, ..., W1n, and signals W21, W22, ... W2n to select a row line or lines in the memory cell array." (RBr at 53; RPFF 1362-64.) Respondents further argued that the "row selection means" limitation and the "column selection means"

limitation both use the phrase "designating ... in response to," and thus the phrase" designating ... in response to" should receive the same interpretation that respondents argued for the "column selection means," infra. (RBr at 53.)

Respondents argued that complainant's expert Reed agreed with respondents' expert Subramanian at trial that "designating" required generating and applying a row selection voltage. (RRBr at 35-36; RRTFF 428E.) The staff, while agreeing with complainant that the "row selection means" limitation should be interpreted consistently with complainant's proposed construction, viz. "designating one of the rows of the memory cells in response to a row selection signal," which is the function recited in the claim, agreed with respondents that only one of the rows of the memory cells must be selected. (SBr at 31-32; SPFF 150, 152.)

With respect to the phrase "one of the rows of the memory cells," the administrative law judge finds that the "memory cell array" limitation of claim 1 of the '969 patent defines the "one of the rows of the memory cells" by the following language of said claim 1:

> a memory cell array comprising memory cells arranged in matrix form having rows and columns and row lines and column lines ... each of the cell transistor having a control gate ... and the control gates of the cell transistors in the same row being commonly connected to one of the row lines.

(JX-4 at 22:55 - 23:3 (emphasis added).) Additionally, in the context of the entire "row selection means" limitation, the administrative law judge finds that a "row of the memory cells" must be a singular entity that the "row selection means" is capable of designating, because the function of the row selection means is, inter alia, to designate "one of the rows of the memory cells." (JX-4 at 23:4-5.) The specification of the '969 patent makes clear that a row of the memory cells, as defined by the memory cell array limitation of claim 1 of the '969 patent is capable of being

designated:

> Row decoder 53 generates signals X1, X2, ... signals W11, W12, ... W1n and signals W21, W22, ... W2n to select a row line or lines in the memory cell array.
>
> * * *
>
> [T]he data programming operation is effected with respect to the memory cells connected to data line X1 of memory cell block Bm. At the time of programming, signals X1 ... are set at a high voltage level. In this condition, signals W11 to W1n are set to a high voltage level ... Then, signals W1n to W11 are sequentially set to "0" level in this order. In this case, electrons are emitted only when the control gate voltage is at "0" level ... and thus data can be programmed in the respective cell transistors.

(JX-4 at 9:1-4, 20-34 (emphasis added).) From the '969 patent specification, the administrative law judge finds that "one of the rows of the memory cells," can be designated by the "row selection means" to be programmed.

For the foregoing reasons, the administrative law judge interprets "one of the rows of the memory cells" to mean "the memory cells whose control gates are commonly connected to the same row line."

With respect to the term "designating," the administrative law judge finds that the term "designating" read in the context of the claim language of claim 1 of the '969 patent and the specification of the '969 patent, is given its ordinary meaning and thus he interprets "designating" to mean "to indicate and set apart for a specific purpose." (Webster's Collegiate Directory, Tenth Edition.) The administrative law judge finds that the specification of the '969 patent supports this interpretation:

> Row decoder 53 generates signals X1, X2, ... signals W11, W12, ... W1n and signals W21, W22, ... W2n to select a row line or lines in

the memory cell array.

(JX-4 at 9:1-4 (emphasis added).) Here, the context of the passage is data programming the semiconductor memory device formed by arranging memory cells in a matrix form consisting of rows and columns. In this context, the row decoder generates and applies a signal that corresponds to one of the rows that is to be programmed:

> [T]he data programming operation is effected with respect to the memory cells connected to data line X1 of memory cell block Bm. At the time of programming, signals X1 ... are set at a high voltage level. In this condition, signals W11 to W1n are set to a high voltage level ... Then, signals W1n to W11 are sequentially set to "0" level in this order. In this case, electrons are emitted only when the control gate voltage is at "0" level ... and thus data can be programmed in the respective cell transistors.

(JX-4 at 9:20-34 (emphasis added).) The administrative law judge finds that said portion of the specification makes clear that by row decoder 53 applying a signal X1, setting X1 to a high voltage level, setting W11 to a high voltage level, and then setting W11 to a "0" level, when programming data is supplied from the data programming means, row decoder 53 has designated row W11 as opposed to the other rows (e.g. W12, ... W1n). The administrative law judge also finds that those portions of the specification do not limit the term "designating" to "generating and applying a signal" and thus the claim should not be limited to a preferred embodiment, especially in light of the claim language of claim 1 of the '969 patent, that uses the term "designating" as opposed to "applying a signal."

With respect to the term "in response to a row selection signal," the administrative law judge finds that the term "in response to a row selection signal" of claim 1 of the '969 patent does not identify which signal is the row selection signal. Thus the specification of the '969

patent discloses that row decoder 53 "generates signals X1, X2, ..., signals W11, W12, ..., W1n, and signals W21, W22, ... W2n to select a row line or lines in the memory cell array." (JX-4 at 9:1-4.) The '969 patent also discloses row decoder 53 and signals X1, X2, W11, W12, W1n, W21, W22 and W2n in Figure 10 of the '969 patent. (JX-4.) Complainant's Reed also testified that one of ordinary skill in the art would have the sufficient knowledge necessary to design a row decoder to perform the function of the "row selection means:"

> Well, as I said before, Mr. Iwahashi had to be considering the row decoder 53 was something that one of ordinary skill could design without having to be told how to do so by the inventor.

(Reed, Tr. at 1447.)

In Amtel Corporation v. Information Storage Devices, Inc., 198 F.3d 1374 (Fed. Cir. 1999), the Federal Circuit stated how 35 U.S.C. § 112, ¶ 2[12] applies in the specific context of a means-plus function claim limitation:

> [T]he "one skilled in the art" mode of analysis applies with equal force when determining whether a § 112, ¶ 6 means-plus-function limitation is sufficiently definite under § 112, ¶ 2.
>
> * * *
>
> That the "one skilled in the art" analysis should apply in determining whether sufficient structure has been disclosed to support a means-plus-function limitation flows naturally form the relationship between claim construction and § 112, ¶ 2.
>
> * * *

[12] 35 U.S.C. § 112, ¶ 2 states that:

> The specification shall conclude with one or more claims particularly point out and distinctly claiming the subject matter which the applicant regards as his invention.

> [I]n order for a claim to meet the particularity requirements of [§ 112, ¶ 2], the corresponding structure(s) of a means-plus-function limitation must be disclosed in the written description in such a manner that one skilled in the art will know and understand what structure corresponds to the means limitation.
>
> * * *
>
> Fulfillment of the § 112, ¶ 6 tradeoff cannot be satisfied when there is a total omission of structure. There must be structure in the specification. The conclusion is not inconsistent with the fact that the knowledge of one skilled in the particular art may be used to understand what structure(s) the specification discloses...

(Amtel, 198 F. 3d at 1379, 1382 (emphasis added).)

In another Federal Circuit case, S3 Inc. v. nVIDIA Corp., 259 F.3d 1364, 1370 (Fed. Cir. 2001), the issue before the Court was whether a "selector" disclosed as an element of an integrated circuit in the specification of the patent-in-issue was sufficiently disclosed as corresponding structure for the "means ... for selectively receiving" limitation even though the electronic structure of the selector and the details of its electronic operation were not described in the specification. At trial, S3 presented evidence that a selector was a standard electronic component whose structure was well known in the relevant art, and that such standard components were usually represented in the manner shown in the patent-in-issue. S3, 259 F.3d at 1370. The inventor of the patent-in-issue and the expert witnesses testified that persons of skill in the relevant field would readily recognize that the selector shown in the specification was an electronic device whose structure was well known. The Court held that "[t]he law is clear that patent documents need not include subject matter that is known in the field of the invention ... for patents are written for persons experienced in the field of the invention." S3, 259 F.3d at 1371.

For the foregoing reasons, the administrative law judge finds that in view of the

disclosure of row decoder 53 in Figure 10 of the '969 patent, combined with the text of the specification and the expert testimony of Reed as to the knowledge of one ordinary skill in the art, "in response to a row selection signal" should be interpreted as "responding to a signal outside of the row selection means."

Respondents argued that "designating" should be interpreted to mean, inter alia, to place in an operable state. It is argued that the specification frames the act as selection or designation as part of a larger operation, which aims to place the selected memory cells and cell transistors in an operable state. However the administrative law judge rejects this interpretation because the larger operation that respondents refer to is "data programming" which is performed by the "data programming means" not the "row selection means" as demonstrated by the specification:

> Row decoder 53 generates signals X1, X2, ..., signals W11, W12, ... W1n, and signals W21, W22, ... W2n to select a row line or lines in the memory cell array. Column decoder 54 generates signals Y1 to Ym to selectively activate column selection MOSFETS Q1 to Qm so that data to be programmed can be supplied to one of memory cell blocks B1 to Bm through data input/output lines IO1 to IO8 or data can be read out from one of the memory cell blocks through the input/output lines.

(JX-4 at 9:1-8 (emphasis added).)

Respondents also argued that "one of the rows of the memory cells" should be interpreted as "set of cell transistors whose control gates are commonly connected to the same row line." However, the administrative law judge finds his interpretation of "one of the rows of the memory cells" is consistent with the "memory cell array" limitation's definition of "one of the rows of the memory cells," i.e., "memory cell array comprising . . . control gates of the cell transistors in the same row being commonly connected to one of the row lines."

ii. structure

Complainant argued that row decoder 53 from Figure 10 in the '969 patent is a proper corresponding structure. (CBr at 47; TFF 429.) It is argued that no additional structure is needed to designate a row and in particular, there is no need to select among horizontal blocks as part of the row selection process. (CBr at 47.) Complainant further argued that row decoders such as the one schematically represented by row decoder 53 were well known to persons of ordinary skill in the art in 1987, and such a person could design different row decoders to meet the row selection needs of different memory cell arrays. (CRBr at 36; TFF 432-436; TRRPFF 1470.) Complainant argued that complainant's Reed further explained that claim 1 of the '969 patent alternatively could be construed such that row decoder 53 would be used expressly in conjunction with the QT transistors of Figure 17, rather than incorporating the functionality of those transistors, in order to perform the recited function of "designating one of the rows of the memory cells in response to a row selection." (CRBr at 36-37; TRRPFF 1370.) Complainant also argued that Reed identified row decoder 131 of Figure 31 of the '969 patent as the corresponding structure for the "row selection means" to comply with precedent indicating that a proper claim construction should identify all corresponding structure for a means-plus-function limitation. (CRBr at 37.)

Respondents do not dispute that the disclosed corresponding structure that performs the claimed function, under either party's construction, includes row decoder 53 of Figure 10 of the '969 patent. (RBr at 54; RPFF 1369.) Respondents however argued that the structure consisting of the QT transistors of Figure 17 in combination with row decoder 53, and the structure consisting solely of row decoder 131 cannot serve as the corresponding structure for the "row selection means" because neither structure is clearly linked to the claimed function of the "row

selection means." (RBr at 54; RPFF 1370.) It is argued that row decoder 131 is a structure disclosed for the patent's UV-EPROM embodiment, which cannot inject electrons by tunneling or emit electrons electrically as the EEPROM devices can, and thus, one of ordinary skill in the art would understand that the injection and emission of electrons via a "tunnel effect" by the "data programming means" would not include structures used in the UV-EPROM devices. (RBr at 54; RPFF 1371-1372.) Respondents further argued that row decoder 131 is irrelevant because complainant's expert Reed testified that row decoder 131 was "cumulative to row decoder 53." (RBr at 54; RPFF 1373.) Respondents further argued that the modified structure of row decoder 53 with the QT transistors of Figure 17 cannot be a corresponding structure, because it is not disclosed anywhere in the specification. (RBr at 54; RPFF 1374.) Respondents also argued that row decoder 53 combined with the QT transistors of Figure 17 are irrelevant because Reed did not use this combined structure for his infringement analysis for the '969 patent. (RBr at 54; RPFF 1376.)

The staff argued that the structure corresponding to the "row selection means" in the '969 patent includes the QT1/QT2 transistors of Figure 17, in combination with row decoder 53 of Figure 10. (SBr at 33; SPFF 159.) It is argued that the structures of Figure 17 and Figure 10 are linked sufficiently to the function of "row selection means" to represent corresponding structure. (SBr at 33.) The staff agreed with respondents that the row decoder 131 relates to an UVEPROM embodiment that is not incorporated into claim 1 of the '969 patent. (SBr at 32; SPFF 154.) The staff was silent as to whether row decoder 53 is a corresponding structure for the 'row selection means' of claim 1 of the '969 patent.[13]

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[13] Thus the staff argued:

As seen from the foregoing, complainant argued that either row decoder 53, row decoder 53 combined with QT transistors, or row decoder 131 is the corresponding structure for the 'row selection means" of claim 1 of the '969 patent while respondents argued that only row decoder 53 is the corresponding structure for the "row selection means" of claim 1 of the '969 patent. At issue is which interpretation of the corresponding structure of the "row selection means" is the correct interpretation (if any).

With respect to row decoder 53 of Figure 10, the specification states the following:

> Row decoder 53 generates signals X1, X2 ...., signals W11, W12, ... W1n, and signals W21, W22, ... W2n to select a row line or lines in the memory cell array.
>
> * * *
>
> At the time of programming, signals X1, ... are set to a high voltage level. In this condition, signals W11 to w1n are set to a high voltage level to inject electrons into the floating gates of the cell transistors. Then, signals W1n to W11 are sequentially set to "0" level in this order. In this case, electrons are emitted when the control gate voltage is at "0" level, ... and thus data can be programmed in the respective cell transistors.

(JX-4 at 9:1-35 (emphasis added.) Thus, the administrative law judge finds that the specification of the '969 patent indicates that row decoder 53 is the structure that generates a signal which designates which row of memory cell transistors to be programmed by the data programming

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> . . . the structure corresponding to the 'row selection means' in the '969 patent include (1) the QT 1/QT2 transistors of Figure 17, in combination with Row Decoder 53 of Figure 10. The structure corresponding to the "row selection means" in the '449 patent includes Row Decoder 53 of Figure 10. This is different from the '969 patent because in the '449 patent some of the 'row selection' function is performed by the 'second switching means.

(SBr at 33 (citations omitted); SPFF 160.)

means. Hence, the administrative law judge finds that row decoder 53 of Figure 10 of the '969 patent is a corresponding structure for the "data programming means."[14]

With respect to row decoder 53 of Figure 10, combined with the QT transistors of Figure 17, the specification states the following:

> The circuit of FIG. 17 corresponds to one of memory cell blocks B1 to Bm, and includes MOSFETS QT1, QT2, ... which are connected to the control gates of the cell transistors and whose conduction states are controlled by signals X1, X2, ... Since signals are input through MOSFETS QT1, QT2, ... a desired one of the memory cell blocks can be programmed by selectively satisfying a logical condition determined by a combination of signals W11, W12, ... and signals Z2 to Zm supplied to corresponding memory cell blocks to selectively set signals W1n1, ... W121, W111 to a high voltage level.

(JX-4 at 11:59-12:2.) Thus, the administrative law judge finds that the function of the QT transistors is to facilitate the programming of a connected cell transistor within a selected row by either allowing or not allowing a row selection signal (e.g. W111) to pass through to the control gate of said connected cell transistor, depending on whether a row selection signal (e.g. X1) has turned the corresponding QT transistor state on by changing its conductive state. Because said function depends on the row decoder 53 having already designated a particular row of memory cells to be programmed, he also finds that the QT transistors do not perform the recited function of designating one of the row of memory cells. Thus, the administrative law judge finds that row

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[14] The administrative law judge finds that only row decoder 53 is the corresponding structure for the "row selection means" of claim 1 of the '969 patent and not row decoder 53 combined with column decoder 55. While the embodiment of the invention that uses the QT transistors (Figure 17) requires both the row decoder 53 and column decoder 55 to perform the function of the "row selection means," this embodiment is only an optional embodiment because the language of claim 1 of the '969 patent (unlike the language in claims 1 and 4 of the '449 patent) does not recite a limitation that requires the use of the QT transistors. (See Section VII.B.1.c.ii, infra.)

decoder 53 of Figure 10 combined with QT transistors of Figure 17 is not a corresponding structure of the "row selection means."

With respect to row decoder 131 of Figure 31 of the '969 patent, the specification states the following:

> FIG. 31 is a circuit diagram showing a UVEPROM of plural-bit output construction according to another embodiment of this invention. The UVEPROM includes row decoder 131, ...

(JX-4 at 15:37-39.) Thus, the administrative law judge finds that the disclosed structure of row decoder 131 is in the context of the UV-EPROM embodiment of the '969 patent, not in the context of the EEPROM embodiment of the '969 patent, like the other structures disclosed (e.g. row decoder 53.) Thus, the administrative law judge finds that row decoder 131 is not a corresponding structure for the "row selection means."

e. "column selection means"

In issue is the claimed phrase "column selection means" which is found in independent claim 1 of the '969 patent, the only asserted independent claim of the '969 patent. (JX-4 at 23:7.)

i. function

Complainant argued that the recited function for the "column selection means" element of claim 1 of the '969 patent is "designating one of the columns of the memory cells in response to a column selection signal." (CBr at 49; TFF 450.) Complainant argued that this interpretation is consistent with Federal Circuit precedent that, whenever possible, "[t]he function is properly identified as the language after the 'means for' clause" in the claim itself, citing Lockheed Martin, 324 F.3d at 1319 and ACTV, Inc. v. Walt Disney Co., 346 F.3d 1082, 1087 (Fed. Cir. 2003). (CRBr at 39.) It is argued that the "column selection means" limitation of claim 1 of the

'969 patent is relatively simple and stated in a language that one of ordinary skill in the art would have no problem understanding. (CRBr at 39.)

Complainant argued that, unless the claim language would be unclear to one of ordinary skill in the art, the language "define[s] the invention" and should be applied as written, citing Phillips, 415 F.3d at 1312. (CRBr at 40.) Complainant also argued that said rule applies with full force when identifying the function of a means-plus-function limitation, citing ACTV, Inc., 346 F.3d at 1087. (CRBr at 40.)

Respondents argued that complainant generally agrees with the analysis of respondents' expert Subramanian, that the "column selection means" selects a column of memory cells; that "column of memory cells" refers to a set of cell transistors strings which are individually connected to the same column line; that the "column selection means" can only select one "column" of memory cells, i.e. a single set of cell transistors strings which are individually connected to the same column line; and that a person of ordinary skill knows that, during various operations in a nonvolatile memory divide, there is one column line activated for each input-output line. (RBr at 48; TFF 1321-1322.) It is argued that the claimed language, "column selection means for designating one of the columns of the memory cells in response to a column selection signal" of claim 1 of the '969 patent means that the selected column is "selected" or "designated" through the generation and application of a column selection signal on gating transistors, which act in response to this signal. (RBr at 49; TFF 1329-1330.) Respondents also argued that this understanding is consistent with the specification of the '969 patent which closely pairs the application of a signal with the selection or designation of memory cells and memory cell transistors. (RBr at 49; TFF 1331-1336, 1339.) Respondents further argued that the

specification of the '969 patent equates the act of selecting or designating with the application of a signal. (RBr at 50; TFF 1337.) Respondents also argued that the specification frames the act of selection as part of a larger operation, which aims to place the selected memory cells and cell transistors in an operable state. (RBr at 50; TFF 1338.)

Respondents argued that the '969 patent never discloses address selection inputs for the column selection means. (RBr at 50; RPFF 1344.) Respondents further argued that the '969 patent does not disclose any circuitry to generate such incoming column selection signals. (RBr at 50; RPFF 1345-1346.) Respondents also argued that there is no disclosed structure to receive such incoming column selection signals. (RBr at 50-51; RPFF 1347-1348.) Respondents, in addition, argued that complainant's proposed corresponding structure, viz. column decoder 54, cannot select just one column of memory cells; it must select eight columns at a time. (RRBr at 33; RRTFF 450C-L.)

The staff argued that "column selection means" should be interpreted, according to complainant's proposed interpretation, to mean the "column selection means for designating one of the columns of the memory cells in response to a column selection signal" which is the function as cited in the claim. (SBr at 31; SPFF 148.) The staff also argued that "designating" should be interpreted to mean "to mark or point out; indicate; show; specify" which appears to be the ordinary meaning. (SBr at 31.) The staff further argued that it agreed with respondents that the device need to have the ability to select only one of the columns of the memory cell. (SBr at 31.)

The administrative law judge finds that the plain language of the "column selection means" limitation of claim 1 of the '969 patent makes clear that the function of the "column

selection means" is to "[designate] one of the columns of the memory cells in response to a column selection signal." (JX-4 at 23:7-9.) In other words, the "column selection means" must respond to a "column selection signal" by "designating" one of the "columns of the memory cells".

The administrative law judge further finds that the "memory cell array" limitation of claim 1 of the '969 patent identifies the "column of memory cells" as a portion of the matrix of memory cells that are commonly connected to one of the column lines in column format:

> a memory cell array comprising memory cells arranged in matrix form having rows and columns and row lines and column lines ... each memory cell having a first terminal and second terminal, the first terminals of the memory cells in the same column being commonly connected to one of the column lines...

(JX-4 at 22:55-67 (emphasis added).) In the context of the entire "column selection means" limitation, the administrative law judge finds that a "column of the memory cells" must be a singular entity that the "column selection means" is capable of designating, because the function of the column selection means is, inter alia, to designate "one of the columns of memory cells." (JX-4 at 23:7-8.) Thus the specification of the '969 patent includes Figure 10 which shows the construction of a memory device formed by arranging cell transistors from Figure 1 in a matrix form. (JX-4.) Figure 10 details the columns of memory cells, consisting of the memory cell array, and shows that memory cells in the same column are commonly connected to one of the column lines. (JX-4.) Figure 10 also details that each column line is connected one data input/output line of the data programming circuit. (JX-4.) The specification describes the column designation process, in light of the overall programming process, as the following:

> Column decoder 54 generates signals Y1 to Ym to selectively

activate column selection MOSEFTs Q1 to Qm so that data to be programmed can be supplied to one of memory cell blocks B1 to Bm through data input/output lines IO1 to IO8 or data can be read out from one of the memory cell blocks through the input/output lines.

* * *

At the time of programming, signals X1, Ym, Z2 to Zm are set at a high voltage level. In this condition, signals W11 to W1n are set to a high voltage level to inject electrons into the floating gates of the cell transistors. Then, signals W1n to W11 are sequentially set to "0" level in this order. In this case, electrons are emitted only when the control gate voltage is at "0" level and programming data is supplied as a high voltage to the drains through any one of data input/output lines IO1 to IO8, column selection transistor Qm and selection transistor STm, and thus data can be programmed in the respective cell transistors.

(JX-4 at 9:4-34 (emphasis added).) Complainant's expert Reed clarified the relationship between the columns of memory cells, the memory cell blocks, the column decoder, and the data input/output lines with respect to the column designation process and the overall programming process:

Q. Could you just briefly describe what Figure 10 shows, Mr. Reed?

A. Figure 10 of the patent shows a combination of a number of these memory cell strings, a number of memory cell strings arrayed horizontally and also vertically, along with a row decoder to allow the selection of desired row of, row line of cells, along with a column decoder for steering data from the data programming circuits into the appropriate columns for reading and writing the cells.

* * *

Q. Moving quickly, let me ask you to look at the top of Figure 10. There are a number of IO1, IO2 up to

IO8. What does that reflect?

A. IO are generally the conduits for data that enters and leaves the memory. So the data that's to be programmed comes in, for example, in this case, there are eight IO pins in the disclosure, and that means eight parallel bits of data come out of the data programming.

And reading circuits Figure 200 -- I mean, element 200 and are steered down to the appropriate columns by the column decoder 54.

Q. Looking at the bottom of the Figure 10, there are a number of collections of columns that are labeled B1, B2 through BM. What does that reflect?

A. Well, that goes into that issue that I was referring to before of the horizontal segmentation of these devices as disclosed in Figure 10. But let's see, basically, in the disclosure in each of these B1, B2 to BM groups, there are groups of eight columns, and the disclosure, this drawing and embodiment allows the separate programming of each, of the columns on each one of those eight groups.

Q. And why are there eight columns, what do they correspond with?

A. Eight columns happens to be the same number of pins there are on the IO pins that come from the data programming circuit 200 and also happens to be the number of bits in a byte.

(Reed, Tr. at 1022:24 - 1025:2 (emphasis added).) From the '969 patent specification and Reed's expert testimony, the administrative law judge finds that a memory cell block is a set of columns, where the number of columns that consist of a memory cell block is equal to the number of data input-output lines (e.g. in Figure 10, there are eight columns per memory cell block because there are eight data input-output lines); that the "column selection means" can only designate a

memory cell block (i.e. set of columns), but cannot designate a particular column within a memory cell block (i.e. set of columns); and that the data programming means can only designate which column out of the memory cell block (i.e. set of columns) is to be programmed, but cannot designate a particular memory cell block (i.e. set of columns). Thus, the administrative law judge finds that the "column selection means" works in tandem with the "data programming means" to designate a column to be programmed, where the "column selection means" generates a signal (Y1, Y2 ... or Ym) that selectively activates the corresponding memory cell block (B1, B2 ... or Bm) and where the "data programming means" provides the data to be programmed to one of the columns within said memory cell block through the corresponding data input/output line (IO1, IO2 ... or IO8.) The administrative law judge further finds that the specification of the '969 patent does not support an interpretation of "column of memory cells" without a limitation of one column per data input-output line within a memory cell block because, as the intrinsic evidence shows, the column selection means cannot perform the function of selecting one of the columns; it can only select all of the columns within a memory cell block simultaneously. For the foregoing reasons, the administrative law judge finds that "column of the memory cells" should be interpreted to be "column of the memory cells for each input-output line."

The administrative law judge finds that the term "designating," read in the context of the claim language of claim 1 of the '969 patent and the specification of the '969 patent, is given its ordinary meaning and he interprets "designating" to mean "to indicate and set apart for a specific purpose." (Webster's Collegiate Dictionary, Tenth Edition.) The administrative law judge finds that the specification of the '969 patent supports this interpretation:

Column decoder 54 generates signals Y1 to Ym to selectively

> activate column selection MOSFETs Q1 to Qm so that data to be programmed can be supplied to one of memory cell blocks B1 to Bm through data input/output lines IO1 to IO8...

(JX-4 at 9:20-34 (emphasis added).) Here, the context of the passage is data programming the semiconductor memory device formed by arranging memory cells in a matrix form consisting of rows and columns. In this context, the column decoder generates and applies a signal that corresponds to one of the memory cells blocks B1 to Bm that is to be programmed:

> That is the data programming operation is effected with respect to the memory cells connected to data line X1 of memory cell block Bm. At the time of programing, signals X1, Ym, Z2 to Zm are set at a high level ... In this case, electrons are emitted only when the control gate voltage is at "0" level and programming data is supplied as a high voltage to the drain through any one of data input/output lines IO1 to IO8, column selection transistor Qm and selection transistor STm, and thus data can be programmed in the respective cell transistors.

(JX-4 at 20-34 (emphasis added).) The administrative law judge finds that this portion of the specification makes clear that by column decoder 54 applying a signal Ym to column selection transistor Qm, when programming data is supplied through one of the input/output lines IO1 to IO8, by the act of activating column selection transistor Qm, and thus activating selection transistor STm, column decoder 54 has designated memory cell block Bm as opposed to the other memory cell blocks, i.e. B1, B2, ... The administrative law judge finds that those portions of the specification do not limit the term "designating" to "generating and applying a signal" and thus the claim should not be limited to a preferred embodiment, especially in light of the claim language of claim 1 of the '969 patent that uses the term "designating" as opposed to "applying a signal."

The administrative law judge finds that the term "in response to a column selection

signal" of claim 1 of the '969 patent does not identify which signal is the column selection signal. The specification of the '969 patent however discloses that column decoder 54 "generates signals Y1 to Ym to selectively activate column selection MOSFETs Q1 to Qm." (JX-4 at 9:4-6.) The '969 patent specification also discloses column decoder 54 and signals Y1, Y2, ... Ym in Figure 10 of the '969 patent. (JX-4.) Complainant's expert Reed testified that one of ordinary skill in the art would have the sufficient knowledge of college decoders that a disclosure of the column selection signal or the circuitry necessary to interpret said signal would not be necessary:

> Q. Sir, isn't it a fact that there's nothing disclosed in this patent that corresponds to the column selection signal?
>
> A. I think we're getting into the level of ordinary skill issue here because the design of these decoders 54 and 53 was -- very little was disclosed about these things in the patent. Mr. Iwahashi, in '87, when disclosing this patent, had to be considering that anybody with enough experience to be reading his patent would know how to design a column decoder and would know how to design a row decoder. You're right, there are no explicit column selection signals decoded or presented, nor are all of the inputs to the row decoder disclosed.
>
> Q. So it's your opinion that someone of ordinary skill would be able to come up with whatever circuitry is necessary to finish out the function, correct?
>
> A. That's correct.

(Reed, Tr. at 1429:24-1425:19 (emphasis added).)

In view of Atmel and S3, supra, the administrative law judge finds that the disclosure of column decoder 54 in Figure 10 of the '969 patent, combined with the text of the specification and the expert testimony of Reed as to the knowledge of one of ordinary skill in the art, identifies

the "column selection signal" as a signal outside the "column selection signal" and discloses sufficient structure to respond to said signal. Hence, the administrative law judge interprets "in response to a column selection signal" as "responding to a signal outside of the column selection means."

For the foregoing reasons, the administrative law judge interprets the function of the "column selection means" to be "designating one of the columns of the memory cells in response to a column selection signal," with the administrative law judge interpreting "columns of the memory cells," "designating," and "in response to a column selection signal" as found supra.

Respondents argued that under controlling precedent, expert testimony cannot supply corresponding structure where there is none, citing Default Proof, 412 F.3d at 1302. However, in that case the Court held "the testimony of one of ordinary skill in the art cannot supplant the total absence of structure from the specification. " (Id.) (emphasis added).) The Court emphasized that it was the total absence of corresponding structure that it was focusing on when it distinguished S3, 259 F.3d at 1371 and Amtel, 259 F.3d at 1371:

> Because the specification of the '182 patent discloses no structure capable of dispensing cards and Gafford's conclusory testimony cannot compensate for such lack of disclosure, Default Proof's reliance on S3 and Amtel is unavailing. In both cases, the specifications of the patents at issue disclosed some corresponding structure.

(Default Proof, 412 F.3d at 1302.) Default Proof can additionally be distinguished because in Default Proof, the expert testified that the POS terminal disclosed in the specification included at least three alternative structures corresponding to the "means for dispensing" (the means-plus-function limitation for the claim-in-issue): (1) a "kiosk" associated with the POS terminal that

sold prepaid telephone cards; (2) the receipt printer peripheral portion of the POS terminal; or (3) the LCD or CRT display peripherals of the POS terminal operated by the "merchant." (Default Proof, 412 F.3d at 1301.) The Court found that none of those alternative structures formed part of the description of the POS terminal in the specification. Instead, the Court found that the specification described certain aspects of the POS terminal, but omitted any mention of the parts capable of dispensing debit cards. (Id.) However, in this investigation, complainant's expert Reed, did not testify that column decoder 54 includes alternative structures that correspond to the "column selection means" which can respond to outside selection signals. Rather, Reed testified that one skilled in the art knows sufficient knowledge with respect a decoder to design a decoder to respond to outside selection signals. Thus, the administrative law judge finds that complainant did not use its expert Reed's testimony to fill in structure that is totally absent from the '969 patent. Instead, the administrative law judge finds that complainant used its expert Reed's testimony to elaborate on the structure column decoder 54 disclosed in the '969 patent, and specifically to illustrate that a column decoder is a well known structure to one skilled in the art and one that is readily implemented from the description in the specification.

In addition, the administrative law judge finds that respondents did not raise an affirmative defense of invalidity of claim 1 of the '969 patent due to indefiniteness in their response. Additionally, the administrative law judge finds that respondents did not raise the issue of invalidity of claim 1 of the '969 patent due to indefiniteness in their pre-hearing statement or at the hearing. Furthermore, the administrative law judge finds that respondents failed to address the issue of the validity of claim 1 of the '969 patent due to indefiniteness in the validity sections of their post-hearing brief and reply brief. Thus, the administrative law judge

finds that respondents' raising of the specter of invalidity with respect to claim 1 of the '969 patent is untimely and unpersuasive.

Respondents also argued that "designating" should be interpreted to mean, inter alia, to place in an operable state. Respondents argued that the specification frames the act of selection or designation as part of a larger operation, which aims to place the selected memory cells and cell transistors in an operable state. (RBr at 50; RPFF 1338-1339.) However, the administrative law judge rejects this interpretation because the larger operation that respondents refer to is "data programming" which is performed by the "data programming means" not the "column selection means" as demonstrated by the specification:

> Column decoder 54 generates signals Y1 to Ym to selectively activate column selection MOSFETS Q1 to Qm so that data to be programmed can be supplied to one of memory cell blocks B1 to Bm through data input/output lines IO1 to IO8 or data can be read out from one of the memory cell blocks through the input/output lines.

(JX-4 at 9:4-8 (emphasis added).)

Respondents also argued that "one of the columns of memory cells" should be interpreted as "set of cell transistors string which are individually connected to the same column line." However, the administrative law judge finds his interpretation of "one of the columns of memory cells," is consistent with the "memory cell array" limitation's definition of "one of the columns of memory cells," i.e., "memory cell array comprising . . . first terminals of the memory cells in the same column being commonly connected to one of the column lines."

ii. structure

The parties agree that the corresponding structure of "column selection means" is column

decoder 54 of Fig. 10 of the '969 patent. (CBr at 50; TFF 451; RBr at 51; RPFF 1350; SBr at 31; SPFF 149.) However, the staff also argued that the claim element covered column decoder 54 and its "equivalents." Respondents argued that undisclosed equivalents are excluded from being corresponding structures because the specification does not clearly link just any general purpose decoder. Respondents also argued that the '969 patent expressly identifies column decoder 54 as the structure linked to performing the claimed function, and precedent limits corresponding structures to this specific decoder, citing WMS Gaming, Inc. v. Int'l Game Tech., 184 F.3d 1339, 1344 (Fed. Cir. 1999).

35 U.S.C. § 112, ¶ 6 states that means-plus-function claims are construed to cover corresponding structures disclosed in the specification and their equivalents:

> An element in a claim for a combination may be expressed as a means or step for performing a specified function without the recital of structure, material, or acts in support thereof, and such claim shall be construed to cover the corresponding structure, material, or acts described in the specification and equivalents thereof.

(emphasis added.) Hence, while a structure may not be deemed a corresponding structure, said structure may fall under the scope of a means-plus-function claim if it is determined to be equivalent to a corresponding structure. Thus, the administrative law judge finds that the corresponding structure for the "column selection means" is column decoder 54 of Fig. 10 of the '969 patent. Additionally, the administrative law judge finds that, under 35 U.S.C. § 112, ¶ 6, the scope of the "column selection means" limitation of claim 1 of the '969 patent encompasses its corresponding structure, viz. column decoder 54 of Fig. 10 of the '969 patent, and its equivalents.

Respondents argued that precedent limits corresponding structures to the structure that is linked to performing the claimed function, and cited WMS Gaming., 184 F.3d at 1344. WMS Gaming is a special situation in which a structure corresponding to the means element is an algorithm executed by a computer. In WMS Gaming, the Court stated that where a patent discloses a general purpose computer or microprocessor as the structure, "[t]he instructions of the software program that carry out the algorithm electrically change the general purpose computer by creating electrical paths within the device [that] create a special purpose machine for carrying out the particular algorithm." 184 F. 3d at 1348. Thus, computers, which can be programmed to carry out a myriad of functions, whereby the program itself changes the structure of the computer by affecting its electrical paths, create a special problem in means-plus-function claim construction. Since the disclosed structure cannot in those circumstances be identified as the general purpose computer, whose structure changes according to its programmed functions, the special purpose computer programmed to perform the disclosed algorithm however must be identified. See WMS Gaming, 184 F.3d at 1348-49. Even in this special case where the structure is altered by virtue of its programmable nature, the structural element is construed to include only the structure programmed to perform the particular disclosed function. Hence, in this special case, where the corresponding structure is a general programmable device such as a computer or microprocessor which requires an algorithm to differentiate the claimed structure from a general programmable device, the algorithm does describe a corresponding structure. The administrative law judge finds that the column decoder 54 of Figure 10 of the '969 patent, however, does not fit into the special case exception and thus the equivalent structures are not limited to the structures disclosed in the '969 patent. However, he finds that under 35 U.S.C. § 112, all equivalent

structures must perform the recited function.

B. Asserted Claims Of The '449 Patent

1. A nonvolatile semiconductor memory device comprising:

a memory cell array comprising memory cells arranged in matrix form having first row lines, second row lines, and column lines, each memory cell including cell transistors and a selection transistor for selecting the memory cell, and each of the cell transistors having a control gate, a floating gate, a channel region, and an insulation film formed between the floating gate and the channel region for electrically storing data by using charges stored in the floating gate, each memory cell having a first terminal and a second terminal, the first terminals of the memory cells in the same column being commonly connected to one of the column lines, the second terminals of the memory cells being connected to a reference potential, the control gates of the cell transistors in the same row being commonly connected to one of the first row lines, and the gate of the selection transistor being connected to one of the second row lines;

data programming means for selectively storing data into the cell transistors by one of injecting electrons through the insulation film into the floating gate by utilizing a tunnel effect, and emitting electrons through the insulation film from the floating gate by utilizing a tunnel effect;

row selection means for applying a signal to one of the first row lines and applying a signal to one of the second row lines in response to a row selection signal, thereby selecting a cell transistor connected to the first row line and a selection transistor connected to one of the second row lines;

first switching means connected between each of the second terminals of the memory cells and the reference potential, for disconnecting the memory cell from the reference potential when the data programming means stores data; and

second switching means for controlling whether or not the signal from the row selection means should be applied to the cell transistor in the memory cell, the second switching means being connected between the row selection means and the memory cell, wherein the second switching means is turned on when the memory cell which is connected to the second switching means is selected, and the second switching means is turned off when the memory cell which is connected to the second switching means is not selected.

4. A nonvolatile semiconductor memory device comprising:

a memory cell array comprising memory cells arranged in matrix form having first row lines, second row lines and column lines, each memory cell including cell transistors and a selection transistor for selecting the memory cell, and each of the cell transistors having a control gate, a floating gate, a channel region and a tunnel insulation film including a portion having a thickness

sufficient to cause a tunnel effect between the channel region and the floating gate, for electrically storing data by using charges stored in the floating gate, each memory cell having a first terminal and a second terminal, the first terminals of the memory cells in the same column being commonly connected to one of the column lines, the second terminals of the memory cells being connected to a reference potential, the control gates of the cell transistors in the same row being commonly connected to one of the first row lines, and the gate of the selection transistor being connected to one of the second row lines;

data programming means for selectively storing data into the cell transistors by one of injecting electrons through the tunnel insulation film into the floating gate, and emitting electrons through the tunnel insulation film from the floating gate;

row selection means for applying a signal to one of the first row lines and applying a signal to one of the second row lines in response to a row selection signal, thereby selecting a cell transistor connected to the first row line and a selection transistor connected to one of the second row lines;

first switching means connected between each of the second terminals of the memory cells and the reference potential, for disconnecting the memory cell from the reference potential when the data programming means stores data; and

second switching means for controlling whether or not the signal from the row selection means should be applied to the cell transistor in the memory cell, the second switching means being connected between the row selection means and the memory cell, wherein the second switching means is turned off when the memory cell which is connected to the second switching means is not selected.

1. Claims 1 And 4

a. "data"

In issue is the claimed phrase "data" found in the phrases "data programming means" and "data latching means" of independent claims 1 and 4 of the '449 patent, the only asserted independent claims of the '449 patent. (JX-7 at 22:5, 24:14.)

The parties' arguments with respect to the term "data," as used in the phrase "data programming means" of the '449 patent, is identical in all material aspects to their arguments with respect to the term "data" as used in the phrase "data programming means" of the '969

patent. As found supra, the administrative law judge interprets the term "data" as the "information that comes into memory, passes through the latch or other circuitry of the memory device, and ultimately is programmed into the memory cells." (See Section VII.A.1.a, supra.)

b. "data programming means"

In issue is the claimed phrase "data programming means" which is found in the following clause of independent claim 1 of the '449 patent:

> data programming means for selectively storing data into the cell transistors by one of injecting electrons through the insulation film into the floating gate by utilizing a tunnel effect, and emitting electrons through the insulation film from the floating gate by utilizing a tunnel effect

(JX-7 at 22:6-11 (emphasis added).)

The claimed phrase "data programming means" is also found in the following clause of independent claim 4 of the '449 patent:

> data programming means for selectively storing data into the cell transistors by one of injecting electrons through the tunnel insulation film into the floating gate, and emitting electrons through the tunnel insulation film from the floating gate

(JX-7 at 24:14-18 (emphasis added).) Claims 1 and 4 of the '449 patent are the only asserted independent claims of the '449 patent.

i. function

In addition to complainant's arguments with respect to the '969 patent, complainant argued that "selectively storing data into the cell transistors," found in both claim 1 and claim 4 of the '449 patent refer to injection and emission as alternative means of carrying out the function of said claims. (CBr at 36; CRBr at 23.) Complainant further argued that said claims use a

"Markush style" of claiming ("selected from the group consisting of A, B, and C") that allows for selection of any one or more of the listed group, but avoids the use of "or," a word that can prompt claim objection or rejection based on indefiniteness. (CBr at 36.) Complainant also argued that regardless of whether said the drafting of said claims is referred to as "Markuish-style" drafting or not, the plain and ordinary meaning of the relevant claim language "by one of injecting electrons ... and emitting electrons..." is properly read in the disjunctive to allow for "selective storing data into the cell transistors" either by injection or emission. (CRBr at 27.)

With respect to the recited function for the "data programming means," complainant argued that, based on Reed's expert testimony, the function for the "data programming means" in claim 1 of the '449 patent is "for selectively storing data into the cell transistors by one of injecting electrons through the insulation film into the floating gate by utilizing a tunnel effect, and emitting electrons through the insulation film from the floating gate by utilizing a tunnel effect" and the function for claim 4 of the '449 patent is "for selectively storing data into the cell transistors by one of injecting electrons through the tunnel insulation film into the floating gate, and emitting electrons through the tunnel insulation film from the floating gate." (CBr at 35, 40; TFF 398-400.)

In addition to respondents' arguments with respect to the '969 patent, respondents also argued that the language in the "data programming means"does not involve a Markush claim because the Patent Office insists on the transition phrase "group consisting of" to "close" a Markush group, citing Gillette Co. v. Energizer Holdings, Inc., 404 F.3d 1367, 1372 (Fed. Cir. 2005), and the terms "consisting of" or "group consisting of" are nowhere to be found in the asserted claims. (RBr at 57; RRBr at 23-24; RPFF 1393.) Respondents also pointed to the claim

language of the "data programming means" in claims 1 and 4 of the '449 patent to support their argument that "programming" requires both injection and emission. (RBr at 20-21, 56; JX-7 at 22:6-11; RPFF 1386-1388.)

Referring to complainant's argument that claims 1 and 4 of the '449 patent uses a "Markush style" of claiming, a Markush-type claim recites alternatives in a format such as "selected from the group consisting of A, B and C." (Manual of Patent Examining Procedure, § 2173.05(h) (8th ed, Rev. 3 Aug. 2005.)) The language in claims 1 and 4 of the '449 patent does not use the phrase "group consisting of," but merely uses the phrase "one of." (JX-7 at 22:7, 24:15.) Thus, the administrative law judge finds that the language "selectively storing data ... by one of injecting electrons... and emitting electrons..." is not Markush-style and that said claims are not Markush-type claims. However, the administrative law judge finds that the plain and ordinary meaning of the language "by one of injecting electrons...and emitting electrons" means that selectively storing data may be accomplished by either injecting electrons into the floating gate or emitting electrons from the floating gate. (JX-7 at 22:7-11, 24:15-18.) The administrative law judge further finds that the use of "one of" qualifies the phrase "injecting electrons ... and emitting electrons" to merely require that one or the other is an acceptable means of selectively storing data. (JX-7 at 22:7-11, 24:15-18.) As found supra, the specification of the '449 patent[15] supports the interpretation that selectively storing data may be accomplished by either injecting electrons into the floating gate or emitting electrons from the floating gate.[16] (See Section

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[15] The specification of the '969 patent is identical to the specification of the '449 patent.

[16] No party has argued that the term "selectively storing data into the cell transistors" should be interpreted differently from "selectively programming the cell transistors." Thus, except for how the remaining language of claim 1 of the '969 patent qualifies the meaning of said

VII.A.1.b.i, supra.)

With respect to the claim language of claims 1 and 4 of the '449 patent, said language does not reference "blanket injection" and does not define selectively storing data as requiring blanket injection as a precondition to selective emission. (JX-7 at 22:6-11, 24:14-18.) Additionally, the language of said claims only states that it requires injection or emission; it does not state whether in "selectively storing data into the cell transistors," the injection is selective, the emission is selective, or both injection and emission are selective. (JX-7 at 22:6-11, 24:14-18.) Unlike claim 1 of the '969 patent, because there is no language within claims 1 and 4 of the '449 patent linking the cell transistor with the stored data of the data latching means, the administrative law judge finds no additional limitation with respect to the relationship between the data selectively stored in the transistors and the stored data in the data latching means.

Referring to the specification of the '449 patent, because it is the same as the '969 patent, the administrative law judge's findings related to the specification and with respect to the '969 patent as to whether programming is a one-step or two-step process and whether programming is limited to selective emission, apply to the '449 patent. As found, supra, with respect to "selectively programming the cell transistors," the administrative law judge finds that "selectively storing data into the cell transistors" is not a two-step process that requires blanket injection before selective emission, and said claim term is not limited to selective emission. (See Section VII.A.1.b.i, supra.)

With respect to the prosecution history, as found supra, the applicant did not disclaim

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term versus how the remaining language of claims 1 and 4 of the '449 patent qualify the meaning of said term, the administrative law judge interprets said terms consistently.

selective injection in light of a prior art reference that disclosed selective injection, but instead disclaimed emitting (releasing) electrons from the floating gate to the control gate in light of the prior art reference. Hence, the administrative law judge finds that the prosecution history does not limit the scope of "data programming means" to merely selective emission.

Based on the foregoing, the administrative law judge interprets the function for the "data programming means" of claim 1 of the '449 patent as

> selectively storing data into the cell transistors by one of injecting electrons through the insulation film into the floating gate by utilizing a tunnel effect, and emitting electrons through the insulation film from the floating gate by utilizing a tunnel effect

and he interprets the function for the "data programming means" of claim 4 of the '449 patent as

> selectively storing data into the cell transistors by one of injecting electrons through the tunnel insulation film into the floating gate, and emitting electrons through the tunnel insulation film from the floating gate.

Additionally, the administrative law judge interprets the language "selectively storing data into the cell transistors [etc.]" of claim 1 of the '449 patent as

> changing the charge state of the cell transistors either by: injecting electrons through the insulation film into the floating gate by utilizing a tunnel effect; or emitting electrons through the insulation film from the floating gate by utilizing a tunnel effect

(emphasis added) and he interprets the language "selectively storing data into the cell transistors [etc.]" of claim 4 of the '449 patent as

> changing the charge state of the cell transistors either by: injecting electrons through the tunnel insulation film into the floating gate; or emitting electrons through the tunnel insulation film from the floating gate.

(emphasis added.)

Respondents, citing Superguide, 358 F.3d at 886, and IPXL Holdings, L.L.C. v. Amazon.com, Inc., 333 F.Supp. 2d 513, 525-26 (E.D. Va. 2004), argued that the use of the phrase "one of" combined with the use of the conjunctive term "and" in claims 1 and 4 of the '449 patent connotes a conjunctive list and thus requires both injection and emission of electrons in order to selectively store data into the cell transistor. (RBr at 56; RPFF 1388.) However, in Superguide and IPXL Holdings, the claims being construed consisted of the term "at least one of" instead of "one of" and the conjunctive list was a list of categories, not a list of processes. Specifically, in Superguide, 358 F.3d at 886, the claimed phrase-at-issue was "at least one of a desired program start time, a desired program end time, a desired program service, and a desired program type." The Court held that the phrase "at least one of" preceded a series of categories of criteria and the patentee used the term "and to separate the categories of criteria, which connoted a conjunctive list. Id. Applying the grammatical principle that an article of a preposition applying to all the members of the series must either be used only before the first term or else be repeated before each term, the Court held that the phrase required at least one desired program start time, at least one desired program end time, at least one a desired program service, and at least one desired program type. Id. The district court used the same principle in IPXL Holdings, 333 F. Supp. 2d at 525-26, to interpret "at least one of user defined transactions and user defined parameters" to mean at least one user defined transaction and one user defined parameter.

In contrast to Superguide, the administrative law judge finds that the phrases "injecting electrons..." and "emitting electrons..." are not "categories", as that term is used in Superguide, but specific processes. There are no subcategories within injection of electrons or emission of electrons. Thus, respondents' interpretation makes the use of "one of" superfluous. For the

foregoing reasons, the administrative law judge interprets "selectively storing data into the cell transistors" as requiring either injecting electrons to the floating gate or emitting electrons from the floating gate.

ii. structure

With respect to corresponding structure for the "data programming means" of the '449 patent, the parties made arguments identical to the parties' arguments with respect to corresponding structure for the "data programming means" of the '969 patent.

In addition, complainant argued that both Reed and Subramanian agreed that the following may comprise corresponding structure for certain embodiments: "programming circuit" 10 of Fig. 1 of the '449 patent, the circuit shown in Fig. 7 of the '449 patent, the circuit shown in Fig. 8 of the '449 patent, and the circuit shown in Fig. 9 of the '449 patent. (CBr at 42.) Thus, unlike the '969 patent, complainant did not oppose respondents' assertion that said structures were appropriate corresponding structures for the "data programming means" function for the '449 patent because the use of the "data latching means" was not required. (CBr at 42.) However, in connection with an embodiment that makes use of the latch of Fig. 18 of the '449 patent, which is an optional improvement for said embodiment, complainant also argued that said structures are not appropriate corresponding structures for the "data programming means" limitation. (CBr at 42; CRBr at 28; TFF 413-415; CRRFF 1107A-I, 1108A-K.) Complainant further argued that the existence of other corresponding structures besides transistor 81 should not count against the identification of transistor 81 as a corresponding structure because a court must consider all of the "alternative embodiments of the invention" in identifying structure that may serve as the "means for" the recited function of a means-plus-function limitation and

because none of the said structures can be used in connection with programming from a latch. (CRBr at 28.)

The parties do not dispute that the programming circuit 10 of Fig. 1, the circuit shown in Fig. 7, the circuit shown in Fig. 8, and the circuit shown in Fig. 9 are appropriate corresponding structures for claims 1 and 4 of the '449 patent because said claims do not require that the "data programming means" use the "data latching means." However, as with the '969 patent, the administrative law judge finds that transistor 81 of Figure 18A of the '449 patent is not an appropriate corresponding structure for the "data programming means." (See Section VII.B.1.b.ii, supra.) Instead, as found supra, the administrative law judges finds that the entire circuit of Figure 18A is a corresponding structure for the "data programming means." (See Section VII.B.1.b.ii, supra.)

For the foregoing reasons, the administrative law judge interprets the corresponding structures for the "data programming means," with respect to claims 1 and 4 of the '449 patent, to be the data programming circuit 10 shown in Figure 1 of the '449 patent, the entire structure shown in Figure 7 of the '449 patent, the entire structure shown in Figure 8 of the '449 patent, the entire structure shown in Figure 9 of the '969 patent, and the entire structure shown in Figure 18A of the '449 patent, with respect to claims 1 and 4 of the '449 patent.

c. "row selection means"

In issue is the claimed phrase "row selection means" which is found in independent claims 1 and 4 of the '449 patent, the only asserted independent claims of the '449 patent. (JX-7 at 22:12, 24:19.)

i. function

Complainant argued that the recited functions for the "row selection means" limitation of claims 1 and 4 of the '449 patent are "applying a signal to one of the first row lines and applying a signal to one of the second row lines in response to a row selection signal, thereby selecting a cell transistor connected to the first row lines and a selection transistor connected to one of the second row lines." (CBr at 46.) It is argued that the method of identifying the function for a means-plus-function element by identifying the appropriate language actually recited in the claim is completely consistent with Federal Circuit precedent. (CBr at 46-47.)

Respondents argued that the functions for the "row selection means" limitation of claims 1 and 4 of the '449 patent are "to place a cell transistor in an operable state by applying a row selection signal to a single first row line, and to place a selection transistor in an operable state by applying a row selection signal to a single second row line." (RBr at 58; RPFF 1403.)

The staff argued that the "row selection means" limitation of claims 1 and 4 of the '449 patent should be interpreted consistently with complainant's proposed construction, viz. "applying a signal to one of the first row lines and applying a signal to one of the second row lines in response to a row selection signal, thereby selecting a cell transistor connected to the first row lines and a selection transistor connected to one of the second row lines." (SBr at 31-32; SPFF 150, 152.)

The administrative law judge finds that the plain language of the "row selection means" limitation of claims 1 and 4 of the '449 patent makes clear that the function of the "row selection means" for both claims 1 and 4 of the '449 patent is to "[apply] a signal to one of the first row lines and [apply] a signal to one of the second row lines in response to a row selection signal, thereby selecting a cell transistor connected to the first row lines and a selection transistor

connected to one of the second row lines." (JX-7 at 22:12-17, 24:19-24.) Thus, the "row selection means" for claims 1 and 4 of the '449 patent must respond to a "row selection signal" by "applying a signal" to both one of the "first row lines" and one of the "second row lines."

Respondents argued that the function of "row selection means" for claims 1 and 4 of the '449 patent should be interpreted to mean, inter alia, to place a cell transistor in an operable state. Respondents also argued that the specification frames the act of applying a signal as part of a larger operation, which aims to place the selected cell transistors in an operable state. Said arguments are rejected because the larger operation that respondents refer to is "data programming," which is performed by the "data programming means" not the "row selection means" as demonstrated by the specification:

> Row decoder 53 generates signals X1, X2, ..., signals W11, W12, ... W1n, and signals W21, W22, ... W2n to select a row line or lines in the memory cell array. Column decoder 54 generates signals Y1 to Ym to selectively activate column selection MOSFETS Q1 to Qm so that data to be programmed can be supplied to one of memory cell blocks B1 to Bm through data input/output lines IO1 to IO8 or data can be read out from one of the memory cell blocks through the input/output lines.

(JX-7 at 10:49-58 (emphasis added).)

Referring to what the administrative law judge has found as the function of the "row selection means," in issue are the phrases "one of the first row lines," "one of the second row lines," and "in response to a row selection signal."[17]

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[17] The parties do not dispute the meaning of the term "applying a signal," "first row line," and "second row line." However, respondents also argued that they incorporated by reference "the relevant discussion and cited intrinsic evidence it presented for its construction of 'one of' and 'in response to' from its analysis with regards to the '969 patent's 'row selection means.'" (RBr at 58-59.) Thus, respondents dispute, inter alia, the meaning of "one of." Because the interpretation of "one of" must be in the context of "first row lines" and "second row lines," the

Complainant argued that the terms "first row lines" and "second row lines" have clear antecedents in the "memory cell array" limitation, and that their meaning is clear. (CRBr at 37.)

Respondents, in addition to their arguments with respect to their interpretation of "one of" and "in response to" for the '969 patent's "row selection means," argued that the '449 patent's "row selection means" use two new terms "first row lines" and "second row lines," whose meaning is not in dispute, and that the "first row line" is the row line connecting the control gates of cell transistors in the same row, while the "second row line" corresponds to the row line connecting the gate of the selection transistors in the same row. (RBr at 59; RPFF 1405-1406.) Respondents also argued that the '449 patent's "row selection means" requires applying a signal to a single first row line. (RBr at 59.) Respondents further argued that complainant's Reed testified at trial that the "row selection means" does not actually select any row line. (RRBr at 38; RRTFF 444C.) Respondents also argued that Reed testified that the function of the row selection means no longer involves "applying a signal" as the claims require but merely involve making the signal "available" would suffice. (RRBr at 38; RRTFF 444D-E.)

The staff, while agreeing with complainant that the "row selection means" limitation should be interpreted consistently with complainant's proposed construction, viz. "applying a signal to one of the first row lines and applying a signal to one of the second row lines in response to a row selection signal, thereby selecting a cell transistor connected to the first row lines and a selection transistor connected to one of the second row lines," which is the function recited in the claim, agreed with respondents that only one of the rows of the memory cells must

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administrative law judge interprets the entire phrases "one of the first row lines" and "one of the second row lines," despite the fact that the parties do not dispute the terms "first row line" and "second row line."

be selected. (SBr at 31-32; SPFF 150, 152.)

The administrative law judge finds that the "memory cell array" limitation of claims 1 and 4 of the '449 patent defines a "first row line" and a "second row line" by the following language of the memory cell array limitation of claims 1 and 4 of the '449 patent:

> a memory cell array comprising memory cells arranged in matrix form having first row lines, second row lines ... the control gates of the cell transistors in the same row being commonly connected to one of the first row lines, and the gate of the selection transistor being connected to one of the second row lines.

(JX-7 at 21:55-56, 22:1-5, 23:62-63, 24:9-13 (emphasis added).) Additionally, in the context of the entire "row selection means" limitation, the administrative law judge finds that "one of the first row lines" and "one of the second row lines" must each be a singular entity that the "row selection means" is capable of applying a signal to, because the function of the "row selection means" is, inter alia, to apply a signal to "one of the first row lines" and "one of the second row lines." (JX-7 at 22:12-14, 24:19-21.) He further finds that the specification of the '449 patent makes clear that a first row line and a second row line, as defined by the memory cell array limitation of claims 1 and 4 of the '449 patent, is capable of being designated:

> Row decoder 53 generates signals X1, X2, ... signals W11, W12, ... W1n and signals W21, W22, ... W2n to select a row line or lines in the memory cell array.

(JX-7 at 8:49-52 (emphasis added).) From this text, combined with Figure 10, the administrative law judge finds that the specification of the '449 patent makes clear that the row decoder is applying a signal to one of the first row lines and one of the second row lines.

For the foregoing reasons, the administrative law judge interprets "one of the first row lines" for claims 1 and 4 of the '449 patent to mean "a line commonly connecting the control

gates of the cell transistors in the same row" and "one of the second row lines" to mean "a line connecting the gates of the selection transistors in the same row."

Based on the same findings made with respect to the function of "row selection means" of claim 1 of the '969 patent, the administrative law judge interprets "in response to a row selection signal" for claims 1 and 4 of the '449 patent as "responding to a signal outside of the row selection means." (See Section VII.A.1.d.i, supra.)

ii. structure

Complainant argued that row decoder 53 of Figure 10 combined with the circuitry of Figure 17, as illustrated in CDX-139-2, comprises sufficient corresponding structure to perform the recited function of the "row selection means" of claims 1 and 4 of the '449 patent. (CBr at 47-48; TFF 429-431, 439.) Complainant also argued that the circuitry of Figure 17 could be combined with the matrix structure and associated circuitry of Figure 10, including row decoder 53, and that said combination was disclosed in the specification. (CBr at 48; TFF 339, 439; JX-7 at 11:58-12:8.) Complainant further argued that, in an embodiment that combined Figures 10, 17 and 18A, as illustrated in CDX-139-4, row decoder 53 of Figure 10 combined with the circuit of Figure 17 would still comprise sufficient corresponding structure to perform the recited functions of "row selection means" elements of claims 1 and 4 of the '449 patent. (CBr at 49; TFF 346-351, 440-443.) Complainant, in addition, argued that the corresponding structure does not require both row decoder 53 and column decoder 55 for the "row selection means" of claims 1 and 4 of the '449 patent. (CRBr at 38.)

Respondents argued that two specific circuits are necessary to carry out the full function of the '449 patent's "row selection means:" the row decoder 53 and column decoder 55. (RBr at

62; RPFF 1419.) Respondents also argued that both circuits are required because to identify the corresponding structure for the "row selection means," an additional claimed element of the '449 patent should be considered, viz. the second switching means.

It is further argued by respondents that the corresponding structure of this "second switching means" is the MOSEFT transistor QT as shown in Figure 17; that the asserted claims of the '449 patent must include and practice the embodiment shown in Figure 17 because the figure and its corresponding text are the only locations where the "second switching means" appear; and that thus, in this context, to apply a signal on any first row line, the '449 patent requires a logical combination of row decoder 53's double-indexed W11-W1n signals and column decoder 55's Z signals to generate the triple-indexed W111-W1n1 signals of Figure 17. (RBr at 60-62; RPFF 1411-1418.)

The staff argued that the structure corresponding to the "row selection means" in the '449 patent includes row decoder 53 of Figure 10. (SBr at 33.) The staff also argued that this is different from the '969 patent because in the '449 patent some of the "row selection" function is performed by the "second switching means." (SBr at 33; SPFF 160.)

The administrative law judge finds that claims 1 and 4 of the '449 patent differ from claim 1 of the '969 patent in that claims 1 and 4 consist of a "second switching means" limitation (and thus require the corresponding structure of the "second switching means," the QT transistors) whereas claim 1 of the '969 patent has no such requirement. (JX-4 at 22:53-23:26; JX-7 at 22:23-23, 24:30-37.) The administrative law judge further finds that the specification of the '449 patent states that row decoder 53 (as well as the other structures of Figure 10 that are connected to the memory cells blocks, including data programming circuit 200, and column

decoders 53 and 55) can be combined with the circuitry of Figure 17, where the Figure 17 circuit replaces the circuit that comprises each of the memory cell blocks in Figure 10:

> FIG. 17 is a circuit diagram showing a modified construction of a peripheral portion of the memory cell section in the circuit of FIG. 10;
>
> * * *
>
> FIG. 17 shows a circuit which can be used to form the FIG. 1 circuit in a matrix form. The circuit of FIG. 17 corresponds to one of memory cells blocks B1 to Bm [previously identified in the specification in FIG. 10], and includes MOSFETs, QT1, QT2 ...

(JX-7 at 3:19-21, 11:27-30 (emphasis added).) The administrative law judge also finds that the specification of the '449 also states that the combined structure of Figure 10 and Figure 17 can be further combined with the latch structure in Figure 18A.

> FIG. 18A is a circuit diagram for illustration of another construction of the circuit of FIG. 10;
>
> * * *
>
> Further it is possible to connect a latch circuit shown in FIG.18 to each column line...

(JX-7 at 3:23-24; 11:45-46.)[18]

However, the administrative law judge finds that the fact that the '449 patent discloses that the structure in Figure 10 can be combined with either the circuit of Figure 17, the circuit of

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[18] There is no issue as to the function of "second switching means." Thus, the parties agree that the function of "second switching means" is "controlling whether or not the signal from the row selection means should be applied to the cell transistor in the memory cell." (CRBr at 43; RRBr at 41; SBr at 33; JX-7.) There is also no issue as to the corresponding structure of "second switching means." Thus, the parties agree that the corresponding structures for the term "second switching means" are the MOSFET QT transistors shown in Figure 17 of the '449 patent. (CRBr at 43; RRBr at 41; SBr at 33; JX-7.)

Figures 18A or both of said circuits does not mean, as complainant argued, that within an embodiment of the '449 patent (JX-7 at 11:27-44) that combines the structure in Figure 10 and the circuit in Figure 17, or within an embodiment of the '449 patent (JX-7 at 11:45 - 65) that combines the structure in Figure 10, the circuit in Figure 17, and the data latch circuit in Figure 18A, the entire structure consisting of row decoder 53 combined with the entire circuit of Figure 17 is the corresponding structure for the "row selection means." He rejects this argument by complainant because the entire circuit of Figure 17 does not perform the recited function of the "row selection means." Thus, the issue is which structures within said embodiments of the '449 patent perform the recited function, and hence are the corresponding structures of the "row selection means" of claims 1 and 4 of the '449 patent

As to said issue, the administrative law judge finds that the specification of the '449 patent states that in an embodiment of the invention that uses the "second switching means," row decoder 53 of Figure 10, column decoder 55 of Figure 17, and the QT transistors of Figure 17 work together to select a particular cell transistor to be programmed:

> FIG. 10 shows a nonvolatile semiconductor memory device formed by arranging memory cells with the above construction in a matrix form. ... Row decoder 53 generates signals X1, X2, ..., signals W11, W12, ..., W1n and signals W2, W22, ..., W2n ... Further, column decoder 55 generates signals Z2 to Zm ...
>
> * * *
>
> FIG. 17 shows a circuit which can be used to form the FIG. 1 circuit in a matrix form. The circuit of FIG. 17 corresponds to one of memory cell blocks B1 to Bm, and includes MOSFETs QT1, QT2, ... which are connected to the control gates of the cell transistors and whose conduction states are controlled by signals, X1, X2, ... Since signals are input through MOSFETs QT1, QT2, ... a desired one of the memory cell blocks can be programmed by

> selectively satisfying a logical condition determined by a combination of signals W11, W12, ... and signals Z2 to Zm supplied to corresponding memory cell blocks to selectively set signals W1n1, ... W121, W111 to a high voltage level.

(JX-7 at 8:43-59, 11:27-38 (emphasis added).)

From said portions of the specification of the '449 patent, the administrative law judge finds that the signals X1, X2, ... are the signals that the row selection means applies to one of the second row lines, and that signals W111, W121, ... W1n1 are the signals that the row selection means applies to one of the first row lines. The administrative law judge further finds that the signals X1, X2, ..., W11, W12, ... W1n, and Z2 to Zm identified in the portion of the specificaion that describes Figure 17 are identical to the signals X1, X2, ...,W11, W12, ... W1n, and Z2 to Zm identified in the portion of the specification that describes Figure 10. The administrative law judge also finds that said signals are identical because the patentee used identical identifiers for both sets of signals, and if the patentee wanted to indicate that the signals in the specification's description of Figure 17 were different from the signals in the specification's description of Figure 10, the patentee would have used a different identifier in identifying the signals in the specification's description of Figure 17. Furthermore, the administrative law judge finds that the text of the specification and Figure 10 make clear that row decoder 53 generates the signals X1, X2, ... and W11, W12, ... W1n and that column decoder 55 generates the signals Z2 through Zm. Thus, the administrative law judge finds that the signals X1, X2, ... that are present in Figure 17 are generated by row decoder 53, and the signals W111, W121, ... W1n1 are generated by row decoder 53 and column decoder 55, through the combinations of signals W11, W12, ... W1n and signals Z2 to Zm as described in the specification of the '449 patent. Hence, the administrative

law judge finds that both row decoder 53 and column decoder 55 are required to apply a signal to one of the first and second row lines in response to a row selection signal in an embodiment that uses a combination of row decoder 53 of Figure 10 and the circuit of Figure 17 of the '449 patent.

The administrative law judge further finds that the fact that both row decoder 53 and column decoder 55 are required to apply a signal to one of the first and second row lines in response to a row selection signal does not change in an embodiment of the '449 patent (JX-7 at 11:45-65) that uses a combination of row decoder 53 of Figure 10, the circuit of Figure 17, and the data latch circuit of Figure 18A of the '449 patent. With respect to said embodiment, the specification of the '449 patent states:

> Further, it is possible to connect a latch circuit shown in FIG. 18 to each column line (the drain of the selection transistor ST). ... Data to be programmed can be latched in latch circuit 89, and the column lines can be selectively set at high voltage or 0 V according to the latched data for one row of memory cells so that the all memory cells [sic] connected to one line of row lines can be programmed. Therefore, MOSFETs QD2 to QDm for array division shown in FIG. 10 can be omitted.

(JX-7 at 11:45-65.) The administrative law judge finds that the specification states, that because it is possible to connect one or more latch circuits to one or more column lines (so that a latch circuit is connected to each column line), it is possible to eliminate MOSFETs QD2 to QDm. The administrative law judge further finds that even if he accepts complainant's argument that the reason MOSFETs QD2 to QDM can be eliminated is because column decorder 55 is no longer needed to select a particular memory cell block due to the presence of one or more data latches, he does not accept complainant's argument that additional structure can be eliminated

because the specification does not state that any additional structure of Figures 10 or 17 can be eliminated (such as column decoder 55, signals W1n1 ..., W121, W111, or QT transistors QT1, QT2, ...). Further, the administrative law judge finds that the specification of the '449 patent is silent as to how MOSFETs QT1, QT2... interpret signals in an embodiment that uses the data latch of Figure 18A. He also finds that there is nothing in the '449 specification that negates or modifies the requirement of an embodiment (JX-7 at 11:45-65) that uses the circuit of Figure 17 to have a combination of signals W11, W12, ... W1n generated by row decoder 53 and signals Z2 to Zm generated by column decoder 55 to satisfy a logical condition and allow the combined signal W1n1, ... W121, W111 to be input through MOSFETs QT1, QT2, ... Thus, the administrative law judge finds that both row decoder 53 and column decoder 55 are required to apply a signal to one of the first and second row lines in response to a row selection signal in an embodiment of the '449 patent (JX-7 at 11:45-65) that uses a combination of row decoder 53 of Figure 10, the circuit of Figure 17, and the data latch circuit of Figure 18A.

With respect to the QT transistors of Figure 17, the parties agree that the QT transistors of Figure 17 are corresponding structure for the "second switching means" of claims 1 and 4 of the '449 patent, as found supra. Additionally, the administrative law judge finds that the purpose of the QT transistors is to facilitate the programming of a connected cell transistor within a selected row by either allowing or not allowing a row selection signal (e.g. W111) to pass through to the control gate of said connected cell transistor, depending on whether a row selection signal (e.g. X1) has turned the corresponding QT transistor state on by changing its conductive state. Because this purpose depends on the row decoder 53 and column decoder 55 having already applied a signal to one of the first row lines and one of the second row lines, the administrative

law judge finds that the QT transistors do not perform the recited function of applying a signal to one of the first row lines and one of the second row lines. Thus, in an embodiment of the '449 patent (JX-7 at 11:27-44) that combines row decoder 53 of Figure 10 with the circuit of Figure 17, the administrative law judge finds that row decoder 53 combined with column decoder 55 of Figure 10 is the corresponding structure of the "row selection means," and that the QT transistors of Figure 17 are not part of the corresponding structure of the "row selection means."[19]

For the foregoing reasons, the administrative law judge finds that the combination of row decoder 53 and column decoder 55 are the corresponding structures for the "row selection means" of claims 1 and 4 of the '449 patent.

Complainant argued that interpreting the corresponding structure to require both row decoder 53 and column decoder 55 for the "row selection means" limitation fails to take account of the fact that the '449 patent requires an embodiment that combines the basic features illustrated in Figure 10 with the circuitry of Figure 17. Complainant further argued that once the circuitry of Figure 10 and Figure 17 are combined, the recited function of the "row selection means" limitations can be performed by row decoder 53. (CRBr at 38; TFF 429-439.) However, complainant failed to show how this conclusory statement shows that column decoder 55 is not part of the corresponding structure for the "row selection means" as column decoder 55 is also a basic feature of Figure 10. In addition, the administrative law judge finds that the specification of the '969 patent is clear that when Figure 10 is combined with Figure 17, the "row selection means" no longer generates signals W11, W12, ... W1n to the row lines but now generates

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[19] The administrative law judge finds that this finding does not change in embodiments that use the data latch circuit of Figure 18A.

W111, W121, ... W1n1 to the row lines, and is equally clear that this signal is a combination of signals W11, W12, ... W1n, and signals Z2 to Zm. (JX-7 at 11:33-38.)

Complainant also argued that one or ordinary skill in the art in 1987 would be able to design a row decoder to include the logical conditions attributed to column decoder 55. (CBr at 48; TFF 336.) It was further argued that by 1987 persons skilled in the art had significant experience with row decoder devices and could design circuitry needed for such devices. (CBr at 48; TFF 436.) It was also argued that the claims and specification of the '449 patent do not limit the structure or functionality of row decoder 53 in any way that would preclude such a structure from performing the recited function of the "row selection means." (CBr at 48; TFF 336.) It was in addition argued that, by its very name, row decoder 53 is linked to the function of the "row selection means" in claims 1 and 4 of the '449 patent. (CBr at 48.) Accordingly, it was further argued, given the level of knowledge of row decoders among those skilled in the art, the disclosed structure of row decoder 53 is sufficient to perform the recited function of the "row selection means" of the '449 patent. (CBr at 48.) However, the administrative law judge finds that the issue is not the level of knowledge of row decoders among those skilled in the art, but what the specification of the '449 patent discloses with respect to the embodiment that utilizes the circuit of Figure 17 of the '449 patent. The specification of the '449 patent identifies one component of the W1n1, ... W121, W111 signal as signals Z2 to Zm. (JX-7 at 11:34-35.) "Z2 to Zm" is the same identifier that the specification of the '449 patent uses to identify the signals generated by column decoder 55 in Figure 10 of the '449 patent. (JX-7 at 8:58-59.) In referring to signals Z2 to Zm with respect to the circuit of Figure 17, the specification of the '449 patent does not state that said signals originate from row decoder 53 of Figure 10, and in fact uses the

same identifier used for signals originating from column decoder 55 of Figure 10. Thus the administrative law judge finds that the specification of the '449 patent discloses that said signals originate from column decoder 55, not row decoder 53. Hence, the administrative law judge finds the issue of the level of knowledge of row decoders among those skilled in the art irrelevant in light of the specification of the '449 patent.

C. Asserted Claims Of The '178 Patent

1. A semiconductor memory device of multistage gate structure, comprising:

a semiconductor substrate;

a field oxidation film of a predetermined pattern formed on said semiconductor substrate, for defining element forming regions in which semiconductor elements are formed;

first gate electrodes formed on said element forming regions, the first gate electrodes being separated from each other by a predetermined width;

an insulating film formed to define grooves having substantially the same width between said first gate electrodes; and

a second gate electrode of superimposed-layer structure formed on said insulating film, made of a polysilicon layer formed on said insulating film and a high melting point metal layer or a silicide layer of a high melting point metal formed on the polysilicon layer, surfaces of those portions of said polysilicon layer which are above said grooves being substantially flat.

2. A semiconductor memory device according to claim 1, wherein those portions of said polysilicon layer which are above said element forming regions have a thickness larger than 1/2 said width of said grooves.

3. A semiconductor memory device according to claim 1 or 2, wherein said grooves are above said field oxidation film.

4. A semiconductor memory device according to claim 1 or 2, wherein said high melting point metal is one selected from a group of tungsten, molybdenum, copper, and titanium.

5. A semiconductor memory device, comprising:

a semiconductor substrate having semiconductor element regions;

first gate electrodes formed on said semiconductor element regions;

an insulating film formed on said first gate electrodes and defining grooves having a substantially same width between said first gate electrodes; and

a second gate electrode formed on said insulating film, said second gate electrode comprising (1) a polysilicon layer formed on said insulating film and filling in said grooves and (2) one of [either] a high melting point metal layer and a silicide layer of a high [metal] point melting on said polysilicon layer, a surface portion of said polysilicon layer at positions corresponding to said grooves being substantially planar.

1. Claim 1

a. "field oxidation film of a predetermined pattern"

The parties have put in issue the claimed phrase "field oxidation film of a predetermined pattern" which appears in the second clause of independent claim 1 of the '178 patent, which reads: "a field oxidation film of a predetermined pattern formed on said semiconductor substrate, for defining element forming regions in which semiconductor elements are formed." (JX-1 at 4:59-62 (emphasis added).)

At the outset, referring to the phrase "predetermined pattern" in the claimed phrase in issue complainant's expert Antoniadis testified:

> Q. Okay. The next claim term is claim 1, that you defined as predetermined pattern, can you explain your construction of that term?
>
> A. It's simply a pattern that is defined by a mask using the processing used in the fabrication of the devices.

(Antoniadis, Tr. at 445 (emphasis added).) Hence, the administrative law judge interprets the claimed phrase "predetermined pattern" as used in claim 1 to mean "a pattern defined by the

mask used in processing."[20]

Regarding the phrase "field oxidation film" in the claimed phrase in issue, complainant argued that said phrase should be construed to mean "an element isolation oxide film." (CBr at 108.) It is argued that the term "field oxidation film" is not a term that is commonly used in the art; and that said term is used frequently to refer to a process of oxidation of the field region, but that although said term is not commonly used to refer to a structure, because the term "field oxidation film" includes the word "film," it is clear that the inventor is referring to a structure. (Id. at 108.) It is further argued that complainant's construction of "field oxidation film" is also supported by the fact that the specification clearly indicates that the patentee did not intend to limit his invention to devices in which the "field oxidation film" is formed in a particular way; that the patent clearly identifies LOCOS (local oxidation of silicon) as just an example of a way in which a "field oxidation film" might be formed; that the specification states the "field oxidation film" is to be "formed by a known method"; that the drawings in the specification also indicate that the patentee contemplated that the "field oxidation film" could be formed by any known method; that while Figure 2C shows a field region formed by LOCOS, Figure 1C shows a field region that is formed in a much different way; that respondents' claim construction is wrong because it seeks to add a process limitation "formed by field oxidation" to a structural claim limitation in a device claim; and that because all of the claims in the '178 patent are device claims, the words used in those claims refer to a structure in a final product and are not limited

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[20] Complainant and respondents agreed that said phrase as used in claim 1 means a pattern defined by the mask used in processing. (TFF 826 (undisputed by respondents).) Respondents, in their reply brief, stated: "Because this language of the claim [predetermined pattern] by itself does not affect the outcome of the non-infringement or invalidity issues as argued by the parties, Hynix does not dispute the definition offered by Toshiba." (RRBr at 51.)

by any particular fabrication method or process. (Id. at 110-12.)

Respondents argued that the claimed phrase "field oxidation film" should be interpreted to mean "a field oxide layer formed by field oxidation, which is a process by which the field oxide is grown in the field region of the semiconductor substrate by the thermal oxidation of the substrate." (RBr at 74.) It is argued that there is absolutely no dispute between the parties that "field oxidation" has a common understanding to a person of ordinary skill in the art; that the standard oxidation process at the center of LOCOS results in a bird's beak structure; that persons of ordinary skill do not refer to the isolation region in any resulting STI (shallow trench isolation) structure as a "field oxidation film"; that Antoniadis testified that he himself would not refer to a STI structure as a "field oxidation film"; that the '178 patent specification described the invention as limited to field oxidation; that the '178 patent makes clear that the invention excludes any isolation oxide not formed by "field oxidation"; that field oxidation is the only isolation technology disclosed in the written description and figures of the '178 patent; that complainant does not even come close to carrying its heavy burden of showing that the '178 patentee was his own lexicographer with respect to the claim language "field oxidation film"; that the claim in issue uses the term "oxidation," which indisputably refers to a thermal oxidation process, not merely the resulting oxide film; that the '178 patent claims are riddled with "process" type language; and that terms such as "formed on" and the term "oxidation" itself invoke the character of process rather than product. (RBr at 74-82.)

The staff argued that the claimed phrase "a field oxidation film of a predetermined pattern" should be construed to mean "element isolation oxide film formed by an oxidation process," and that the patent did not modify said phrase from its ordinary meaning. (SBr at 11.)

The staff, however, also argued and proposed a finding that a "person of ordinary skill in the art would construe the term "field oxidation film" to mean a process of creating a film through thermal oxidation of silicon." (SBr at 11; SPFF 44, citing Antoniadis, Tr. at 514.) The staff further argued that neither the claim nor the specification use the term "birds beak" or otherwise mandates such a limitation; and that to the extent a "birds beak" is shown in the figures of the '178 patent, claims 1-5 are not limited to such figures. (SBr at 11-12.)

The '178 patent discloses an invention of a nonvolatile semiconductor memory device with a multigate structure. (TFF 722 (undisputed).) LOCOS and STI are each isolation technologies. (TFF 791 (undisputed).) Both LOCOS and STI use silicon dioxide as their isolation material. (TFF 792 (undisputed).) Trench isolation was a known process for forming element isolation in a semiconductor device at the time of the '178 patent. (TFF 824 (undisputed).) STI was also well known by one skilled in the art in 1990 as a means of obtaining element isolation and creating a field region. (TFF 780 (undisputed).)[21] In 1990, the predominant means of obtaining element isolation was the use of localized oxidation of the silicon substrate, or LOCOS. (Antoniadis, Tr. at 442.)

Although it is undisputed that while STI was known at the time of the '178 patent, STI is not disclosed anywhere in said patent. While complainant's expert Antoniadis testified that the '178 patent has a "special definition" for "field oxidation film" (Antoniadis, Tr. at 519-20), and

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[21] Several papers had been published prior to 1990 disclosing forms of STI. (TFF 784 (undisputed).) The concept of trench isolation was disclosed as early as 1984 in an IEDM paper prepared by employees of NEC, which described trench isolation as a method that might replace LOCOS. (TFF 785 (undisputed).) STI, the isolation technique used by both Toshiba and Hynix in their NAND flash devices, was disclosed by IBM researchers in a paper published in 1989, a full year before the priority date of the '178 patent. (TFF 786 (undisputed).)

presumably would include STI, Antoniadis testified with respect to STI:

> Q. Now, the patent doesn't say anything about shallow trench isolation [STI]; is that right?
>
> A. No.
>
> Q. It doesn't have STI somewhere hidden in the language of the claim or in the specification, does it?
>
> A. No.
>
> Q. And I think you said in your direct testimony that shallow trench isolation was known prior to the time of the patent; is that right?
>
> A. That's correct.
>
> Q. And yet the inventor here didn't describe that in his patent, did he?
>
> A. He did not. I - he didn't think it was relevant.

(Antoniadis, Tr. at 517:12-518:1 (emphasis added).) Thus, Antoniadis agreed that although STI was known prior to the '178 patent, STI is not disclosed anywhere in said patent.

In addition, complainant's expert Antoniadis admitted that a person of ordinary skill in the art "outside of the context of the patent," would interpret the claimed language "field oxidation film" to mean "a process of creating a film through thermal oxidation of silicon." Thus, Antoniadis testified as follows:

> JUDGE LUCKERN: Would you - well, let me - all right. But do you agree that people skilled in the art will look at this term, field oxidation film, and understand that to mean thermal oxidation of silicon?
>
> DR. ANTONIADIS: If it were completely outside the patent that we're describing, in other words, somebody was referring to a process step, that's the way we would understand it, yes.

(Antoniadis, Tr. at 551:15-23 (emphasis added).)

Notwithstanding that Antoniadis testified that the '178 patent has a "special definition" for "field oxidation film," the specification of the '178 patent makes only two references to the phrase "field oxidation film." The SUMMARY OF THE INVENTION section states: "a field oxidation film of a predetermined pattern formed on said semiconductor substrate, for defining element forming regions in which semiconductor elements are formed." The above passage in said SUMMARY section is identical, however, to the second clause of claim 1 in issue. However, describing manufacturing methods where the invention is applied to an EPROM cell array, the specification states:

> As shown in FIG. 2A, on a p-type silicon substrate 201, an element isolation oxide film (field oxidation film) 202 having a thickness of 500 nm is formed by a known method such as LOCOS (local oxidation of silicon), and a first gate oxide film 203 having a thickness of 20 nm is formed by a well-known method such as thermal oxidation.

(JX-1 at 3:26-32 (emphasis added).) Thus, the specification shows that an element isolation oxide film, which it equates to field oxidation film, is formed by a known method such as LOCOS (local oxidation of silicon). As seen from said language in the specification, "element isolation oxide film" is defined as "(field oxidation film)."[22]

Complainant relied on the language "formed by a known method such as LOCOS" to support its argument that the patent clearly identifies LOCOS as just an example of a way in which a "field oxidation film" might be formed and since STI was known at the time of the patent, that STI is also included within the meaning of how a "field oxidation film" might be

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[22] The language of the specification is the sole language which Antoniadis relied on for his departure from the ordinary meaning. (Antoniadis, Tr. at 520-21.)

formed. The administrative law judge, however, finds nothing in the specification to support complainant's argument. Significantly, complainant's expert Antoniadis agreed that there is no disclosure in the '178 patent specification of any other method for forming the "field oxidation film" other than LOCOS. Thus, Antoniadis testified:

> Q. Okay. And in the specification, there's no disclosure of any other methods for forming that field oxidation film other than LOCOS; is that fair?
>
> A. There is no direct disclosure, no.

(Antoniadis, Tr. at 508:7-11.)

Complainant argued that while Figure 2C shows a field region formed by LOCOS, Figure 1C shows a field region that is formed in a much different way. However, regarding the "field oxidation film" disclosed Figure 1C, respondents' expert Bravman testified:

> Q. And figure 1C, layer 2, field oxidation film is defining the actual areas; is that right?
>
> A. Yes.
>
> .....
>
> Q. How is it formed in figure 1C?
>
> A. It was probably formed by etching a recess in the substrate in a periodic fashion and then conducting a thermal oxidation.

(Bravman, Tr. at 2408:24-2409:10 (emphasis added).)

Also, with respect to the claimed phrase "field oxidation film," Antoniadis testified as follows:

> Q. Okay. So as I understand your construction, what you want this Judge to do, Judge Luckern, what you want him to do, you want him to cross out field, and I'm writing on the document now. I'm crossing out field and I'm crossing out

the word oxidation. Let me put a little arrow. I'm going to do a little insert here. I'm going to insert - what you want him to do is element isolation oxide, and film is there. So you want the Judge Luckern, when he does his ID in his case, you want him to cross out field oxidation, you want him to insert the words element isolation oxide; is that right?

A. No. No. All I want to do is change oxidation with oxide. Change the process with the structure. That's all I'm -- because the claim says four defining element forming regions. So obviously that is already included. So I wouldn't put it there.

Q. Okay. So you want him to cross out oxidation and put in oxide.

A. Correct.

Q. You think -- you think maybe the inventor messed that one up? He should have put oxide there instead of oxidation?

A. Frankly, yes. It's an improper use.

Q. And the problem is of course, as you understand it, is that the public is entitled to rely on what the inventor did in this claim. And we're not going to go around the public, that is, and cross out oxidation and put in oxide because the inventor messed that one up. You understand how that works; is that right?

A. I understand how that works.

(Antoniadis, Tr. at 522:9-523:18 (emphasis added).) Significantly, as admitted by Antoniadis, the specification equates "element isolation oxide film" to "field oxidation film." (Antoniadis, Tr. at 520-21.)

The ordinary meaning for the claimed phrase "field oxidation film," as admitted by complainant's expert Antoniadis (Antoniadis, Tr. at 551:15-23), i.e., "thermal oxidation of

silicon," is consistent in the context of the '178 patent, which "relates to a semiconductor memory device and a method of manufacturing the same." (JX-1 at 1:7-9.) Absent a clear and deliberate preference for an alternate definition, claim terms are given their ordinary definition. Renishaw PLC v. Marposs Societa Per Azioni, 158 F.3d 1243, 1249 (Fed. Cir. 1998). See also Lear Siegler, Kumar, and Bell Atlantic, supra. The administrative law judge finds nothing in the disclosure of the '178 patent which gives notice of the inventor's use of an alternate definition of "field oxidation film."

Complainant argued that respondents' claim construction is wrong because it seeks to add a process limitation, viz, "formed by field oxidation," to a structural claim limitation in a device claim, and the words used in said claim are not limited by any particular fabrication method or process. Claim 1 in issue, however, uses the phrase "field oxidation film," not "formed by field oxidation." The phrase "field oxidation film" would be interpreted by a person of ordinary skill in the art as "a process of creating a film through thermal oxidation of silicon." (See Antoniadis, Tr. at 551:15-23; and Bravman, Tr. at 2408:24-2409:10, supra.)

Additionally, Antoniadis referred to the process of manufacture as important to the meaning of the claims. Thus, Antoniadis testified:

> Q. And to create this, you have a mask that's put over the underlying silicon substrate 201. And that's exposed to oxygen at high temperature. And you go through an oxidation process; is that right?
>
> A. In a few words, yes.
>
> Q. And that's field oxidation?
>
> A. That would be a process of field oxidation, yes.

Q. The reason it's a process of field oxidation is you're oxidizing the underlying silicon in the field, so to speak, right there on the substrate?

A. Yes.

* * *

Q. Okay. Let me ask it again one at a time. When we look at the claim and we look at the words field oxidation, it is your opinion that you've got to look at the method on how you got there – let me make sure I got it right, too – the method by which you got there and what it actually does; is that right?

A. Yes.

(Antoniadis, Tr. at 517:4-11 (emphasis added); Tr. at 505:17-506:5 (emphasis added).)

Based on the foregoing, the administrative law judge interprets the claimed phrase "field oxidation film of a predetermined pattern" to mean "a field oxide layer formed by field oxidation, which is a process by which the field oxide is grown in the field region of the semiconductor substrate by the thermal oxidation of the substrate."

b. "element forming regions"

The claimed phrase "element forming regions" appears in the second clause of independent claim 1 of the '178 patent, which reads: "a field oxidation film of a predetermined pattern formed on said semiconductor substrate, for defining element forming regions in which semiconductor elements are formed." (JX-1 at 4:59-62 (emphasis added).)[23]

Complainant argued that its expert Antoniadis testified that one of ordinary skill in the art

[23] The phrase "element forming regions" also is found in the third clause of claim 1. However, the third clause recites "said element forming regions" and hence is referring back to the phrase as recited in the second clause.

would understand the claim term "element forming regions" to mean "active areas of the device topped by a non-conductive film"; and that complainant's proposed construction is supported by both respondents' and complainant's witnesses who testified that the tunnel or gate oxide is part of the silicon substrate or active area; and that a device without a non-conductive film separating the floating gate from the active area would not work. (CBr at 114.) Complainant also argued that the only difference between the parties' respective constructions is that respondents' expert Bravman improperly includes references to the "field oxidation film" in his proposed construction; that Bravman's approach is needlessly repetitive and redundant because the claim already discloses that the "field oxidation film" is "for defining element forming areas"; that respondents' only purpose for offering this redundant construction is to use a similar phrase to read "field oxidation film" into claim 5; and that such construction would be wrong as a matter of law. (CRBr at 81.)

Respondents argued that "Hynix agrees that claim 1 should be construed to be operable, and thus, 'element forming region' should be construed to mean an active area with a non-conductive film on top." (RRBr at 51.)

The plain language of the claimed second clause "a field oxidation film of a predetermined pattern formed on said semiconductor substrate, for defining element forming regions in which semiconductor elements are formed" indicates that a "field oxidation film" is the isolation structure which defines the "element forming regions." Moreover, the administrative law judge finds that a person of ordinary skill in the art would interpret the claimed phrase "element forming regions" to mean "active areas of the device topped by a non-conductive film" to make claim 1 operable. Thus, a semiconductor device would not

properly operate without a non-conductive film separating the first gate electrode from the active area of the substrate. (TFF 829 (undisputed).) Also, the private parties agreed that claim 1 should be construed to be operable, and thus, the claim phrase "element forming region" should be construed to mean "an active area with a non-conductive film on top." (RRBr at 51; CBr at 114.) Hence, the administrative law judge finds that a person of ordinary skill would construe the claimed phrase "element forming regions" to mean "active areas of the device topped by a non-conductive film."

Respondents argued that their proposed construction recognizes that an active area must be defined by an isolation structure and the only isolation structure recited in claim 1 and disclosed by the '178 patent is a field oxidation film. (RRBr at 51.) However, the plain language of claim 1 recites "a field oxidation film... for defining element forming regions." As already found, supra, "a field oxidation film" would relate to "a field oxide layer formed by field oxidation, which is a process by which the field oxide is grown in the field region of the semiconductor substrate by the thermal oxidation of the substrate."

c. "first gate electrodes formed on said element forming regions"

The claimed phrase "first gate electrodes formed on said element forming regions" appears in the third clause of independent claim 1 of the '178 patent, which reads: "first gate electrodes formed on said element forming regions, the first gate electrodes being separated from each other by a predetermined width." (JX-1 at 4:63-65 (emphasis added).)[24]

Complainant argued that the claimed phrase "first gate electrodes formed on said element

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[24] The administrative law judge, supra has construed the claimed phrase "element forming regions" to mean "active areas of the device topped by a non-conductive film."

forming regions" should be construed to mean: "floating gate electrodes formed on said element forming regions."

Respondents argued that the claimed phrase "first gate electrodes formed on said element forming regions" should be construed to mean: "a conductive layer of each first gate electrode is formed on the element forming regions." Moreover it is argued that "the '178 patent limits 'first gate electrodes' to a particular type of floating gate," and that a "floating gate electrode" is limited to a single conductive layer. (RBr at 83.) Hence, respondents at least concede that "first gate electrodes" are "floating gates" of some type. The issue is whether the '178 patent limits "first gate electrodes" to a particular type of floating gate electrode.

The plain language of the claimed phrase in issue "first gate electrodes formed on said element forming regions" requires that the "first gate electrodes" be formed on the "element forming regions." In addition while the specification's description of a preferred embodiment, as shown in Figure 2A, states that "[a] first polysilicon layer 204 forming a floating gate electrode of a first level layer is formed thereon..." (JX-1 at 3:32-33), the ABSTRACT of the '178 patent states that

> "[t]hose portions of the second polysilicon layer which are above the element forming regions have a thickness larger than 1/2 the width of grooves formed between adjacent first gate electrodes (floating gate electrodes), so that the grooves are filled with the second polysilicon layer to flatten the surfaces of those portions of the second polysilicon layer which are above the grooves."

(JX-1 (emphasis added).) Thus, the ABSTRACT section equates "first gate electrodes" with "floating gate electrodes." Further, in the Description of the Related Art section of the specification of the '178 patent, describing Figure 1A, the specification discloses that "[a] first

polysilicon layer 5 serving as a first level gate electrode (floating gate electrode) is formed on the resultant semiconductor structure." (JX-1 at 1:25-28 (emphasis added).) Hence, in the description of Figure 1A, a "first level gate electrode," i.e., "first gate electrode," is again equated with a "floating gate electrode."

In addition, respondents' expert Bravman conceded on cross examination (when confronted with his deposition testimony) that "first gate electrodes" would be understood by one of ordinary skill in the art to be a floating gate. Thus, Bravman testified:

> Q. Page 57. At your deposition, Professor Bravman, I asked you the next element of claim 1, first gate electrodes, is that a reference to the floating gate? Your answer was: The -- the first gate electrodes, one would understand to be what's commonly called a floating gate. Do you recall giving that testimony at your deposition?
>
> A. Oh, 58. Page 58. I don't recall it, but I see it here. I think that's consistent with what I'm saying. One would understand that, when the structure, the memory device described in '178 was built, the first layer electrode goes on to serve the purpose of the floating gate, as commonly understood.

(Bravman, Tr. at 2412-13 (emphasis added).)

Respondents argued that because the claims provide that the "second gate electrode" is formed of a "superimposed-layer structure," the first gate electrode must be limited to one layer because it is not claimed to be formed of a "superimposed-layer structure." (RBr at 83.) The administrative law judge rejects this argument because there is no limitation on the claimed phrase "first gate electrodes."

Based on the foregoing, the administrative law judge interprets the claimed phrase "first gate electrodes formed on said element forming regions" to mean "floating gate electrodes

formed on said element forming regions."

d. "first gate electrodes being separated from each other by a predetermined width"

The claimed phrase "first gate electrodes being separated from each other by a predetermined width" appears in the third clause of independent claim 1 of the '178 patent, which reads: "first gate electrodes formed on said element forming regions, the first gate electrodes being separated from each other by a predetermined width." (JX-1 at 4:63-65 (emphasis added).)

Complainant argued that the claimed phrase "first gate electrodes being separated from each other by a predetermined width" should be construed to mean "the width between the floating gate electrodes that is intended by the designer within a certain level of tolerance that the particular process technology is able to deliver." (CRBr at 82.) In support, it is argued that there will always be some variation from rectangular-shaped separations between floating gates; that there are many different groove shapes in semiconductor manufacturing, including v-shaped grooves, U-shaped grooves, and even kettle shaped grooves; that given that the shape of the groove is typically the same as the shape of the separation between floating gates (modified only by the thin insulating film that is deposited conformally over and on the side of the floating gates), it follows that the "predetermined" separation between floating gates can be any number of different shapes. (CRBr at 84.)

Respondents argued that the claimed phrase "first gate electrodes being separated from each other by a predetermined width" should be construed to mean "a single predetermined separation between adjacent first gate electrodes; that is, the same separation exists at any point along an axis perpendicular to the width of the separation." In other words, "the predetermined

width is rectangular shaped." (RBr at 84.) In support, it is argued that a person of ordinary skill would review the '178 patent and realize the intent of the disclosed process is to form straight sidewalls between floating gates using anisotropic etching; that anisotropic etching results in rectangular shaped separations between the floating gates, albeit not perfect rectangles as Toshiba notes; and that while it may be true that a perfect rectangular may not be formed in practice, that is simply a manufacturing tolerance issue having nothing to do with the appropriate claim construction. (RRBr at 55.)

The staff argued that the claimed phrase "predetermined width" should be construed to mean "'predetermined separation between gate electrodes' that is not limited to a single width or a rectangular separation." (SBr at 13.)

At the outset, it is uncontroverted that the claimed phrase "predetermined width" carries the "notion" of pre-design and non-randomness of said width. (Antoniadis, Tr. at 447:5-11; Bravman, Tr. 2389:8-12.) In issue is whether the claim phrase require a rectangular separation between floating gates.

The claims of the '178 patent do not state that there must be a rectangular separation between first gate electrodes. (JX-1.) Moreover, the words "rectangle" or "rectangular" appear nowhere in the patent. (JX-1.) While drawings in the specification show a rectangular separation between first gate electrodes, the administrative law judge finds no language in the claim in issue or in the specification of the '178 patent which requires a rectangular separation between first gate electrodes. Moreover, it is common in the industry to refer to the width of an active area by a single width despite the fact that there would be a gradual transition between the thin oxide and the thick oxide of the field. Thus complainant's Antioniadis testified:

Q. In your view, does this claim term require that the space between the floating gates be a rectangle?

A. I don't think it requires that.

Q. And why not?

A. It is not specified anywhere in the patent that this should be a rectangular gap. Moreover, a gap of that kind is unlikely to be perfectly rectangular because it depends on an etch, which is designed to be typically anisotropic, but can have a fair amount of variation for – from perfect rectangular shape.

Q. Is it common in the industry to refer - - to use a single width to refer to an element or a gap that is not perfectly rectangular?

A. It is not uncommon. It is not uncommon. Let me give you some examples.

The width of the active area of the transistor often is referred to by a single width, despite the fact that there would be a gradual transition between the thin oxide and the thick oxide of the field.

A width of the STI region, for example, all of the field region for that matter, can be referred to with a single width. And then it would be understood what it means. It means that it is the relevant part of the device. In this particular case, the top.

(Tr. at 447-8 (emphasis added).)

Also, the claim language at issue, which is not limited by the embodiment of dependent claim 2, references a width that separates gate electrodes "from each other" and the specification refers to "predetermined width" as being a width that separates the gate electrodes "from each other." (JX-1 at 2:31-32, 2:48-50.) The administrative law judge finds nothing in the '178 patent that states that "width" or "predetermined width" should be used only to define the width that

exists along the vertical axis of the side of a single gate electrode. In addition, the fact that claim 1 recites "a predetermined width," the administrative law judge finds, would indicate to one of ordinary skill in the art that the gate electrodes must be separated from each other by a width that is measured at one point along the sidewall of the gate.

Based on the foregoing, the administrative law judge finds that a person of ordinary skill in the art would interpret "first gate electrodes being separated from each other by a predetermined width" as a predetermined separation between first gate electrodes that is not limited to a single width or a rectangular separation and with the width determined prior to the final product as opposed to randomly occurring.

e. "an insulating film formed to define grooves"

The claimed phrase "an insulating film formed to define grooves" appears in the fourth clause of independent claim 1 of the '178 patent, which reads: "an insulating film formed to define grooves having substantially the same width between said first gate electrodes." (JX-1 at 4:66-68 (emphasis added).)

Complainant argued that the claimed phrase "insulating film" means a "film that provides electrical isolation between electrically conductive materials." (CBr at 125-27.) It is argued that "[t]he critical dispute here is whether a multilayered film, such as an ONO structure, can qualify as an insulating film within the meaning of the patent." (CRBr at 67.)

Respondents argued that the claimed phrase "an insulating film formed to define grooves" means "a non-conductive film that defines grooves between adjacent first gate electrodes." (RBr at 88-90.) Respondents argued that "[t]he debate here centers around the issue of whether the claimed insulating film can be applied in such a way as to cover the accused

products that use a three-film ONO structure." (RBr at 89.)

The staff argued that the claimed phrase "an insulating film formed to define grooves" means "a non-conducting film that defines grooves between adjacent first gate electrodes and that may be multi-layered." (SBr at 13-14.) According to the staff, "[t]he key issue appears to be whether a multi-layer material such as ONO can be considered a film as used in the claim." (SBr at 13.)

The plain language of the claimed phrase "an insulating film formed to define grooves" in issue, shows that the grooves are defined by an "insulating film." Moreover the claim term "insulating film" is not limited in the claim to a structure that has only one layer.

As respondent's Bravman testified:

> Q. The claim does not say a one-layer insulating film, does it?
>
> A. That language does not appear in the patent; that's right.

(Tr. at 2350.)

In the Description of the Related Art section, the specification of the '178 patent states:

> Moreover, when the control gate layer is etched, the refractory metal or the refractory metal silicide layer and the first polysilicon layer are etched. In this case, when the refractory metal layer or the refractory metal silicide layer and the first polysilicon layer are etched, etching conditions are preferably often changed from a point of view of an etching shape and selectivity of the an underlying insulating film.

(JX-1 at 1:66-2:5 (emphasis added).) Also, the SUMMARY OF THE INVENTION section discloses the claimed phrase "insulating film" several times. (JX-1 at 2:15-3:6.) Said portions of the specification do not limit insulating film to a one-layer insulating film.

Describing a preferred embodiment as shown in Figure 2B, the specification does state in part:

> Thereafter, as shown in FIG. 2B, a first oxide film 206 is formed over the semiconductor structure by a known method such as a thermal oxidation method to isolate the gate electrodes 20 of the first level layer from a gate electrode (control gate electrode) of a second level layer formed at a later step. In this time, channels or grooves 205 defined by the oxide film 206, having substantially the same width are formed on the element isolation oxide film 202. In other words, channels or grooves 205 are formed between adjacent floating gate electrode 204.

(JX-1 at 3:39-49 (emphasis added).) The written description however is describing a preferred embodiment where "first oxide film 206" is merely an example of an oxide film in the specification, whereas claim 1 requires only an "insulating film."

Respondents argued that the "'178 patent simply does not disclose, claim, describe, or illustrate a multi-film insulating structure." (RBr at 89.) However, the administrative law judge can find nothing in the '178 patent that requires that multi-film insulating structures should be excluded from the claim. Also published articles at the time of the invention referred to multi-film insulating structures as insulting film. See CX-101, RX-943. Moreover , it is not denied that respondents' own engineering documents refer to the ONO structure as a "film." (TFF 893-94, 911-12 (all (undisputed).)

Based on the foregoing, the administrative law judge interprets the claimed phrase "an insulating film formed to define grooves" to mean "a non-conductive film that defines grooves between adjacent first gate electrodes where said film may be multi-layered."

f. "grooves having substantially the same width between said first gate electrodes"

In issue is the claimed phrase "grooves having substantially the same width between said

first gate electrodes," which appears in the fourth clause of independent claim 1 of the '178 patent and reads: "an insulating film formed to define grooves having substantially the same width between said first gate electrodes." (JX-1 at 4:66-68 (emphasis added).)

Complainant argued that said claimed phrase can be construed to mean that the width of each groove is approximately the same between adjacent gates within a level of tolerance that the particular process technology is able to deliver. (CRBr at 89.)

Respondents argued that the claimed phrase "grooves having substantially the same width between said first gate electrodes" means "grooves defined by the insulating film between adjacent first gate electrodes have the same single width, within manufacturing tolerances." (RBr at 90.) In other words, it is argued that this claim language simply means that the insulating film defines rectangular-shaped grooves between adjacent first gate electrodes viewed "along the wordline" and that all the rectangular-shaped grooves have the same width. (Id.)

The staff argued that the claimed phrase "substantially the same width" means "substantially the same separation between gate electrodes." In other words, it is argued that since there are multiple grooves in a memory device, the separation between the gate electrodes for each groove must be substantially the same. (SBr at 15.)

Claim 1 in issue reads in part:

> A semiconductor memory device of multistage gate structure, comprising:
>
> a semiconductor substrate;
>
> a field oxidation film of a predetermined pattern formed on said semiconductor substrate, for defining element forming regions in which semiconductor elements are formed;

> first gate electrodes formed on said element forming regions, the first gate electrodes being separated from each other by a predetermined width;
>
> an insulating film formed to define grooves having substantially the same width between said first gate electrodes...

(JX-1 at 4:56-68 (emphasis added).) The plain language of the claimed phrase "grooves having substantially the same width between said first gate electrodes" shows that the grooves between said first gate electrodes have substantially the same separation between said first gate electrodes. Moreover, the plain language of the entire fourth clause shows that said grooves are defined by insulating film.

The administrative law judge has construed, supra, the claimed phrase "first gate electrodes being separated from each other by a predetermined width" recited in claim 1, as a predetermined separation between first gate electrodes that is not limited to a single width or a rectangular separation and with the width determined prior to the final product as opposed to randomly occurring. The administrative law judge, based on his finding that said phrase "first gate electrodes being separated from each other by a predetermined width" is not limited to a single width or a rectangular separation, finds that the claimed phrase "grooves having substantially the same width between said first gate electrodes" in issue, is not limited to a single width or a rectangular separation.

The private parties disagree on the claim interpretation of the term "between" as recited in the claimed phrase "grooves having substantially the same width between said first gate electrodes" in issue. Complainant, relying on its expert Antoniadis, argued that the "groove" is "between" the floating gates in the sense that said groove separates said floating gates from each

other, which necessarily means that said grooves are on the same plane as said floating gates. (CBr at 131.) Respondents, relying on Figure 3 of the '178 patent, argued that the '178 patent does not impose a co-planarity requirement on the term "between" as recited in the claimed phrase "grooves having substantially the same width between said first gate electrodes." (RRBr at 61-64.)

In the SUMMARY OF THE INVENTION section, the specification states:

> According to the present invention, there is provided a semiconductor memory device of multistage gate structure, comprising...
>
> an insulating film formed on the semiconductor structure to define grooves having substantially the same width between said first gate electrodes.

(JX-1 at 2:22-36.) Thus, the specification discloses that "grooves having substantially the same width" are "between said first gate electrodes." Further, as shown in Figure 2B, the specification states:[25]

> Thereafter, as shown in FIG. 2B, a first oxide film 206 is formed over the semiconductor structure by a known method such as a thermal oxidation method to isolate the gate electrodes 20 of the first level layer from a gate electrode (control gate electrode) of a second level layer formed at a later step. In this time, channels or grooves 205 defined by the oxide film 206, having substantially the same width are formed on the element isolation oxide film 202. In other words, channels or grooves 205 are formed between adjacent floating gate electrode 204.

(JX-1 at 38-49.) Hence, the specification discloses that "grooves 205... having substantially the same width"... "are formed between adjacent floating gate electrode 204."

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[25] The specification states: "FIGS. 2A-2C are views showing steps in manufacturing a semiconductor memory device according to an embodiment of the present invention." (JX-1 at 3:11-13.)

The administrative law judge rejects respondents' argument that the '178 patent does not impose a co-planarity requirement on the term "between" as recited in the claimed phrase "grooves having substantially the same width between said first gate electrodes." Respondents relied on Figure 3 of the '178 patent for their assertion that the floating gate electrodes are "between" the source 210_1 and the drain 210_2. However, the plain language of the claimed phrase "grooves having substantially the same width between said first gate electrodes" in issue shows that the grooves must be between the "first gate electrodes," not between the source 210_1 and the drain 210_2. Figure 3, which respondents rely on for their argument that the '178 patent does not impose a co-planarity requirement on the term "between" as recited in the claimed phrase in issue, does not even disclose grooves 205 between first gate electrodes because Figure 3 is a cross section view of Figure 2C.[26] Figures 2B and 2C, however, shows the grooves 205 located between the floating gate electrodes 204, where said grooves 205 are substantially on the same plane as said floating gate electrodes 204. Moreover, as indicated, supra, the specification discloses that "grooves 205... having substantially the same width"... "are formed between adjacent floating gate electrode 204."[27]

Based on the foregoing, the administrative law judge interprets the claimed phrase "grooves having substantially the same width between said first gate electrodes" to mean that grooves between said first gate electrodes have substantially the same separation that is not

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[26] The specification states: "FIG. 3 is a view taken along the line III–III in FIG. 2C." (JX-1 at 3:14-15.)

[27] The administrative law judge already construed, supra, the claimed phrase "first gate electrodes formed on said element forming regions" to mean "floating gate electrodes formed on said element forming regions." Thus, he equated "first gate electrodes" to "floating gate electrodes."

limited to a single width or a rectangular separation, and said "grooves" must be "between" said first gate electrodes (floating gate electrodes) in the sense that said grooves are in the spaces that separate said floating gate electrodes, where said grooves are substantially on the same plane as said floating gate electrodes.

g. "substantially flat"

The claimed phrase "substantially flat" appears in the fifth clause of independent claim 1 of the '178 patent, which reads: "a second gate electrode of superimposed-layer structure formed on said insulating film, made of a polysilicon layer formed on said insulating film and a high melting point metal layer or a silicide layer of a high melting point metal formed on the polysilicon layer, surfaces of those portions of said polysilicon layer which are above said grooves being substantially flat." (JX-1 at 5:1-8 (emphasis added).)

Complainant, relying on its expert Antoniadis, argued that the claimed phrase "substantially flat" should be construed to mean:

> Relatively flat as compared to the conventional structure described in the patent in which the polysilicon layer contained a recess above the separating groove. In other words, a layer that is "substantially flat" eliminates or substantially attenuates the topographical features of the underlying structures.

(CBr at 133.) It is argued that one of ordinary skill in the art would not expect to see a surface in an actual semiconductor device that looks like the stylized flat line shown in Figure 2C because the surface at issue is an interface between crystalline materials that can interact with each other; that during thermal processing, there is grain growth and evolution that will create texture at that surface that will be random and will mirror the crystallite evolution; that the random variation will not amount to a systematic recess or feature that is associated with the underlying

topography; and thus it is important to recognize that the claim term "substantially flat" refers to topographical features, and not to the texture of the interface between the polysilicon and metal or silicide layer, as that interface will inevitably contain some roughening and grain growth caused by the chemical reaction between the two materials. It was further argued by complainant that the problems addressed and solved by the '178 patent would reinforce to one of ordinary skill in the art that the claim term "substantially flat" is intended to measure the topography, and not the texture, of the polysilicon surface. (Id. at 134-135.) In addition, it was argued that the proper time to measure "substantially flat" is in a completed NAND flash device. (Id. at 162-63.)

Respondents argued that the claimed phrase "surfaces of those portions of said polysilicon layer which are above said grooves being substantially flat" should be construed to mean "the surface of the polysilicon layer above the groove... is substantially characterized without peaks or depressions so as to prevent disconnection of the metal or silicide layer." (RBr at 93-94.) It is argued that respondents' claim interpretation is consistent with the ordinary meaning of flat, "being or characterized by a horizontal line or tracing without peaks or depressions"; and that the '178 patent specification provides a standard for measuring the required degree of flatness, i.e., the degree to which a surface must be characterized without peak or depressions; and that the standard articulated is whether the control gate polysilicon surface is substantially flat after deposition of the polysilicon layer above the grooves and before subsequent processing so that the desired result of avoiding cracking or disconnection is achieved. (Id. at 94.) Respondents also argued that the proper time to measure "substantially flat" is at an intermediate processing step just after deposition of the second gate polysilicon layer and before any further processing steps are carried out. (Id. at 173-76.)

The staff agreed with complainant that the claimed phrase "substantially flat" should be construed to mean "flat enough to eliminate or substantially attenuate the topographical features of the underlying structures." (SBr at 15-16.) As to the private parties' disagreement about when said flatness should be determined, the staff argued that the flatness should be determined "after the polysilicon layer is deposited but prior to subsequent processing." (Id. at 17-18.)

The specification of the '178 patent identifies three different problems for obtaining a conventional EPROM with the topography of the non-flat surface of polysilicon layer 8 above groove 9 in Fig. 1C.[28] (JX-1 at 1:35-2:13; Antoniadis, Tr. at 415-22.) First, the uneven surface of the polysilicon layer can lead to mechanical stress on the metal or metal silicide layer subsequently formed on the polysilicon layer 8, which can lead to disconnects or high resistance. (TFF 993 (undisputed).) Second, the non-flat, non-planar surface of polysilicon layer 8 above the groove 9 can make it difficult subsequently to form a uniform metal or metal silicide layer. (TFF 994 (undisputed).) Third, when a metal or metal silicide layer is formed on the non-flat, non-planar surface of the polysilicon layer 8 shown in FIG. 1C, the metal or metal silicide layer may deposit more thickly on the polysilicon layer 8 above the groove. Subsequent etching of the metal or metal silicide layer can require excessive etching to remove the thicker portions of the metal or metal silicide layer in a way that eventually leads to overetching and damage to the control gate polysilicon layer 8. (TFF 995 (undisputed).) Thus, it is undisputed and one of ordinary skill in the art would find that the '178 patent discloses that there is a problem with the overlayer of metal or metal silicide layer in the conventional devices as a result of the underlying

[28] The '178 patent discloses that "FIGS. 1A-1C are views showing steps for obtaining a conventional EPROM." (JX-1 at 3:9-10.)

topography. (RPFF 3284 (undisputed).) All parties agree and a person of ordinary skill in the art would know that the uneven surface of the polysilicon layer can lead to mechanical stress on the metal or metal silicide layer subsequently formed on the polysilicon layer 8, which can lead to disconnects or high resistance. (TFF 993 (undisputed).)

Moreover, one of ordinary skill in the art would know that the claimed phrase "substantially flat" does not require exact flatness. Thus, it is undisputed that the claimed phrase "substantially flat" does not require perfect flatness or anatomic flatness and both complainant's expert Antioniadis and respondents' expert Bravman agreed. (TFF 976 (undisputed).) Importantly, respondents' expert Bravman testified that substantial flatness cannot be viewed as perfect flatness or anatomical flatness because "[w]e all know that...matter is granular." (TFF1001 (undisputed).) Figures 2A-2C "are views showing steps in manufacturing a semiconductor memory device according to an embodiment of the present invention." (JX-1 at 3:11-13.) In the prior art shown in Figure 1C of the '178 patent, there is a groove that has a recess above it that mirrors the underlying topography of the step at the edge of the floating gates. (Antoniadis, Tr. at 451.) In contrast, Figure 2C shows the solution of the patent wherein the polysilicon of the control gate fills the grooves defined by the insulating film and the surface of that polysilicon is substantially flatter above the groove. (Antoniadis, Tr. at 452.) In the solution shown in Figure 2C, the underlying topography has been eliminated and there is no systematic repetition of a recess that is associated with the grooves. (Antoniadis, Tr. at 451-52.) Hence, the administrative law judge finds that the claimed phrase "substantially flat" refers to topographical features, and not to the texture of the polysilicon layer.

The administrative law judge rejects respondents equating "substantially flat" to

"substantially characterized without peaks or depressions." Respondents' proposed construction is based in part on a dictionary definition of the term "flat" printed off a website on June 20, 2006. (RX-93, definition 2b states: "being or characterized by a horizontal line or tracing without peaks or depressions".) The administrative law judge finds that this 2006 standard dictionary definition of "flat" cannot establish the meaning of the claimed phrase "substantially flat" in 1990, particularly since one of ordinary skill in the art would understand the flatness of the polysilicon layer in a much different way than flatness is understood in everyday conversation. The administrative law judge also rejects respondents equating "substantially flat" to "so as to prevent disconnection of the metal or silicide layer." Respondents' expert Bravman admitted that cracking in the silicide layer can be caused by other phenomena despite achieving substantial flatness of the polysilicon layer. (TFF1014 (undisputed).) Bravman also admitted that the metal cracking problem can be solved even without having a substantially flat polysilicon layer. (Bravman, Tr. at 2376-77.)

As for where and when said flatness should be determined, respondents' Bravman and complainant's Antoniadis agreed on the area where substantial flatness should be measured for purposes of the asserted claims. (RPFF 3298 (undisputed).) Also, complainant's Antoniadis testified that substantial flatness is determined at the interface between the polysilicon layer and the metal layer along the entire width of the groove above the groove. (RPFF 3299 (undisputed).)

With respect to when flatness should be determined, respondents' Bravman testified that the only way for a person of skill to determine whether the "substantially flat" limitation has been met is to study the polysilicon film by performing tests after it has been deposited and before any further processing occurs. (Bravman, Tr. at 2179, 2368-69, 2375, 2434-35.) Consistent with

Bravman's testimony, Antoniadis testified at his deposition that the proper time to determine flatness is after the poly layer is deposited. (Antoniadis, Tr. at 624-627.) At the hearing, however, he testified that the proper time was at the completion of the final product because the claim is a product claim, not a process claim. (Id.) However, an engineer of ordinary skill cannot tell from examining the final product if the poly layer is flat enough to meet the claim limitation because (1) etching has occurred which may smooth the surface, and (2) crystals grow after the metal layer has been deposited, and during thermal processing, in the natural course of building the device. (Bravman, Tr. at 2178-81; Antoniadis, Tr. at 640-42.) Also, Antoniadis testified that etching may in some circumstances cause smoothing of the poly layer. (Antoniadis, Tr. at 638-40.) Significantly, he testified that he could not tell how smooth the poly surface was before crystals had grown except that it would have been flatter than what is shown in a TEM or SEM photo of a final device. (Antoniadis, Tr. at 641-42.) Hence, the administrative law judge finds that substantial flatness should be determined after the polysilicon layer is deposited but before any subsequent processing.

The administrative law judge rejects complainant's assertion that since the patent is a product patent and not a process patent, the only time at which an accused device can be evaluated is at the final product and thus the determination of whether the "surfaces of those portions of said polysilicon layer which are above said grooves being substantially flat" can be made only after the silicide layer is deposited on top of said polysilicon layer. The Federal Circuit has found that even purely product claims can be evaluated at any point during the manufacturing process in order to determine infringement. Thus, in Exxon Chemical Patents, Inc. v. Lubrizol Corp., 64 F.3d 1553 (Fed. Cir. 1995) (Exxon), the Court stated:

> Under Lubrizol's view of the claims, as asserted at trial and on appeal, the composition claimed by Exxon is limited to the final product made and ready for use in the engine environment. Lubrizol is correct that the claims read on a product, not simply a recipe, but Lubrizol errs in thinking that the claims read only on end product compositions.

(64 F.3d at 1558.) The claims in Exxon were product claims, not product by process claims. Importantly, the plain language of claim 1 of the '178 patent in issue specifically recites that the "surfaces of those portions of said polysilicon layer which are above said grooves being substantially flat" (emphasis added). The term "said polysilicon layer" in the claim does not include the "high melting point metal layer or a silicide layer of a high melting point metal" which said claim requires be formed on the polysilicon layer. If the inventor intended that said polysilicon layer include the subsequent layer, the inventor had the opportunity to so state, viz., said polysilicon layer with the subsequent layer being substantially flat. However, the inventor chose to limit the flatness term to "said polysilicon layer." Moreover, the substantial flatness of the polysilicon layer may be affected after the subsequent layer is formed on it. Thus, complainant's expert Antoniadis testified that etching in the formation of the high melting point metal layer may in some circumstances cause smoothing of the polysilicon layer (Tr. at 638-40) and that he could not tell how smooth the polysilicon surface was before crystals had grown except that it would have been flatter than what is shown in a TEM or SEM photo of a final device. (Tr. at 641-42.) Hence, substantial flatness of said polysilicon layer can be affected depending on when the "substantially flat" determination is made.

Based on the foregoing, the administrative law judge (1) interprets "substantially flat," as it appears in the claimed phrase "surfaces of those portions of said polysilicon layer which are

above said grooves being substantially flat," as a surface which substantially eliminates the topographical features of the underlying structure and thus does not require perfect flatness or anatomic flatness, and (2) finds that the substantial flatness should be determined after the polysilicon layer is deposited but before any subsequent processing.

2. Claim 5

a. "semiconductor element regions"

In issue is the claimed phrase "semiconductor element regions," which appears in the first clause of independent claim 5 of the '178 patent and reads: "a semiconductor substrate having semiconductor element regions." (JX-1 at 5:22-23 (emphasis added).)[29]

Complainant, relying on its expert Antoniadis, argued that the claim phrase "semiconductor element regions" means "active regions separated by field regions on the semiconductor substrate and topped by a non-conducting film." (CBr at 141.) Complainant further argued that the issue is whether the claim phrase "field oxidation film" should be read into claim 5 from claim 1; that the parties agree that these regions must be topped by a non-conductive film and must be separated by some type of isolation structure; that consistent with established Federal Circuit law, complainant contends that it is inappropriate to read this term into claim 5; and that one of ordinary skill in the art would understand that "some kind of isolation structure" is required, and that "isolation structure" could include STI. (CRBr at 61-62.)

Complainant further argued that the conclusion that "semiconductor element regions" should not be defined to include a "field oxidation film" is also supported by the fact that on

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[29] The phrase "semiconductor element regions" is also found in the second clause of claim 5. However, the second clause recites "said semiconductor element regions" and hence is referring back to the phrase as recited in the first clause.

January 16, 1992, the patentee filed a supplemental information disclosure statement (the supplemental IDS) which disclosed three references, one of which was the Sugatani '676 publication which discloses a form of trench isolation; that on the same day that the inventor disclosed the Sugatani reference to the PTO, he also submitted a new claim (originally numbered claim 9, but which later became claim 5 in the issued patent) that made no reference whatsoever to a "field oxidation film"; and that accordingly, it is reasonable to infer that the patentee specifically intended claim 5 to cover devices in which the field region could be any of various isolation structures, including those formed by some type of trench isolation process. (CBr at 143.)

Respondents argued that if the claim phrase "semiconductor element regions" is read to be operable, then said phrase should mean "active regions defined on each of their sides by a field oxidation film and on their top by a non-conductive film"; that both experts agree that the claimed "semiconductor element regions" must be read to include (1) non-conductive film on top of the semiconductor substrate and (2) some isolation region; that it is the latter requirement that is disputed; that because a "field oxidation film" is the only isolation structure disclosed in the patent, the claim must be read as limited to that structure; and that both experts acknowledge that the '178 patent discloses nothing but the use of field oxidation isolation structures for creating semiconductor element regions. (RBr at 98-99.) Respondents further argued that while complainant contends that STI was disclosed because Mori submitted a supplemental IDS, which disclosed three references, one of which disclosed a form of trench isolation, that complainant does not provide any case law supporting its argument that this is sufficient disclosure that must be used to define the alleged invention in the wake of Phillips and its progeny. (RRBr at 70.)

At the outset, it is undisputed that a semiconductor device would not properly operate without a non-conductive film separating the first gate electrode from the active area of the substrate. (TFF 1021 (undisputed).) The private parties agreed that the claimed "semiconductor element regions," to be operable, must be read to include a non-conductive film on top of the semiconductor substrate. (RBr at 99; CRBr at 61.) The private parties also agreed that an "isolation structure" is required. (CRBr at 62; RRBr at 99.) Hence, the administrative law judge finds that the active regions must have a non-conductive film on top and some type of an isolation structure.

The disagreement between the parties is whether the isolation structure must be limited to a "field oxidation film." Claim 5 in issue reads in part:

> A semiconductor memory device, comprising:
>
> a semiconductor substrate having semiconductor element regions;
>
> first gate electrodes formed on said semiconductor element regions;

(JX-1 at 5:21-25 (emphasis added).) The plain language of the first clause of claim 5 shows that a semiconductor substrate includes "semiconductor element regions." Also, the plain language of the second clause requires that first gate electrodes are formed on "said semiconductor element regions." In addition, as indicated, supra, the private parties agreed that some type of an "isolation structure" is required. Also, the administrative law judge, with reference to "field oxidation film" recited in claim 1, supra, found that the specification of the '178 patent is limited to a thermal oxidation process such as LOCOS for forming the "field oxidation film."

The administrative law judge rejects complainant's argument that a disclosure of the

Sugatani reference in the supplemental IDS is support for including isolation structures which are formed by some type of a trench isolation process in claim 5. The patent application which issued as the '178 patent, was filed on April 24, 1991. (JX-1 at 1.) Also, the '178 patent shows a foreign application priority date of April 24, 1990. (Id.) On January 16, 1992, some nine months after the application filing date of the '178 patent, the patentee filed a supplemental IDS. (TFF 1032 (undisputed).)[30] However, as Phillips makes clear, it is the specification filed on April 24, 1991 that a person of ordinary skill in the art looks to for claim interpretation, not a document filed some nine months later.

Complainant asserted that based on the doctrine of claim differentiation, "semiconductor element regions" should not be defined to include a "field oxidation film" since non-asserted dependent claim 7 does include the term "field oxidation film". While said claim 7 does recite the term "field oxidation film," said claim 7, which depends from independent claim 5 in issue, imposes additional imitations not included in claim 5, e.g., the limitation "said first gate electrodes extending onto said field oxidation film." Hence, the administrative law judge rejects complainant's assertion with respect to claim 7.

Based on the foregoing, the administrative law judge interprets the claimed phrase "semiconductor element regions" to mean active regions separated by isolation regions and topped by a non-conductive film, where said isolation regions include 'field oxidation film" but said isolation regions are not formed by a trench isolation process such as STI.

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[30] The patentee submitted said IDS only because of a continuing duty of disclosure and because a search report issued on November 11, 1991 in the European application corresponding to the '178 patent application, which date is after the mailing date of the Office Action of August 7, 1991. (JX-2 at TC-ITC-B 000207.)

b. "first gate electrodes"

The claimed phrase "first gate electrodes" appears in the second clause of independent claim 5 of the '178 patent, which reads: "first gate electrodes formed on said semiconductor element regions." (JX-1 at 5:24-25 (emphasis added).)

Complainant argued that the claimed phrase "first gate electrodes" should be construed to mean "floating gate electrodes." (CRBr at 65.)

The administrative law judge has found that the claimed phrase "first gate electrodes formed on said element forming regions" of claim 1 in issue to mean "floating gate electrodes formed on said element forming regions." See supra. Hence, the administrative law judge interprets the claimed phrase "first gate electrodes" of claim 5 in issue to mean "floating gate electrodes."

c. "an insulating film formed on said first gate electrodes and defining grooves"

The claimed phrase "an insulating film formed on said first gate electrodes and defining grooves" appears in the third clause of independent claim 5 of the '178 patent, which reads: "an insulating film formed on said first gate electrodes and defining grooves having a substantially same width between said first gate electrodes." (JX-1 at 5:26-28 (emphasis added).)

Complainant argued that the claimed phrase "insulating film" means a "film that provides electrical isolation between electrically conductive materials." (CRBr at 67-69.)

Respondents argued that the claimed phrase "an insulating film formed on said first gate electrodes and defining grooves" means "a non-conductive film that is both formed on the conductive layer of the first gate electrodes and defines grooves between adjacent first gate electrodes." (RBr at 101-102.)

The administrative law judge has construed the claimed phrase "an insulating film formed to define grooves" of claim 1 to mean "a non-conductive film that defines grooves between adjacent first gate electrodes where said film may be multi-layered." Thus, the administrative law judge found that an "insulating film" as recited in claim 1 may be multi-layered. See supra. Based on the findings as to claim 1, he finds that the "insulating film" of claim 5 may be multi-layered.

A difference between the claimed phrase "an insulating film formed to define grooves" of claim 1 and the claimed phrase "an insulating film formed on said first gate electrodes and defining grooves" of claim 5 is that claim 5 includes further limiting language "formed on said first gate electrodes." However, the administrative law judge finds that the plain language of the claimed phrase "an insulating film formed on said first gate electrodes and defining grooves" of claim 5 shows that an "insulating film" must be formed on the first gate electrodes and said "insulating film" must also define grooves.

Based on the foregoing, the administrative law judge interprets the claimed phrase "an insulating film formed on said first gate electrodes and defining grooves" to mean "a non-conductive film is formed on the first gate electrodes and said film defines grooves between said first gate electrodes where said film may be multi-layered."

d. "grooves having a substantially same width between said first gate electrodes"

In issue is the claimed phrase "grooves having a substantially same width between said first gate electrodes," which appears in the third clause of independent claim 5 of the '178 patent and reads: "an insulating film formed on said first gate electrodes and defining grooves having a substantially same width between said first gate electrodes." (JX-1 at 5:26-28 (emphasis added).)

Complainant argued that the claimed phrase "grooves having a substantially same width between said first gate electrodes" means "the width of each groove is approximately the same between adjacent gates within a level of tolerance that the particular process technology is able to deliver" (CBr at 144-45), which is the same construction as complainant's proposed construction for the claimed phrase "grooves having substantially the same width between said first gate electrodes" of claim 1.

Respondents argued that the claimed phrases "grooves having a substantially same width between said first gate electrodes" of claim 5 and "grooves having substantially the same width between said first gate electrodes" of claim 1 "should be construed in the same way for both claim 1 and claim 5 " because "the language is the same in all material respects." (RBr at 102.)

The staff argued that the claimed phrase "substantially the same width" means "substantially the same separation between gate electrodes." (SBr at 15.)

Hence, the administrative law judge finds that all parties agreed that said claimed phrases "grooves having a substantially same width between said first gate electrodes" of claim 5 and "grooves having substantially the same width between said first gate electrodes" of claim 1, should be construed in the same way for both claim 1 and claim 5.

The plain language of the claimed phrase "grooves having a substantially same width between said first gate electrodes" in issue, shows that the grooves between said first gate electrodes have substantially the same separation between said first gate electrodes.

Based on the foregoing, in view of how the administrative law judge interpreted the claimed phrase "grooves having substantially the same width between said first gate electrodes" of claim 1, he interprets the claimed phrase "grooves having a substantially same width between

said first gate electrodes" of claim 5 to mean that grooves between said first gate electrodes have substantially the same separation that is not limited to a single width or a rectangular separation, and said "grooves" must be "between" said first gate electrodes, i.e., floating gate electrodes, in the sense that said grooves are in the spaces that separate said floating gate electrodes, where said grooves are substantially on the same plane as said floating gate electrodes.

e. "a second gate electrode formed on said insulating film"

In issue is the claimed phrase "a second gate electrode formed on said insulating film," which appears in the fourth clause of independent claim 5 of the '178 patent and reads:

> a second gate electrode formed on said insulating film, said second gate electrode comprising (1) a polysilicon layer formed on said insulating film and filling in said grooves and (2) one of [either] a high melting point metal layer and a silicide layer of a high melting point [metal] on said polysilicon layer, a surface portion of said polysilicon layer at positions corresponding to said grooves being substantially planar.

(JX-1 at 5:29-38 (emphasis added).)

Complainant argued that the claimed phrase "a second gate electrode formed on said insulating film" means "a control gate electrode formed on said insulating film." (CRBr at 71-72.)

Respondents argued that the claimed phrase "a second gate electrode formed on said insulating film" means "the polysilicon layer of the second gate electrode is formed directly on the insulating film." (RBr at 102.)

The plain language of the fourth clause of claim 5 shows that a second gate electrode is formed on said insulating film, where said second gate electrode includes (1) a polysilicon layer and (2) either a metal layer or a silicide layer. The plain language of said fourth clause also

requires that said "polysilicon layer" is formed on said insulating film and that either a "metal layer" or a "silicide layer" be on said polysilicon layer.

The specification of the '178 patent equates the claimed phrase "second stage gate electrode" with "control gate electrode." For example, the ABSTRACT of the specification states:

> In a semiconductor memory device of multistage gate structure, the second stage gate electrode (control gate electrode) is of superposed-layer structure of a second polysilicon layer and a high melting point layer or a silicide layer of a high melting point metal layer formed thereon.

(JX-1 at Abstract (emphasis added).) Also, the "Field of the Invention" section of the specification states:

> The present invention relates to a semiconductor memory device and a method of manufacturing the same and, more particularly, to a semiconductor memory device having gate electrode layers of multistage structure such as an EPROM (electrically programmable read only memory) or EEPROM (electrically erasable and programmable read only memory) in which the control gate electrode is of superposed-layer structure of a polysilicon layer and a refractory metal layer (a high melting point metal layer) or a silicide layer thereof.

(JX-1 at 1:6-17 (emphasis added).) Further, the specification states:

> Thereafter, as shown in FIG. 2B, a first oxide film 206 is formed over the semiconductor structure by a known method such as a thermal oxidation method to isolate the gate electrodes 20 of the first level layer from a gate electrode (control gate electrode) of a second level layer formed at a later step.

(JX-1 at 3:39-44 (emphasis added).) Hence, the administrative law judge finds that one of ordinary skill in the art would understand that a "second gate electrode" is a "control gate

electrode."[31] Further, the specification's disclosure regarding the "superposed-layer structure of a second polysilicon layer and a high melting point layer or a silicide layer of a high melting point metal layer" is consistent with the plain language of the fourth clause of claim 5 which requires that a second gate electrode include (1) a polysilicon layer and (2) either a metal layer or a silicide layer.

The administrative law judge rejects respondents' assertion that the claimed phrase in issue means "the polysilicon layer of the second gate electrode is formed directly on the insulating film." As indicated, supra, the plain language of the fourth clause of claim 5 in issue and the specification of the '178 patent make clear that "a second gate electrode," not merely "the polysilicon layer of the second gate electrode," is formed on said insulating film, where said "second gate electrode" includes (1) a polysilicon layer and (2) either a metal layer or a silicide layer. Moreover, said fourth clause recites "a second gate electrode formed on said insulating film, said second gate electrode comprising (1) a polysilicon layer formed on said insulating film." As seen from the plain language of said fourth clause, respondents' proposed construction, i.e., "the polysilicon layer of the second gate electrode is formed directly on the insulating film," is essentially the same as the language subsequent to the claimed phrase in issue, i.e., "a polysilicon layer formed on said insulating film."

Based on the foregoing, the administrative law judge interprets the claimed phrase "a second gate electrode formed on said insulating film" to mean "a control gate electrode formed on said insulating film."

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[31] The administrative law judge finds that a person of ordinary skill would understand that a "second stage gate electrode" or a "gate electrode [ ] of a second level layer" means a "second gate electrode."

f. "substantially planar"

In issue is the claimed phrase "substantially planar," which appears in the fourth clause of independent claim 5 of the '178 patent and reads:

> a second gate electrode formed on said insulating film, said second gate electrode comprising (1) a polysilicon layer formed on said insulating film and filling in said grooves and (2) one of [either] a high melting point metal layer and a silicide layer of a high melting point [metal] on said polysilicon layer, a surface portion of said polysilicon layer at positions corresponding to said grooves being substantially planar.

(JX-1 at 5:29-38 (emphasis added).)

All of the parties agreed that one of ordinary skill in the art would understand the claimed phrase "substantially planar" of claim 5 to mean the same thing as the claimed phrase "substantially flat" of claim 1. (TFF 1049 (undisputed).) The administrative law judge has already found that "substantially flat," as it appears in the claimed phrase "surfaces of those portions of said polysilicon layer which are above said grooves being substantially flat" of claim 1 as a surface which substantially eliminates the topographical features of the underlying structure and thus does not require perfect flatness or anatomic flatness and that the substantial flatness should be determined after the polysilicon layer is deposited but before any subsequent processing. See supra.

Hence, the administrative law judge (1) interprets "substantially planar" as he has interpreted "substantially flat" of claim 1 and (2) finds that the substantial planarity should be determined after the polysilicon layer is deposited but before any subsequent processing.

VIII. Infringement

Under the provisions of 35 U.S.C. § 271, liability for infringement arises if "whoever

without authority makes, uses, offers to sell, or sells any patented invention, within the United States or imports into the United States any patented invention during the term of the patent therefor." 35 U.S.C. § 271(a). This infringement of a patented invention is the usual meaning of the expression "direct infringement." See Joy Techs., Inc. v. Flakt, Inc., 6 F.3d 770, 773 (Fed. Cir. 1993).

A determination of infringement requires a two-step analysis. First, the patent claim must be properly construed to determine its scope and meaning. Second, the claim as properly construed must be compared to the accused device or process. Zelinski v. Brunswick Corp., 185 F.3d 1311, 1315 (Fed. Cir. 1999), citing Markman v. Westview Instruments, Inc., 52 F.3d 967, 976 (Fed. Cir. 1995). Whereas claim construction is a matter of law and therefore, the exclusive province of the court, "whether a claim encompasses an accused device, either literally or under the doctrine of equivalents, is a question of fact." Zelinski, 185 F.3d at 1315, citing N. Am. Vaccine, Inc. v. Am. Cyanamid Co., 7 F.3d 1571, 1574 (Fed. Cir. 1993).

To prove literal infringement, the patentee must show, by a preponderance of the evidence, that the accused device contains every limitation in the asserted claims. WMS Gaming Inc. v. Int'l Game Tech., 184 F.3d 1339, 1350 (Fed. Cir. 1999), citing Mas-Hamilton Group v. LaGard, Inc., 156 F.3d 1206, 1211 (Fed. Cir. 1998).

To establish literal infringement of a claim written in means-plus-function format, the patentee must prove that the relevant structure in the accused device performs the identical function set forth in the claim. Odetics, Inc. v. Storage Tech. Corp., 185 F.3d 1259, 1267 (Fed. Cir. 1999). Means-plus-function claiming applies only to purely functional limitations that do not provide the recited structure. See Watts v. XL Systems, Inc., 232 F.3d 877, 880-81 (Fed. Cir.

2000). Once a "functional identity" has been established, the patentee must then prove that the relevant structure in the accused device is either identical or equivalent to the corresponding structure disclosed in the patent specification. Id. Thus, "[f]unctional identity and either structural identity or equivalence are both necessary" for a finding of literal infringement. Id. (emphasis in original); see Frank's Casing Crew & Rental Tools v. Weatherford Int'l, Inc., 389 F.3d 1370, 1378 (Fed. Cir. 2004) (affirming summary judgement of non-infringement where identity of function satisfied yet accused device and disclosed corresponding structure "represent two distinct structural approaches") (citation omitted).

As for determining structural equivalence under 35 U.S.C. § 112, ¶ 6:

> the statutory equivalence analysis requires a determination of whether the 'way' the assertedly substitute structure performs the claimed function, and the 'result' of that performance, is substantially different from the 'way' the claimed function is performed by the 'corresponding structure . . . described in the specification,' or its 'result.' Structural equivalence under § 112, ¶ 6 is met only if the differences are insubstantial . . .; that is, if the assertedly equivalent structure performs the claimed function in substantially the same way to achieve substantially the same result as the corresponding structure described in the specification.

Odetics, Inc., 185 F.3d at 1267 (citations omitted) (emphasis added); see Chiuminatta Concrete Concepts, Inc. v. Cardinal Indus., Inc., 145 F.3d 1303, 1309-10 (Fed. Cir. 1998) (reversing summary judgement of infringement where accused device and disclosed structure were substantially different). The Federal Circuit has cautioned, however, that "[t]he individual components, if any, of an overall structure that corresponds to the claimed function are not claim limitations." Odetics, Inc., 185 F.3d at 1268. "Rather, the claim limitation is the overall structure corresponding to the claimed function. This is why structures with different numbers of parts

may still be equivalent under § 112, ¶ 6 thereby meeting the claim limitation." Id.; see Caterpillar Inc. v. Deere & Company, 224 F.3d 1374, 1380 (Fed. Cir. 2000) (vacating district court's summary judgement of non-infringement based on an "impermissible component-by-component analysis" for structural equivalence).

A device that does not literally infringe a patent claim may nonetheless infringe under the doctrine of equivalents. The infringement analysis under the doctrine of equivalents requires a determination of whether the differences between the recited claim element and the accused device are insubstantial, i.e. if the accused device performs substantially the same function in substantially the same way to achieve substantially the same result as that required by the particular claim element.[32] Graver Tank & Mfg. Co., Inc. v. Linde Air Prods., 339 U.S. 605, 609 (1950); see Kemco Sales, Inc. v. Control Papers Co., 208 F.3d 1352, 1365 (Fed. Cir. 2000) (discussing applicability of doctrine of equivalents to means-plus-function claims). To prove infringement under the doctrine of equivalents, a patentee must prove equivalency on a limitation-by-limitation basis, which requires "particularized testimony and linking argument." Texas Instr. Inc. v. Cypress Semiconductor Corp., 90 F.3d 1558, 1566 (Fed. Cir. 1996). Thus, Federal Circuit precedent requires that:

> a patentee must . . . provide particularized testimony and linking argument as to the 'insubstantiality of the differences' between the claimed invention and the accused device or process, or with respect to the function, way, result test when such evidence is presented to support a finding of infringement under the doctrine of

[32] In addition, other "objective evidence" may be relevant to determining whether the differences between the accused device and the claimed invention are insubstantial, which "may include evidence of known interchangeability to one of ordinary skill in the art, copying, and designing around." Texas Instr. Inc. v. Cypress Semiconductor Corp., 90 F.3d 1558, 1566 (Fed. Cir. 1996).

equivalents.

Id. As for a doctrine of equivalents infringement analysis of a claim written in means-plus-function format, as set forth in Kemco Sales, 208 F.3d at 1364:

> If an accused structure is not a section 112, paragraph 6 equivalent of the disclosed structure because it does not perform the identical function of that disclosed structure and hence does not literally infringe, it may nevertheless still be an "equivalent" under the doctrine of equivalents. Thus, if one applies the traditional function-way-result test, the accused structure must perform substantially the same function, in substantially the same way, to achieve substantially the same result, as the disclosed structure.FN6 See Dawn Equipment Co. v. Kentucky Farms Inc., 140 F.3d 1009, 1016, 46 USPQ2d 1109, 1113 (Fed.Cir.1998). A key feature that distinguishes "equivalents" under section 112, paragraph 6 and "equivalents" under the doctrine of equivalents is that section 112, paragraph 6 equivalents must perform the identical function of the disclosed structure, see Odetics, 185 F.3d at 1267, 51 USPQ2d at 1229; Pennwalt, 833 F.2d at 934, 4 USPQ2d at 1739, while equivalents under the doctrine of equivalents need only perform a substantially similar function, see Al-Site Corp. v. VSI Int'l, Inc., 174 F.3d 1308, 1320-21, 50 USPQ2d 1161, 1168 (Fed.Cir.1999).
>
> * * *
>
> Because the "way" and "result" prongs are the same under both the section 112, paragraph 6 and doctrine of equivalents tests, a structure failing the section 112, paragraph 6 test under either or both prongs must fail the doctrine of equivalents test for the same reason(s). That was the case in Chiuminatta, in which the "way" was determined to be substantially different under a section 112, paragraph 6 analysis. See Chiuminatta, 145 F.3d at 1309, 46 USPQ2d at 1757. Accordingly, we concluded that the accused structure did not infringe under the doctrine of equivalents for precisely the same reason. See id. at 1311, 145 F.3d 1303, 46 USPQ2d at 1758.

(footnote omitted)

A. The '969 Patent

Complainant asserted that claims 1, 6 and 7 of the '969 patent are infringed by

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}

The administrative law judge has found that complainant has established, by a preponderance of the evidence, that the accused chips are "nonvolatile semiconductor memory devices" that have:

> a memory cell array comprising memory cells arranged in matrix form having rows and columns and row lines and column lines, each memory cell including cell transistors connected in series, and each of the cell transistors having a control gate, a floating gate, a channel region and an insulation film between the floating gate and the channel region, for electrically storing data by using charges stored in the floating gate, each memory cell having a first terminal and a second terminal, the first terminals of the memory cells in the same column being commonly connected to one of the column lines, the second terminals of the memory cells being connected to

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[33] The sizes specified are in nanometers (nm), referring to feature sizes within the integrated circuits.

[34] The staff's finding of fact actually identifies respondents as the party asserting that the claims are infringed. (SPFF 12 ("Hynix contends that ... claims 1, 6, and 7 of the '969 patent are infringed").) The staff's finding of fact is not disputed by complainant. Respondents objected to the staff's finding of fact as inaccurate, stating that it was complainant, not respondents, who asserted that the claims are infringed. (RRSPFF 12 ("Toshiba, not Hynix contends that the claims ... are infringed.").) However, Respondents do not dispute that complainant asserted that said claims are infringed. (RRSPFF 12.)

[35] The abbreviations "Mb" and "Gb" refer to megabits and gigabits, indicating the memory storage capacity of the devices.

[36] Neither party disputed that these NAND flash memory devices included the listed flash products.

> a reference potential, and the control gates of the cell transistors in the same row being commonly connected to one of the row lines, [memory cell array limitation][37]

"data latching means for storing data, connected to each of the column lines," and "column selection means for designating one of the columns of the memory cells in response to a column selection signal."

However, he finds that complainant has not met its burden in establishing that the accused chips have the claimed phrase:

> data programming means for selectively programming the cell transistors, wherein a selected cell transistor is programmed in accordance with data corresponding to the stored data of the data latching means, the cell transistor holds an injected state of electrons which are injected through the insulation film into the floating gate by utilizing a tunnel effect by the data programming means when the stored data of the data latching means is a first logic level, and the cell transistor holds an emitted state of electrons which are emitted through the insulation film from the floating gate by utilizing a tunnel effect by the data programming means when the stored data of the data latching means is a second logic level.

He also finds that complainant has not met its burden in establishing that the accused chips have the claimed phrase "row selection means for designating one of the rows of the memory cells in

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[37] Respondents argued that complainant adopted a new interpretation for the claim term "channel region" in the memory cell array limitation under which respondents' accused products do not infringe the asserted claims. (RBr at 137.) Respondents argued that complainant interpreted "channel region" to include the tunnel insulation film, so that there is nothing between the channel region and the floating gate. (RBr at 139.) Respondents also argued that complainant stated that there is nothing between the identified "channel region" and the floating gate in respondents' accused products, with the insulation film having become part of the "channel region." (RBr at 139.) Thus, the respondents argued that respondents' accused products do not infringe because the '969 patent requires that there be an insulation film between the floating gate and the channel region. (RBr at 139; RPFF 2648.) The administrative law judge finds that respondents' representative accused products do have the memory cell array limitation.

response to a row selection signal." Hence, he finds that complainant has not established, by a preponderance of the evidence, that the asserted claims of the '969 patent are infringed.

1. Claim 1

a. "data programming means for selectively programming the cell transistors, wherein a selected cell transistor is programmed in accordance with data corresponding to the stored data of the data latching means, the cell transistor holds an injected state of electrons which are injected through the insulation film into the floating gate by utilizing a tunnel effect by the data programming means when the stored data of the data latching means is a first logic level, and the cell transistor holds an emitted state of electrons which are emitted through the insulation film from the floating gate by utilizing a tunnel effect by the data programming means when the stored data of the data latching means is a second logic level"

Complainant argued that based on its claim interpretation,{

} It is argued that the identified transistor is the same as or equivalent to the corresponding structure disclosed in the specification, specifically, the transistor 81 in Figure 18A of the '969 patent. (CBr at 58; TFF 542-545, 552, 553, 561.) {

}

Respondents, as to all of respondents' representative products, argued that there is no infringement if the administrative law judge adopts respondents' proposed claim interpretation that circuit 10 in Figure 1 or its alternative embodiments in Figures 7-9 of the '969 patent and not transistor 81 of Figure 18A of the '969 patent are the proper disclosed structures corresponding to the claimed function of the "data programming means." (RBr at 105.) It is argued that their

accused products do not contain any structure identical or equivalent to either circuit 10 or the circuits shown in Figures 7-9. (RBr at 105; RPFF 2001.) It is also argued that even if "[complainant] could read the term 'programming' to somehow make the recited function align with the accused product," respondents' accused products do not perform the function in substantially the same way to achieve substantially the same result because respondents' accused products program differently in at least four respects: {

}

Respondents further argued that complainant failed to provide any proof that respondents' MLC products infringe. (RBr at 128.) Respondent argued that complainant's expert Reed, did not consider the MLC cells for his analysis (RBr at 128-129; RPFF 2071); and that Reed treated the MLC product as if they were identical to the other SLC products and thus never provided a separate infringement analysis for the MLC product. (RBr at 129; RPFF 2072.) It is argued that respondents' MLC products operate and program very differently from the SLC products and that {

}

The staff argued that respondents' {

} It is argued that in respondents' accused products, {

} infringement because all of the claim limitations are still performed,{ } (SBr at 40.) The staff argued that the only difference from the '969 patent { } The staff further argued, however, that claim 1 is silent on whether or not the injection or emission should occur in one or multiple pulse. (SBr at 40.) The staff argued that the presence of additional structure in an accused device will not exclude a finding of infringement and therefore,{ }

As found supra, the entire circuit of Figure 18A of the '969 patent, not merely transistor 81 of Figure 18A, is the corresponding structure for the recited function of the "data programming means" limitation of claim 1 of the '969 patent. However, complainant solely relied on transistor 81 as the corresponding structure for the recited function of the "data programming means" limitation of claim 1 of the '969 patent. (RPFF 2006 (undisputed).) Complainant's sole reliance on transistor 81 as the corresponding structure for the recited function of said "data programming means" is conclusively established by complainant's expert Reed, testimony that he only relied on transistor 81 of Figure 18A of the '969 patent for his infringement opinion with respect to the "data programming means" limitation:

Q. You're not relying on corresponding structure 1 in

your infringement or domestic industry analysis, correct?

A. Corresponding structure 1. Oh, circuit 10 of figure 1. No, I'm not.

Q. You're not relying on corresponding structure 2, the circuit of figure 7 in your infringement or domestic industry analysis, correct?

A. No, sir, I'm not.

Q. You're not relying on circuit figure 8, item 3, correct?

A. That's right.

Q. You're not relying on the structure of circuit figure 9, number 4 here, correct?

A. That's right.

Q. So the only structure with which you have asserted infringement or coverage of the domestic industry products for the data programming means is transistor 81 of figure 18A, correct?

A That's the evidence here, sir.

* * *

BY MR. CORDELL:

Q. So we're crystal clear about that, right, Mr. Reed, it's only transistor 81 of figure 18A that you have used as your corresponding structure for all of your infringement and domestic industry analysis, correct?

A. That's correct.

(Reed, Tr. at 1317:18 - 1318:15, 1318:21 - 1319:1 (emphasis added).) Thus, the administrative

law judge finds that complainant's entire argument with respect to whether respondents' accused products contain identical structure to the corresponding structure of the "data programming means" of claim 1 of the '969 patent, relates only to whether respondents' products contain structure identical to transistor 81 of Figure 18A of the '969 patent. (See CBr at 58-60; TFF 542-545, 552-556, and 558-560.) He further finds that none of the evidence relied on by complainant establishes, by a preponderance of the evidence, that any of respondents' products contain structure identical to the entire circuit of Figure 18A of the '969 patent. (See id.)

Based on the foregoing, the administrative law judge finds that complainant has not established, by a preponderance of the evidence, that the accused products literally meet all the limitations of the claimed phrase in issue.

Regarding any alleged infringement under the doctrine of equivalents, as found supra, the entire circuit of Figure 18A of the '969 patent, not merely transistor 81 of Figure 18A, is the corresponding structure for the recited function of the "data programming means" limitation of claim 1 of the '969 patent. However, complainant relied solely on transistor 81 as the corresponding structure for the recited function of the "data programming means" limitation of claim 1 of the '969 patent. (RPFF 2006 (undisputed).) Thus, the administrative law judge finds that complainant failed to establish, by preponderance of the evidence, that any of respondents' products contain structure that was equivalent to the entire circuit of Figure 18A or any other structure besides transistor 81 of Figure 18A disclosed in the specification of the '969 patent. (See CBr at 58-60; TFF 542-545, 552-556, and 558-560.)

Based on the foregoing, the administrative law judge finds that complainant has not established, by a preponderance of the evidence, that the accused products meet all of the

limitations of the claimed phrase in issue under the doctrine of equivalents.

b. "row selection means for designating one of the rows of the memory cells in response to a row selection signal"

Complainant argued that each of respondents' NAND flash devices includes{

} It is argued that respondents' row selection circuitry is the same as or equivalent to the corresponding structure disclosed in the specification, specifically row decoder 53, particularly as it is employed in Figure 17 of the '969 patent. (CBr at 54; TFF 492.) Complainant also argued that in respondents' representative parts, {

} Respondents argued that neither performs the same function and both are substantially different structurally and operationally. (RBr at 135; RPFF 2617.) Respondents argued that if complainant relies on some combination of Figures 10 and 17, or 10, 17 and 18, there is no infringement because Figure 17 requires the use of column decoder 55 and triple-index W signals generated from the combination of Z signals (produced by column decoder 55) and double–indexed W signals (produced by row decoder 53), yet, respondents' accused products{

} Respondents also argued that even if complainant argued that row decorder 53 alone is the corresponding structure, respondents do not infringe because{

}

The staff argued that respondents' accused devices have{

} (SBr at 41.) Therefore, the staff argued, respondents' accused products satisfy the "row selection means" limitation. (SBr at 41.)

The issue is whether the accused{

} (SBr at 41.)

The administrative law judge finds that the structure that comprises{

} He so finds because the

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[38] The administrative law judge finds that respondents' accused representative products {

} (RPFF 2626 (undisputed).) The administrative law judge also finds that

{ } perform the recited function of "row selection means" in a substantially different way since in the embodiment that comprises solely of the circuit of Figure 10, row decoder 53 generates and applies a signal to one of the first row lines, and said signal passes through the entire first row line and into every cell transistor connected to the first row line, and also applies a signal to one of the second row lines, and said signal passes through the entire second row line and into every selection transistor connected to the second row line, and no additional signal is needed to perform the recited function of the "row selection means." (JX-4 at 9:1-10.) However, in respondents' accused representative products, the administrative law judge finds that{

} (Reed, Tr. at 1114:5-18, 1115:22-1117:12, 1118:4-1119:2, 1121:1-17, 1122:15-1123:18; Subramanian, Tr. at 1879:23 - 1880:19.) Rather, the administrative law judge finds that in respondent's accused representative products,{

} (Id.)

The administrative law judge also finds that the{

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respondents' accused representative products{

} Thus, the administrative law judge finds that the{ }structure of the respondents' accused representative products is more analogous to the embodiment of the '969 patent that combines the circuits of Figures 10 and 17, compared to the embodiment of the '969 patent that consists solely of the circuit of Figure 10, because respondents' accused representative products {

}(JX-4 at 11:58-12:8.) However, as found infra, the administrative law judge finds that the accused representative products do not infringe the "row selection means" limitation under either embodiment.

} "row selection means" in a substantially different way in an embodiment that combines the circuits of Figures 10 and 17 because said embodiment requires a triple-indexed W signal which comprises a double-indexed W signal generated by row decoder 53 and a single-indexed Z signal generated by column decoder 55[39] applied to a row line, whereas in the respondents' representative products,{

} (JX-4 at 11:58-12:8; Reed, Tr. at 1114:5-18, 1115:22-1117:12, 1118:4-1119:2, 1121:1-17, 1122:15-1123:18; Subramanian, Tr. at 1879:23 - 1880:19.) The administrative law judge finds that the{

} He further finds that complainant has failed to show any combination at all of the signals generated by the{

} disclosing the corresponding structure of the "row selection means" of the '969 patent. While the individual components of the structure disclosed in Figures 10 and 17 of the '969 patent are not claim limitations, said

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[39] Complainant failed to assert that row decoder 55 was required to perform the recited function of the "row selection means" for the '969 patent in an embodiment that used the QT transistors of Figure 17 of the '969 patent, instead asserting that row decoder 53 combined with the circuitry of Figure 17 of the '969 patent was the corresponding structure of the "row selection means". (CBr at 47.) As found supra, the administrative law judge found row decoder 53 of Figure 10 of the '969 patent to be the corresponding structure for the "row selection means" of claim 1 of the '969 patent. However, in an embodiment that combines Figure 10 and Figure 17 of the '969 patent, and thus, uses the QT transistors of Figure 17 of the '969 patent, the administrative law judge has already found in the claim interpretation section that row decoder 53 and column decoder 55 are required to perform the function of the "row selection means" because the embodiment that comprises Figure 10 and Figure 17 of the '969 patent is an optional embodiment of claim 1 of the '969 patent, and because both embodiments use row decoder 53, the administrative law judge only found row decoder 53 to be to the corresponding structure of the "row selection means" of claim 1 of the '969 patent.

components comprise the way that said structure performs the recited function of the "row selection means." The specification of the '969 patent specifically states that the signal that is applied to a row line is a triple-indexed W signal generated by combining the signals generated by row decoder 53 and column decoder 55. (See JX-4 at 11:65-12:2.) The administrative law judge finds that the{

} For the foregoing reasons, the administrative law judge finds that the WL Decoder and X-Decoders of respondents' representative accused products perform the recited function of the "row selection means" in a substantially different way.

Based on the foregoing, the administrative law judge finds that complainant has not established, by a preponderance of the evidence, that the accused products literally meet all the limitations of the claimed phrase "row selection means for designating one of the rows of the memory cells in response to a row selection signal."

As for any alleged infringement under the doctrine of equivalents, as found supra, the {

} in a substantially different way than row decoder 53 of Figure 10 of the '969 patent, either in the embodiment that uses solely the circuit in Figure 10, or the embodiment that combines the circuit in Figure 10 with the circuit in Figure 17, for the previously stated reasons.

Based on the foregoing, the administrative law judge finds that complainant has not established, by a preponderance of the evidence, that the accused products meet all of the limitations of the claimed phrase "row selection means for designating one of the rows of the

memory cells in response to a row selection signal," under the doctrine of equivalents.

Complainant argued that its expert Reed in his testimony established that, in each of respondents' representative accused products,{

} (CBr at 54-55; TFF 496-499, 501-502.) However, complainant failed to demonstrate how this process is substantially the same as the process disclosed in the specification of the '969 patent that requires the combined signals of row decoder 53 and column decoder 55 to both{

}

Complainant also argued that respondents' principal challenge to infringement is that the { } as does the row decoder 53 as depicted in Figure 10 of the '969 patent, and that this challenge should fail because the specific features of the embodiment of row decoder 53 shown for purposes of illustration in the specification should not be incorporated into the claims. (CRBr at 51.) However, the "row selection means" limitation is a means-plus-function limitation. The

disclosure of row decoder 53 in the various embodiments of the '969 patent (specifically the embodiment that comprises the circuit of Figure 10, and the embodiment that comprises of the combined circuitry of Figure 10 and Figure 17) is the disclosure that identifies the corresponding structure of the means-plus-function limitation. Thus, complainant has not shown, by a preponderance of the evidence, that the accused structure is either identical or equivalent to the structure disclosed in the specification of the '969 patent. As found supra, the structure disclosed in the specification of the '969 patent and the structure in respondents' accused products perform the recited function in substantially different ways.

2. Dependent Claims 6 And 7

Complainant argued that each of respondents' representative NAND flash devices include

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(CBr at 61; TFF 471, 562, 563, 565-571.) It is argued that the identified transistors,{

} are the same or equivalent to corresponding structure disclosed in the specification, specifically the "ST" transistors in Figure 1 of the '969 patent's specification. (CBr at 61; TFF 471, 563, 565-571.) Complainant argued that, consequently, the representative devices infringe claim 6 of the '969 patent. (CBr at 61.)

Complainant also argued that each of respondents' representative NAND flash devices

{

} (CBr at 61-62; TFF 473-475, 573-577.) It is argued that the identified transistors are the same or equivalent to the corresponding structure disclosed in the specification, specifically, the transistor 80 in Figure 16 of the '969 patent's specification. (CBr

at 62; TFF 573-575.) Complainant argued that the{

} (CBr at 62; TFF 578-580.) Thus, complainant argued that the{ } perform the recited function using the corresponding structure and therefore meet the element of claim 7. (CBr at 62.) Hence, complainant argued that respondents' representative devices infringe claim 7. (CBr at 62.)

Respondents argued that because claims 6 and 7 are dependent on claim 1, which respondents argued is not infringed, respondents' products do not infringe claims 6 and 7. (RBr at 139; RPFF 2651-2652.)

The staff argued that claims 6 and 7 are dependent on claim 1 and there are no disputed limitations in claims 6 and 7 that are included in claim 1. (SBr at 41.) Thus, staff argued, claims 6 and 7 are infringed for the same reasons that claim 1 is infringed. (SBr at 41.)

Claim 6 depends on claim 1[40] and recites a further limitation "selection transistors respectively inserted between the first terminals of the memory cells and the column lines, gates of the selection transistors being connected to one of the row lines." (JX-4 at 25:26-32.) Claim 7 depends on claim 1[41], and recites a further limitation "switching means respectively inserted

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[40] The language of claim 6 of the '969 patent reads: "A nonvolatile semiconductor memory device according to any one of claims 1 to 5..." (JX-4 at 26-27.) However, claim 6 is asserted by complainant only to the extent of its dependence on claim 1 of the '969 patent. (CBr at 60.)

[41] The language of claim 7 of the '969 patent reads: "A nonvolatile semiconductor memory device according to any one of claims 1 to 5..." (JX-4 at 33-34.) However, claim 7 is asserted by complainant only to the extent of its dependence on claim 1 of the '969 patent. (CBr at 61.)

between the second terminals of the memory cells and the reference potential, and controlled so as to be in an off state when the data programming means stores data." (JX-4 at 25:33-38.)

As seen, supra, the administrative law judge found that complainant has not established, by a preponderance of the evidence, that the accused products meet all of the limitations of independent claim 1. Hence, the administrative law judge finds that complainant has not established, by a preponderance of the evidence, that the accused products meet all of the limitations of each of the dependent claims 6 and 7.

B. The '449 Patent

Complainant asserted that claims 1 and 4 of the '449 patent are infringed by the same chips that it asserted infringed claims 1, 6 and 7 of the '969 patent.

With respect to claims 1 and 4 of the '449 patent, while the administrative law judge finds that complainant has established, by a preponderance of the evidence, that the accused chips are "nonvolatile semiconductor memory devices" that have:

> a memory cell array comprising memory cells arranged in matrix form having first row lines, second row lines, and column lines, each memory cell including cell transistors and a selection transistor for selecting the memory cell, and each of the cell transistors having a control gate, a floating gate, a channel region, and an insulation film formed between the floating gate and the channel region for electrically storing data by using charges stored in the floating gate, each memory cell having a first terminal and a second terminal, the first terminals of the memory cells in the same column being commonly connected to one of the column lines, the second terminals of the memory cells being connected to a reference potential, the control gates of the cell transistors in the same row being commonly connected to one of the first row lines, and the gate of the selection transistor being connected to one of

the second row lines, (memory cell limitation)[42]

and "first switching means connected between each of the second terminals of the memory cells and the reference potential, for disconnecting the memory cell from the reference potential when the data programming means stores data," he finds that complainant has not met its burden, by a preponderance of the evidence, in establishing that the accused chips have:

> data programming means for selectively storing data into the cell transistors by one of injecting electrons through the insulation film into the floating gate (by utilizing a tunnel effect), and emitting electrons through the insulation film from the floating gate (by utilizing a tunnel effect).[43]

He further finds that complainant has not met its burden by establishing that the accused chips have "row selection means for applying a signal to one of the first row lines and applying a signal to one of the second row lines in response to a row selection signal, thereby selecting a cell transistor connected to the first row line and a selection transistor connected to one of the second row lines," and,

> second switching means for controlling whether or not the signal from the row selection means should be applied to the cell transistor in the memory cell, the second switching means being connected between the row selection means and the memory cell, wherein (the second switching means is turned on when the memory cell which is connected to the second switching means is selected, and) the second switching means is turned off when the

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[42] Respondents argued that complainant adopted a new interpretation for the claim term "channel region" of the memory cell array limitation, under which respondents' accused products do not infringe the asserted claims. (RBr at 144.) As the administrative law judge did with respect to his treatment as to alleged infringement of claims 1, 6 and 7 of the '969 patent, supra, he rejects respondents' argument.

[43] Claim 1 of the '449 patent includes the language that is in parenthesis in the body of the text, and claim 4 of the '449 patent omits said language. Aside from those differences said claims are identical. Hence the administrative law judge is treating claims 1 and 4 identically.

memory cell which is connected to the second switching means is not selected.[44]

1. Claims 1 And 4

a. "data programming means for selectively storing data into the cell transistors by one of injecting electrons through the insulation film into the floating gate (by utilizing a tunnel effect), and emitting electrons through the insulation film from the floating gate (by utilizing a tunnel effect)"[45]

For both claims 1 and 4 of the '449 patent, complainant argued that each of respondents' representative NAND flash devices{

} (CBr at 64, 72.) It was also argued that the transistor is the same as or equivalent to a corresponding structure disclosed in the specification, the transistor 81 in Figure 18A. (CBr at 64, 72; TFF 611-627, 675-676, 678, 680-683, 685-689.) It was further argued that the "data programming means" element corresponds to the

{

} (CBr at 64-65, 72; TFF 613-614, 617-621, 675-676, 678.)

For both claims 1 and 4 of the '449 patent, respondents incorporated by reference the relevant noninfringement arguments they gave for the '969 patent's "data programming means." (RBr at 140-141; RPFF 2666-2672).

The staff argued that because claims 1 and 4 of the '449 patent contain similar limitations

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[44] Claim 1 of the '449 patent includes the language that is in the parenthesis in the body of the text, and claim 4 of the '449 patent omits said language. Aside from those differences said claims are identical. Hence the administrative law judge is treating claims 1 and 4 identically.

[45] The text in the parentheses are present in claim 1 of the '449 patent, but are omitted in claim 4 of the '449 patent.

to the limitations of claim 1 of the '969 patent, except that they eliminate a limitation to a "column selection means" and add a limitation to a "second switching means" and because complainant has shown that respondents' accused products have a{

} (SBr at 41-42.)

For the reasons stated supra, for the "data programming means" limitation of the '969 patent, the administrative law judge finds that none of complainant's evidence establishes, by preponderance of the evidence, that any of respondents' products contain structure identical to the entire circuit of Figure 18A of the '449 patent and that complainant provided no evidence of infringement under any other corresponding structure. Hence, the administrative law judge finds that complainant has not established, by a preponderance of the evidence, that the accused products literally meet all the limitations of the claimed phrase-at-issue.

For the reasons stated supra, for the "data programming means" limitation of the '969 patent, the administrative law judge finds that complainant failed to establish, by preponderance of the evidence, that any of respondents' products contained structure that was equivalent to the entire circuit of Figure 18A or any other structure besides transistor 81 of Figure 18A disclosed in the specification of the '449 patent. Hence, the administrative law judge finds that complainant has not established, by a preponderance of the evidence, that the accused products meet all of the limitations of the claimed phrase-at-issue under the doctrine of equivalents.

b. "row selection means for applying a signal to one of the first row lines and applying a signal to one of the second row lines in response to a row selection signal, thereby selecting a cell transistor connected to the first row line and a selection transistor connected to one of the second row lines"

For both claims 1 and 4 of the '449 patent, complainant argued that each of respondents' NAND flash devices includes{

} (CBr at 65-66, 73.) Complainant further argued that the row selection circuitry is the same as or equivalent to the corresponding structure disclosed in the specification, specifically, row decoder 53, particularly as it is employed in Figure 17 of the '449 patent. (CBr at 66, 73; TFF 628-644.) Complainant also argued that in respondents' representative parts,{

} (CBr at 66, 73.) {

}

(CBr at 66, 73.)

For both claims 1 and 4 of the '449 patent, respondents argued that under respondents' claim interpretation of the corresponding structure requiring both row decoder 53 and column decoder 55 of Figure 10 of the '449 patent, there is no possible infringement, because column decoder 55 in the '449 patent is a "nonstandard decoder" which selects all the lines to the left of any particular line rather than selecting one of "m" lines. (RBr at 141; RPFF 2678-2679.) Respondents argued that this "nonstandard decoder" does not exist and does not have any equivalent structures in respondents' accused products. (RBr at 141; RPFF 2679-2680.) It is also argued that even if complainant's interpretation requiring only row decorder 53 is adopted, there would still be no infringement{

} (RBr at 141-142; RPFF 2684-2688, 2690-2693.) It is also argued that the accused structures do not infringe because they are not structurally or operationally equivalent to complainant's proposed corresponding structure of row decoder 53 combined with Figure 17. (RBr at 142.) In addition, respondents raised similar arguments that they raised with respect to "row selection means" for the '969 patent. (See RBr at 143; RPFF 2694-2700.)

The staff argued that because claims 1 and 4 of the '449 patent contain similar limitations to the limitations of claim 1 of the '969 patent, except that they eliminate a limitation to a "column selection means" and add a limitation to a "second switching means" and because complainant has shown that respondents' accused products have a "second switching means" by { } claims 1 and 4 of the '449 patent are infringed by respondents' accused products. (SBr at 41-42.)

For the reasons stated supra, for the "row selection means" limitation of the '969 patent, the administrative law judge finds that the structure that comprises{ } is not equivalent structure to row decoder 53 and column decoder 55 of the embodiment of the '449 patent that uses the combination of the circuits of Figures 10 and 17.[46]

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[46] As found in the claim interpretation section supra, because of the added limitation of the "second switching means" limitation in the '449 patent, as opposed to the '969 patent, either the embodiment that comprises the circuit of Figure 10 combined with the circuit of Figure 17, or the embodiment that comprises the circuit of Figure 10 combined with the circuit of Figure 17 combined with the circuit of Figure 18A, is required, and thus, the corresponding structure for the "row selection means" is both row decoder 53 and column decoder 55. However, the administrative law judge finds that the{ } within respondents' accused products are not identical or equivalent to row decoder 53 and column decoder 55 for the reasons stated for the "row selection means" of the '969 patent, as found in the

Hence, the administrative law judge finds that complainant has not established, by a preponderance of the evidence, that the accused products literally meet all the limitations of the claimed phrase-at-issue.

For the reasons stated supra, for the "row selection means" limitation of the '969 patent, the administrative law judge finds that the structure that comprises the{

} is not equivalent structure to row decoder 53 and column decoder 55 of the embodiment of the '449 patent that uses the combination of the circuits of Figures 10 and 17. Hence, the administrative law judge finds that complainant has not established, by a preponderance of the evidence, that the accused products meet all of the limitations of the claimed phrase-at-issue under the doctrine of equivalents.

c. "second switching means for controlling whether or not the signal from the row selection means should be applied to the cell transistor in the memory cell, the second switching means being connected between the row selection means and the memory cell, wherein (the second switching means is turned on when the memory cell which is connected to the second switching means is selected, and) the second switching means is turned off when the memory cell which is connected to the second switching means is not selected"[47]

For both claims 1 and 4 of the '449 patent, complainant argued that each of respondents' representative NAND flash devices includes{

} (CBr at 69, 76-77; TFF 649-656, 711-713.) Complainant

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infringement section for the '969 patent. supra.

[47] The text in the parentheses is present in claim 1 of the '449 patent, but are omitted in claim 4 of the '449 patent.

also argued that the "second switching means" element corresponds to the transistors passing the {

} (CBr at 69, 77; TFF 649-654, 711-713.)

Complainant further argued that each of the{

} (CBr at 69, 77; TFF 649-654, 711-713.)

For both claims 1 and 4 of the '449 patent, respondents argued that respondents' accused devices'{

} (RBr at 143.)

Respondents argued that{

} (RBr at 143-144; RPFF 2705-2707.) Respondents further argued that respondents' accused products{

} (RBr at 144; RPFF 2708-2709.) Instead, respondents argued,{

} (RBr at 144; RPFF 2711.)

The staff argued that because claims 1 and 4 of the '449 patent contain similar limitations to the limitations of claim 1 of the '969 patent, except that they eliminate a limitation to a "column selection means" and add a limitation to a "second switching means" and because complainant has shown that respondents' accused products have a "second switching means" by {

} (SBr at 41-42.)

With respect to the "second switching means" of the '449 patent, the claim language reads as follows:

> second switching means for controlling whether or not the signal from the row selection means should be applied to the cell transistor in the memory cell, the second switching means being connected between the row selection means and the memory cell, wherein (the second switching means is turned on when the memory cell which is connected to the second switching means is selected, and) the second switching means is turned off when the memory cell which is connected to the second switching means is not selected ...[48]

(JX-7 at 22:23-33, 24:30-37.) In addition, the specification of the '449 patent describes the QT transistors (i.e. the "second switching means") as follows:

> The circuit of FIG. 17 ... includes MOSFETs QT1, QT2, ... which are connected to the control gates of the cell transistors and whose conduction states are controlled by signals X1, X2, ... Since signals are input through MOSFETs QT1, QT2, ... a desired one of the memory cell blocks can be programmed by selectively satisfying a logical condition determined by a combination of signals W11, W12, ... and signals Z2 to Zm supplied to corresponding memory cell blocks to selectively set signals W1n1,

[48] The text in the parentheses is present in claim 1 of the '449 patent, but are omitted in claim 4 of the '449 patent.

..., W121, W111 to a high voltage level.

(JX-7 at 11:28-38 (emphasis added).) Based on the foregoing, the administrative law judge finds

{

} The administrative law judge further finds that the{

} The administrative law judge also finds that based on the

{

} While

the administrative law judge finds that the{

}

the administrative law judge finds that, because respondents'{

}

Based on the foregoing, the administrative law judge finds that complainant has not established, by a preponderance of the evidence, that the accused products literally meet all the limitations of the claimed phrase-at-issue.

As found supra, the pass transistors in respondents' accused products interpret{

} Hence, the administrative law judge finds that complainant has not established, by a preponderance of the evidence, that the accused products meet all of the limitations of the claimed phrase-at issue, under the doctrine of equivalents.

Complainant argued that{ } are present in an alternative embodiment that combines Figure 10, 17, and 18A of the '449 patent as provided in the specification. (CRBr at 54.) However, as found supra, the specification only calls for the

{

} (See JX-7 at 11:45-65.)

C. The '178 Patent

Complainant asserted that claims 1-5 of the '178 patent are infringed by respondents'

{

} (SPFF 12 (undisputed).) These NAND flash memory devices include respondents'

{ } NAND flash products.[50] (SPFF 12 (undisputed).) Respondents' { } is representative of all respondents' NAND flash memories manufactured at the{

} (TFF 1050 (undisputed).) Further, respondents' 512 Mb NAND flash memory manufactured{ } is representative of all respondents' NAND flash memories manufactured at the { } (TFF 1051 (undisputed).)

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[49] The sizes specified are in nanometers (nm), referring to feature sizes within the integrated circuits.

[50] The abbreviations "Mb" and "Gb" refer to megabits and gigabits, indicating the memory storage capacity of the devices.

While the administrative law judge finds that complainant has established, by a preponderance of the evidence, that the accused chips have "element forming regions" (claim 1), "first gate electrodes formed on said element forming regions, the first gate electrodes being separated from each other by a predetermined width" (claim 1), "an insulating film formed to define grooves having substantially the same width between said first gate electrodes" (claim 1), "first gate electrodes" (claim 5), "an insulating film formed on said first gate electrodes and defining grooves having a substantially same width between said first gate electrodes" (claim 5) and "a second gate electrode formed on said insulating film" (claim 5), he finds that complainant has not met its burden in establishing that the accused chips have a "field oxidation film of a predetermined pattern" (claim 1), "surfaces of those portions of said polysilicon layer which are above said grooves being substantially flat." (claim 1), "semiconductor element regions" (claim 5), and "a surface portion of said polysilicon layer at positions corresponding to said grooves being substantially planar" (claim 5). Hence, he finds that complainant has not established, by a preponderance of the evidence, that the asserted claims of the '178 patent are infringed.

1. Claim 1

a. "field oxidation film of a predetermined pattern"

As seen, supra, the claimed phrase "field oxidation film of a predetermined pattern" appears in the second clause of independent claim 1 of the '178 patent, which reads: "a field oxidation film of a predetermined pattern formed on said semiconductor substrate, for defining element forming regions in which semiconductor elements are formed." (JX-1 at 4:59-62 (emphasis added).)

Complainant argued that each of the Hynix NAND flash devices includes an{

} (CBr at 168.)

Respondents argued that the accused Hynix NAND flash products do not infringe the limitation of "a field oxidation film of a predetermined pattern" literally because they have{

}

(RBr at 152-53.)

The staff argued that the evidence shows that none of the accused Hynix products infringe the "field oxidation film of a predetermined pattern" limitation; that the Hynix products do not infringe because this limitation requires that the film be formed using a thermal oxidation process (described in the patent as LOCOS); that{

} (SBr at 34-35.)

As indicated, supra, the administrative law judge has interpreted the claimed phrase "field oxidation film of a predetermined pattern" to mean "a field oxide layer formed by field oxidation, which is a process by which the field oxide is grown in the field region of the semiconductor substrate by the thermal oxidation of the substrate."

It is undisputed that both the{

}(RPFF 3672 (undisputed).) It is also undisputed that

{

} (RPFF 3708 (undisputed).) Respondents' expert

Bravman explained that in comparing the claimed "field oxidation film" to the{

} the formation process is field oxidation, or growth, for the "field oxidation film" and{ } (Bravman, Tr. at 2161-64, 2203-07.)

Bravman further explained that in comparing the claimed "field oxidation film" to the{

}

(Bravman, Tr. at 2203:7-13.) Significantly, complainant's expert Antoniadis testified that the Hynix NAND flash products would not literally infringe the limitation "field oxidation film" if that term means a film formed by a thermal oxidation process. (RPFF 3675 (undisputed).) Moreover, Antoniadis does not contend that the{

} (RPFF 3692 (undisputed).) Hence, the administrative law judge finds that respondents' accused products do not have field oxide grown by thermal oxidation of the silicon substrate as required by the claimed phrase "a field oxidation film of a predetermined pattern."

Complainant argued that respondents' NAND flash products infringe the second clause of claim 1 under a doctrine of equivalents analysis; that the function of the "field oxidation film" is stated in the claim as "defining element forming regions"; {

} is explained in the specification as providing "isolation" and said "isolation" creates the active areas in which the semiconductor devices are built. (CBr at 168-69.)

Respondents argued that{

} while the way the "field oxidation film" simultaneously defines the active areas and isolates the active areas is through the growth of the silicon oxide. (RRBr at 93.)

The staff argued that the evidence shows that Hynix' accused products do not meet the limitation in issue under the doctrine of equivalents; that the function of the field oxidation film is to isolate the element forming regions, thus defining the active regions of the device;{

} (SBr at 35.)

The administrative law judge finds that the way of forming isolation regions in the accused products is substantially different since{ } while field oxidation is growth based. (Antoniadis, Tr. at 527; Bravman, Tr. at 2210-12.) The administrative law judge further finds that the results are substantially different{

}

that would result from a thermal oxidation process. (Id.)

Based on the foregoing, the administrative law judge finds that complainant has not established, by a preponderance of the evidence, that the accused products meet the limitation "a field oxidation film of a predetermined pattern."

b. "surfaces of those portions of said polysilicon layer which are above said grooves being substantially flat"

Complainant argued that because the proper time to measure substantial flatness is in a completed NAND flash device, the polysilicon layer in the representative Hynix devices is "substantially flat" as shown by the TEMs produced by both of the private parties in this investigation. (CRBr at 118.)

Respondents argued that Toshiba has not proffered any evidence as to what the surface of the polysilicon layer of the control gate in the Hynix products looked like after deposition and before subsequent processing that forever altered the topology of the surface; and that even if flatness and planarity were measured in the final structure of a Hynix product, there are still fatal problems with respect to a lack of evidence as to metal cracking or lack of metal cracking in the Hynix products. (RRBr at 100-101.)

The staff argued that Toshiba's evidence is flawed because it does not show the polysilicon layer before the next layer is formed; that it is impossible to tell from the SEM and TEM evidence whether the polysilicon layer was flat when it was deposited; and that based on this fundamental lack of evidence, one skilled in the art would not understand that the polysilicon layer in Hynix' accused processes was "substantially flat" as required by claim 1 of the '178 patent. (SBr at 37.)

As seen, supra, the administrative law judge has interpreted the claimed phrase "substantially flat" to mean a surface which substantially eliminates the topographical features of the underlying structure and thus does not require perfect flatness or anatomic flatness, and that the substantial flatness should be determined after the polysilicon layer is deposited but before any subsequent processing. No evidence has been presented by complainant showing what the surface of the polysilicon layer looks like after deposition of said polysilicon layer and before subsequent processing. (See Bravman, Tr. at 2226-27 see also Antoniadis, Tr. at 626:19-25.)

Based on the foregoing, the administrative law judge finds that complainant has not established, by a preponderance of the evidence, that the accused products have the "surfaces of those portions of said polysilicon layer which are above said grooves being substantially flat" limitation.

2. Claim 5

a. "a semiconductor substrate having semiconductor element regions"

Complainant argued that the accused Hynix products have "a semiconductor substrate having semiconductor element regions." (CBr at 148.)

Respondents argued that the accused Hynix NAND flash products do not infringe claim element "a semiconductor substrate having semiconductor element regions" because they do not have the claimed "semiconductor element regions." (RBr at 184.)

As seen, supra, the administrative law judge has interpreted the claimed phrase "semiconductor element regions" to mean active regions separated by isolation regions and topped by a non-conductive film, where said isolation regions include 'field oxidation film" but said isolation regions are not formed by a trench isolation process such as STI.

It is undisputed that both the{

} (RPFF 3692 (undisputed).) See also Bravman, Tr. at 2237-39. Hence, the administrative law judge finds that respondents' accused products' isolation regions are{ }but said isolation regions do not include "field oxidation film" as required by the claimed phrase "semiconductor element regions."

Based on the foregoing, the administrative law judge finds that complainant has not established, by a preponderance of the evidence, that the accused products literally meet all of the limitations of the claimed phrase "a semiconductor substrate having semiconductor element regions."

b. "a surface portion of said polysilicon layer at positions corresponding to said grooves being substantially planar"

Complainant argued that the accused Hynix products have "a surface portion of said polysilicon layer at positions corresponding to said grooves being substantially planar." (CRBr at 96.)

Respondents argued that the accused Hynix NAND flash products do not infringe the limitation "a surface portion of said polysilicon layer at positions corresponding to said grooves being substantially planar" of claim 5 for the same reasons the limitation "surfaces of those portions of said polysilicon layer which are above said grooves being substantially flat" of claim 1 is not infringed. (RBr at 189.)

The staff argued that all parties construe "substantially planar" of claim 5 to be the same as "substantially flat" of claim 1, and thus, Hynix' accused products do not infringe the substantially planar limitation of claim 5 for the same reasons stated in regard to claim 1. (SBr at 38.)

Based on the findings with regard to the claimed phrase "surfaces of those portions of said polysilicon layer which are above said grooves being substantially flat" of claim 1, supra, the administrative law judge finds that complainant has not established, by a preponderance of the evidence, that the accused products literally meet all of the limitations of the claimed phrase "a surface portion of said polysilicon layer at positions corresponding to said grooves being substantially planar" of claim 5.

3. Dependent Claims 2, 3 And 4

Complainant argued that the accused Hynix NAND flash products infringe each of the dependent claims 2, 3 and 4. (CBr at 176-79.)

Respondents argued that the accused Hynix NAND flash products do not infringe each of the dependent claims 2, 3 an 4 for the same reasons they do not infringe claim 1. (RBr at 183-84.)

The staff argued that claims 2-4 are dependent on claim 1, and thus Hynix' accused products do not infringe claims 2-4 for the same reasons stated for claim 1. (SBr at 38.)

Claim 2 depends on claim 1 and recites a further limitation "wherein those portions of said polysilicon layer which are above said element forming regions have a thickness larger than ½ said width of said grooves." (JX-1 at 5:10-13.) Claim 3 depends on claim 1 or claim 2, and recites a further limitation "wherein said grooves are above said field oxidation film." (JX-1 at 5:14-16.) Claim 4 depends on claim 1 or claim 2, and recites a further limitation "wherein said

high melting point metal is one selected from a group of tungsten, molybdenum, copper, and titanium." (JX-1 at 5:17-20.)

As seen, supra, the administrative law judge found that complainant has not established, by a preponderance of the evidence, that the accused products meet all of the limitations of independent claim 1.

Based on the foregoing, the administrative law judge finds that complainant has not established, by a preponderance of the evidence, that the accused products literally meet all of the limitations of each of the dependent claims 2, 3 and 4.

IX. Validity (Prior Art)

A patent issued from the Patent Office bears the presumption of validity. 35 U.S.C. § 282. The party challenging a patent's validity has the burden of overcoming this presumption by clear and convincing evidence. Advanced Display Sys., Inc. v. Kent State Univ., 212 F.3d 1272 (Fed. Cir. 2000). An analysis for anticipation under section 102 is a two-step inquiry. Power Mosfet Technologies, L.L.C. v. Siemens AG, 378 F.3d 1396, 1406 (Fed. Cir. 2004). The first step requires construing the claim, which is a question of law to be decided by the administrative law judge. Oakley, Inc. v. Sunglass Hut Int'l, 316 F.3d 1331, 1339 (Fed. Cir. 2003); Markman v. Westview Instruments, Inc., 52 F.3d 967, 970-71 (Fed. Cir. 1995). The second step requires a comparison of the properly construed claims to the prior art, which is a question of fact. Power Mosfet, 378 F.3d at 1406; Oakley, 316 F.3d at 1339.

A patent claim is invalid for anticipation if a prior art reference discloses, either expressly or inherently, all of the limitations of a claim. EMI Group N. Am., Inc. v. Cypress Semiconductor Corp., 268 F.3d 1342, 1350 (Fed. Cir. 2001) (citation omitted). As to any inherent disclosure of

a prior art reference, the Federal Circuit has stated:

> To serve as an anticipation when the reference is silent about the asserted inherent characteristic, such gap in the reference may be filled with recourse to extrinsic evidence. Such evidence must make clear that the missing descriptive matter is necessarily present in the thing described in the reference, and that it would be so recognized by persons of ordinary skill.

Metabolite Labs., Inc. v. Laboratory Corp. Of America Holdings, 370 F.3d 1354, 1367 (Fed. Cir. 2004).

Under 35 U.S.C. § 103, a patent is valid unless "the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains." The ultimate question of obviousness is a question of law, but "it is well understood that there are factual issues underlying the ultimate obviousness decision." Richardson-Vicks Inc. v. The Upjohn Co., 122 F.3d 1476, 1479 (Fed. Cir. 1997); Lockwood v. American Airlines, Inc., 107 F.3d 1565, 1570 (Fed. Cir. 1997).

After construing the claims, the next "step in an obviousness inquiry is to determine whether the claimed invention would have been obvious as a legal matter, based on underlying factual inquiries including: (1) the scope and content of the prior art; (2) the level of ordinary skill in the art; (3) the differences between the claimed invention and the prior art; and (4) secondary considerations of nonobviousness, also known as 'objective indicia of nonobviousness." Ruiz, 234 F.3d at 660; Graham v. John Deere Co., 383 U.S. 1, 17 (1966). Secondary considerations, also part of the Graham factors, include commercial success, long-felt but unresolved need, failure of others, copying, and unexpected results. Id.

With respect to the scope and content of the prior art, as the Federal Circuit stated in State Contracting & Engineering Corp. v. Condotte America, Inc., 346 F.3d 1057 (Fed. Cir. 2003), citing In re Clay, 966 F.2d 656, 658 (Fed. Cir.1992): "A prerequisite to making a finding on the scope and content of the prior art is to determine what prior art references are pertinent." References within the statutory terms of 35 U.S.C. § 102 (anticipation) can qualify as prior art for an obviousness determination only when analogous to the claimed invention. In re Clay, 966 F.2d 656, 658 (Fed. Cir. 1992). The Federal Circuit restated the test for determining the scope and content of the prior art to be considered for obviousness purposes in In re Bigio as follows:

> Two separate tests define the scope of analogous prior art: (1) whether the art is from the same field of endeavor, regardless of the problem addressed and, (2) if the reference is not within the field of the inventor's endeavor, whether the reference still is reasonably pertinent to the particular problem with which the inventor is involved. In re Deminski, 796 F.2d 436, 442 (Fed. Cir.1986); see also In re Wood, 599 F.2d 1032, 1036 (CCPA 1979).

In re Bigio, 381 F.3d 1320, 1325 (emphasis added); accord State Contracting, 346 F.3d at 1069. One of ordinary skill in the art would have known of such art because such a person is a hypothetical person who is presumed to be aware of all the pertinent prior art. Custom Accessories, Inc. v. Jeffrey-Allan Industries, Inc., 807 F.2d 955, 962 (Fed. Cir. 1992).

When combining references in an attempt to show obviousness, the accused infringer must make "a showing of a suggestion, teaching, or motivation to combine the prior art references." Brown & Williamson Tobacco Corp. v. Philip Morris Inc., 229 F.3d 1120, 1124-25 (Fed. Cir. 2000). To prove obviousness, a respondent must establish that "there is a reason, suggestion, or motivation in the prior art that would lead one of ordinary skill in the art to combine the references, and that would also suggest a reasonable likelihood of success." Smiths

Indus. Medical Sys., Inc. v. Vital Signs, Inc., 183 F.3d 1347, 1356 (Fed. Cir.); see also United States Surgical Corp. v. Ethicon, Inc., 103 F.3d 1554, 1564 (Fed. Cir. 1997). The "references in combination must suggest the invention as a whole." In the Matter of Certain ERPROM, EEPROM, Flash Memory, and Flash Microcontroller Semiconductor Devices and Products Containing Same, Inv. No. 395, Final, Init. and Recommended Determinations, (Mar. 19, 1998). In the absence of a suggestion to combine references, "one can do no more than piece the invention together using the patented invention as a template; such hindsight reasoning is impermissible." Id. at 140-41 (citations omitted). Furthermore, the Federal Circuit has held that not only must a motivation to combine the references exist but the motivation must be directed toward combining prior art references in the particular manner claimed. See In re Kotzab, 217 F.3d 1365, 1371 (Fed. Cir. 2000); In re Rouffet, 149 F.3d 1350, 1357 (Fed. Cir. 1998). The patent challenger "must show reasons that the skilled artisan, confronted with the same problems as the inventor and with no knowledge of the invention, would select elements from the cited prior art references for combination in the manner claimed." Rouffet at 1357. The Federal Circuit has rejected "broad conclusory statements regarding the teaching of multiple references" so as to guard against "the subtle but powerful attraction of a hindsight-based obviousness analysis." In re Dembiczak, 175 F.3d 994, 999 (Fed. Cir. 1999).

A. The '969 And '449 Patents Under § 103

Respondents argued that, based on the evidence presented by their expert Pashley, both the '969 and '449 patents are invalid as obvious in light of prior art under 35 U.S.C. § 103. It is argued that Pashley presented four prior art references pertinent to his analysis of the invalidity of the '969 and '449 patents; that those references fall into two categories: those which disclose

memory cell transistors connected in series ("NAND references") and those which disclose Fowler-Nordheim tunneling between the floating gate and the drain or channel region of a cell transistor ("tunneling references"); that to one of ordinary skill in the art, the combination of U.S. Patent No. 4,933,904 (NAND reference) and a Kuo paper in the IEEE Journal of Solid-State Circuits (October 1982) (tunneling reference) contains each and every limitation of claim 1 of the '969 patent under Toshiba's construction of the asserted patents; that to one of ordinary skill in the art, the combination of an Adler paper entitled "Densely Arrayed EEPROM Having Low-Voltage Tunnel Write" in the IBM Technical Disclosure Bulletin (NAND reference) and the Kuo paper contains each and every limitation of claim 1 of the '969 patent; that to one of ordinary skill in the art, the combination of the Adler paper and a Cioaca paper published in October 1987 in IEEE Journal of Solid State Circuits (tunneling reference) contains each and every limitation of claim 1 of the '969 patent; and that to one of ordinary skill in the art, the combination of the '904 patent and the Cioaca paper contains each and every limitation of claim 1 of the '969 patent. (RBr at 190-4.)

Respondents, with respect to their alleged obviousness of dependent claim 6 of the '969 patent in light of the prior art relies on the combination of the '904 patent and the Kuo paper, the combination of the Adler paper and the Cioaca paper, the combination of the Adler paper and the Kuo paper and the combination of the '904 patent and the Cioaca paper and asserted that complainant's expert Reed does not dispute that each of said combinations disclose the "selector transistors" limitation of claim 6 of the '969 patent. (RBr at 194-5.) As to the alleged obviousness of dependent claim 7 of the '969 patent, respondents rely on each of said combinations and asserted that complainant's expert Reed does not dispute respondents

Pashley's conclusion that each of said combinations disclose the "switching means" limitation of claim 7. (RBr at 195-6.)

Respondents argued that claims 1 and 4 of the '449 patent are obvious based on each of the combination of the '904 patent and the Kuo paper, the combination of the Adler paper and the Cioaca paper, the combination of the Adler paper and the Kuo paper, and the combination of the '904 patent and the Cioaca paper. (RBr at 196-7.)

It is argued by respondents that each asserted prior art combination expressly identifies suggestions that would lead one skilled in the art to combine a NAND reference with a tunneling reference; and that the tunneling references suggest advantageous programming/erasing approaches, whereas the NAND references suggest an architecture to increase the density of a nonvolatile memory. Specifically, respondents argued that the '904 patent teaches one of ordinary skill in the art the use of a NAND structure to achieve a higher memory density and teaches enhanced Fowler-Nordheim tunneling, i.e., between the control gate and the floating gate. (RPFF 5810, 5812 (undisputed).) Respondents also argued that the Kuo paper teaches one of ordinary skill the art that tunneling through the "bottom dielectric," i.e., the oxide between the floating gate and the channel region, provides better process control than using enhanced Fowler-Nordheim tunneling (i.e., between the control gate and the floating gate) and that a lower trap density provides the device with higher program-erase endurance. (RPFF 5805-5809 (undisputed).) In addition, respondents argued that the Adler paper teaches one of ordinary skill in the art the use of a NAND structure to achieve a higher memory density. (RPFF 5812 (undisputed).) Respondents further argued that the Cioaca paper teaches that using a tunneling dielectric underneath the floating gate allows for higher data retention than a device using

enhanced Fowler-Nordheim tunneling. (RPFF 5814-5815.)

Respondents further argued that when viewed in light of the Kuo paper's teachings, one of ordinary skill in the art would replace the enhanced Fowler-Nordheim tunneling of the '904 patent with the tunneling taught by the Kuo paper. (RPFF 5811.) Respondents also argued that one of ordinary skill in the art would be motivated to combine the Adler paper with the Cioaca paper. (RPFF 5818.) Respondents further argued that one of ordinary skill in the art would be motivated to combine the Adler paper with the Kuo paper. (RPFF 5821.) Respondents also argued that one of ordinary skill in the art would be motivated to combine the '904 patent with the Cioaca paper. (RPFF 5824.[51])

Complainant argued that the evidence presented by Hynix falls far short of a clear and convincing showing that the claims of the '969 or '449 patents cited by respondents are invalid. It is argued that each of the asserted combinations is missing a number of elements of the asserted claims of the '969 and '449 patents. In addition, it is argued that Cioaca is not prior art. (CRBr at 129-130.)

The staff argued that if the administrative law judge assumes that Hynix cited references disclose exactly what Hynix asserts they disclose, Hynix still has not shown a motivation to combine any two or more of the cited prior art references to arrive at the specific invention of the asserted claims in issue of the '969 and '449 patents; that for example, all of the references showing tunneling are based on NOR technology; that due to the differences between NAND and

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[51] The text of RPFF 5824 actually references the Adler paper and the Kuo paper. However, the factual finding is under the heading "The '904 patent and the Cioaca paper," and the rest of the factual findings under this heading reference the '904 patent and the Cioaca paper. Hence, despite the plain language of the factual finding, the administrative law judge treats this finding as though it references the '904 patent and the Cioaca paper.

NOR technology, one of ordinary skill in the art at the time of the invention would likely not have been be motivated to combine NAND and NOR art in the way suggested by Hynix; and that, for example, citing Tr. at 2547-63, Pashley worked in the NOR flash industry but could not point to a time prior to the filing date of the patent application in issue when he discussed combining NOR and NAND. (SBr at 50.)

The staff further argued that, while complainant has provided no evidence that the particular innovations in the '969 and '449 patents, in the context of the thousands of innovations included in NAND flash chips, have resulted in any increased sales in its products and that on the whole, the objective evidence does not support the conclusion that the inventions recited in the claims are non-obvious, respondents have failed to prove that the '969 and '449 patents are obvious. (SBr at 50-51.)

The administrative judge finds all of respondents' argued combinations rely on the presumption that a reading of both a NAND reference and a tunneling reference would motivate one of ordinary skill in the art to replace the enhanced Fowler-Nordheim tunneling (i.e., tunneling between the control gate and the floating gate) taught in the NAND references with the tunneling process (i.e., tunneling between the floating gate and the channel region) taught in the tunneling references. However, the administrative law judge finds that all of the tunneling references (assuming the Cioaca paper is prior art) are based on NOR flash EEPROM technology, whereas the NAND references are based on NAND flash EEPROM technology. (See Pashley Tr. at 2478:6-2483:3, 2483:22-25; RDX-132-137; RDX-139.) Respondents' expert Pashley, testified as to the significant differences between NAND and NOR technology that weigh against finding a motivation to combine one of respondents' NAND references with one

of respondents' NOR references:

Q. Let me focus on the time period leading up to 1987. During that time period, let's say '85 to '87, during that period you would have had at least 70 engineers who would qualify under your definition of being skilled in the art, as being such working for you; is that correct?

A. That's true. They just weren't all working on flash. I think you indicated in your first question NAND flash. But as far as someone skilled in the art, I would agree with you because that covers EPROM and other technologies besides just flash.

Q. In -- during that period that you were involved in flash development, you don't recall any of those engineers ever coming up to you and proposing to you a NAND flash technology, correct?

A. That's very true. But as -- as you have noticed from my slides earlier, I was in the NOR business, not the NAND business.

* * *

THE WITNESS: Now let me add one thing. Clearly there were other people working on NAND technology. Just because I wasn't working on technology doesn't mean that there weren't universities working on it and there weren't companies working on it. Clearly, Toshiba was working on it and there were other companies working on it as well. I was not motivated to do that because I was dedicated to the NOR flash technology.

* * *

Q. With all of those combinations out there, all of the motivation to combine them, according to your testimony, all of the skilled engineers, including those working for you, looking for better ways to

have better NAND flash products, do you really think -- well, looking for better ways to have nonvolatile memory products.

A. Thank you.

Q. Do you think it's fair to say the combination arrived at by Mr. Iwahashi was obvious, when none of those people found and created that combination?

A. Yes, I do. As I pointed out earlier, all of my people were focused on one goal, and that was to build the equivalent of a gasoline engine, a really high-speed flash memory. And unfortunately the NAND device doesn't do that. And when the NAND device was finally brought to market, it could not even cannibalize the NOR market because of this. It had to create its own market.

(Pashley, Tr. at 2547:17-2548:10, 2554:22-2555:6, 2562:11-2563:6 (emphasis added).)

Hence, the administrative law judge finds that the mere fact that the NAND references teach a different tunneling process and also teach that said tunneling process has advantages over the enhanced Fowler-Nordheim tunneling process of the tunneling references does not establish a motivation to combine any of the NAND and tunneling references.[52]

Respondents argued that other references available in the 1987 timeframe supplied the requisite motivation to combine a NAND reference (i.e., '904 patent or Adler paper) with a tunneling reference (i.e., Kuo paper or Cioaca paper). (RBr at 199; RPFF 5825.) As a representative sampling of the prior art, respondents argued that the Yaron paper and the Johnson

[52] In addition, the cited art lacks certain claim limitations. For example, while respondents argued that the Cioaca paper teaches an insulation film formed between the floating gate and the channel region for electrically storing data in the floating gate, the teaching of the Cioaca paper is directed at tunneling via an insulation film in the drain region. (Reed, Tr. at 2759-2763; RX-249 at HY79103-79014, ii. b. Memory Cell, Fig. 2(b); RX-249-A; RDX-219.)

and Perlegos paper provided ample motivation to combine a NAND reference with a tunneling reference. (RBr at 199-200; RPFF 5825-5843.) Specifically, respondents argued that the Yaron paper taught the use of a floating gate EEPROM device which used Fowler-Nordheim tunneling across a thin dielectric (insulation film) between the floating gate and the channel region. (RPFF 5835.) Furthermore, respondents argued that the Johnson and Perlegos paper taught the use of an EEPROM that uses Fowler-Nordheim tunneling through a thin oxide between the floating gate and the drain. (RPFF 5840 (undisputed).)

The administrative law judge finds that respondents failed to offer either the Yaron paper (RX-253) or the Johnson and Perlegos paper (RX-255), so identified in findings of fact RPFF 5828 and RPFF 5839, into evidence at the hearing. Respondents' counsel was contacted on October 31, 2006, and said counsel confirmed that respondents did not so offer either the Yaron paper or the Johnson and Perlegos paper into evidence. However, said counsel stated that complainant in its proposed rebuttal findings of fact at 1518, 1521 did not object to findings of fact RPFF 5828 (which references the Yaron Paper) and RPFF 5839 (which references the Johnson and Perlegos paper). Said counsel also stated that respondents' expert Pashley referenced the Yaron paper and the Johnson and Perlegos paper in his testimony. (See Pashley Tr. at 2491:16-2492:17.) The administrative law judge finds that those arguments do not change the fact that the Yaron paper and the Johnson and Perlegos paper are not part of the evidentiary record. Hence, the administrative law judge finds that respondents cannot rely on said references that are not in evidence to meet their burden of proof on patent validity.

Furthermore, similar to respondents' other obviousness arguments and assuming the Yaron paper and the Johnson and Perlegos paper are in evidence, the administrative law judge

finds that respondents' arguments with respect to said prior art rely on the presumption that either the Yaron paper or the Johnson and Perlegos paper would motivate one of ordinary skill in the art to replace the enhanced Fowler-Nordheim tunneling (i.e., tunneling between the control gate and the floating gate) taught in the NAND references with the tunneling process (i.e. tunneling between the floating gate and the channel region) taught in the tunneling references. However, there is nothing in the record to the effect that either the Yaron paper or the Johnson and Perlegos paper taught that elements of NOR technology could be combined with elements of NAND technology. (See Pashley Tr. at 2491:16-2492:18.) Hence, the administrative law judge finds that the Yaron paper and Johnson and Perlegos paper do not establish a motivation to combine any of the NAND and tunneling references.

Based on the foregoing, the administrative law judge finds that respondents have not established, by clear and convincing evidence, that asserted claims 1, 6 and 7 of the '969 patent and asserted claims 1 and 4 of the '449 patent are obvious under 35 U.S.C. § 103.

B. The '178 Patent

1. Anticipation

Respondents argued that the asserted claims 1 and 5 and/or claims 1-5 (as indicated infra) of the '178 patent are anticipated by the Sugaya Japanese Patent Publication S63-186478 (the '478 publication), which was published on August 2, 1988 (RX-32), the Sato and Yoshikawa Japanese Patent Publication S61-24283 (the '283 publication), which was published on February 1, 1986 (RX-29), the Yoshikawa Japanese Patent Publication S64-89466 (the '466 publication), which was published on April 3, 1989 (RX-33), and the Mori 1987 IEDM article (the 1987 article) published in the 1987 proceedings of the International Electron Devices meeting (JX-32).

(RBr at 207-23.)

Each of complainant and the staff argued that respondents have not established by clear and convincing evidence that any of the asserted claims of the '178 patent are anticipated.

a. The Sugaya Reference (The '478 Publication)

Respondents argued that the "substantially flat" limitation of claim 1 and the "substantially planar" limitation of claim 5 (with both private parties agreeing that "substantially flat" and "substantially planar" are equivalent terms) of the '178 patent were the only ones complainant's expert Antoniadis did not acknowledge to be present in the '478 publication (RX-32); and that the control gate polysilicon above the grooves in the '478 publication is "substantially flat" or "substantially planar." (RBr at 209, 211.)

Complainant argued that the Sugaya '478 publication discloses exactly the same thing as the Mori 1987 IEDM article that was before the Examiner and thus Hynix bears a particularly heavy burden in seeking to establish anticipation based on this reference; and that specifically, the '478 publication discloses a proposed solution to the silicide disconnection problem by thinning the floating gate to reduce the step height; and that Sugaya's proposed solution is not the invention Mori devised in the '178 patent. (CBr at 204-05.)

The staff argued that the '478 publication describes a slanted or sloped surface rather than a flat surface; and that it is clear from Figure 1 in the Sugaya reference that the surface of the polysilicon is not substantially flat. (SBr at 47.)

The '478 publication states, "the EPROM cells that used conventional polycide word lines experienced problems in that there was an increase in the word line resistance or inconsistencies caused by coverage defects in the step sections by the floating gate, and

improvement is desired." (RPFF 4309 (undisputed).) The solution to the cracking problem disclosed in the Sugaya '478 publication is to make the floating gate thickness thinner than the polysilicon layer of the control gate. (TFF 1803 (undisputed).) The Sugaya '478 publication discloses a floating gate that is as thin or thinner than the polysilicon layer of the control gate. (TFF 1808 (undisputed).) Too thin of a silicide coverage ("excessively thin," according to the Sugaya '478 publication) can lead to higher resistance. (TFF 1811 (undisputed).) In contrast, a goal of the invention of the '178 patent is described as "flatten[ing] the refractory metal silicide layer of the gate of the second level layer to avoid occurrence of cracks thereof and to reduce an increase in resistance thereof." (TFF 1825 (undisputed).)

As seen, supra, the administrative law judge has and interpreted "substantially flat" and "substantially planar" of claims 1 and 5 to mean a surface which substantially eliminates the topographical features of the underlying structure and thus does not require perfect flatness or anatomic flatness, and that the "substantial flatness" or "substantial planarity" should be determined after the polysilicon layer is deposited but before any subsequent processing.

The administrative law judge finds that the polysilicon layer shown in Figures 1 and 2 of the Sugaya '478 publication follows the contours of the grooves and is therefore not "substantially flat" (RX-32 at HY93657; Antoniadis, Tr. at 2609-10), and that the top of the polysilicon layer in the control gate in Figures 1 and 2 of the Sugaya '478 publication does not substantially eliminate the underlying topography as required by the asserted claims 1 and 5. (RX-32 at HY93657; Antoniadis, Tr. at 2609; CDX300-1, 300-2.)

Respondents, in RRTFF1816B, argued:

In the Sugaya '478 publication, the upper surface of the control gate polysilicon

> layer is formed such that it has a "slightly sloped surface" above the step sections created by the ends of the floating gates so that the metal silicide layer is "formed in more or less equal thickness" above the step sections of the floating gates. (RX-32 at HY93655, HY93657.)

However, the administrative law judge finds, in conjunction with the testimony of Antoniadis, supra, that when comparing Figures 1 and 2 of Sugaya with the prior art Figure 1C set out in the '178 patent as against Figures 2B and 2C of the '178 patent, which is illustrative of the claimed invention in issue, the Sugaya '478 publication is closer to said prior art because the top of the polysilicon layer in the control gate is substantially flatter in Figures 2B and 2C of the '178 patent than Figures 1 and 2 of Sugaya. In addition, there is no evidence what the polysilicon layer of Sugaya would look like before any further processing, the administrative law judge having determined that the "substantial flat" and "substantial planar" limitation of the polysilicon layer should be determined before any further processing.

Based on the foregoing, the administrative law judge finds that respondents have not established, by clear and convincing evidence, that the '478 publication anticipates asserted independent claims 1 and 5.

b. The Sato Reference (The '283 Publication)

Respondents argued that the '283 publication (RX-29) anticipates asserted claims 1 and 5 of the '178 patent; that respondents bear no heavy burden in seeking to prove anticipation by the '283 publication because only pages HY605-606 of a European counterpart to RX-29 (JX-22), which correspond to EP 160965 A3, were made of record in the prosecution of the '178 patent, and EP 160965 A3 does not contain the same disclosure or figures as the '283 publication;[53] and

[53] JX-22 also has HY581-604 which corresponds to EP 160965 A2, which appears to contain the disclosure and figures of the '283 publication.

that the embodiment represented in Figure 6(f) of the Sato '283 publication discloses an upper control gate polysilicon surface above the grooves that is both "substantially flat" and "substantially planar" and does not follow the underlying topography. (RRBr at 114.)

Complainant argued that the '283 publication does not anticipate any of the asserted claims of the '178 patent; that substantially the same disclosures contained in the '283 publication were before the Examiner in the '965 publication that is listed on the face of the patent; that accordingly, respondents bear a particularly heavy burden in seeking to prove anticipation based on the '283 reference; that Figure 6(f) from the '283 publication does not anticipate the asserted claims of the '178 patent because it does not satisfy the "substantially flat" limitation in claim 1 or the "substantially planar" limitation of claim 5; and that the '283 publication cannot anticipate the claims of the '178 patent because its drawings are inaccurate, and following the process disclosed in the publication would lead to a device with a polysilicon layer that is far less planar than the surface shown in Figure 6(f). (CBr at 207-08.)

The staff argued that the '283 publication reference discloses a slanted or sloped surface rather than a flat surface; and that it is clear from Figure 6 in the Sato reference that the surface of the polysilicon is not substantially flat. (SBr at 47.)

The '283 publication states that in a conventional EPROM manufacturing method, "a recessed section 9 between the floating gate electrode 6 is generated, and stress is concentrated on the control electrode which is formed on this recessed section 9." (RPFF 4497 (undisputed).) Further, the '283 publication states: "This invention has, in keeping with the above-mentioned information, the goal of providing a manufacturing method for a semiconductor device which prevents disconnection of gate electrodes at the 2nd layer or above, and along with preventing the

lowering of field voltage it provides for the high integration of elements." (RPFF 4512 (undisputed).)

As seen, supra, the administrative law judge has interpreted "substantially flat" and "substantially planar" of claims 1 and 5 to mean a surface which substantially eliminates the topographical features of the underlying structure and thus does not require perfect flatness or anatomic flatness, and that the "substantially flat" or "substantially planar" limitation should be determined after the polysilicon layer is deposited but before any subsequent processing.

At the hearing, complainant's expert Antoniadis testified:

> Q. Could you turn to CDX-300-6.
>
> A. So this is a figure from that [Sato '283] publication. It's either 1F or 6F. I don't quite recall. That shows the finished result again.
>
> We can see highlighted in yellow the area above the grooves that separate the floating gate. It would be 25 and 29 here.
>
> And as we can see, the surface of the, in this case the interface of that polysilicon with the silicide above it is essentially an exact replica of the topography underneath. And, therefore, under my definition of substantially planar, it doesn't meet that.
>
> * * *
>
> Q. Could you turn back to CDX-300-6, please. And regardless of the accuracy of the figures, do you have an opinion as to whether this figure 6F anticipates the claims of the '178 patent?
>
> A. Regardless of the accuracy, I still maintain that it does not anticipate because it doesn't meet the substantially flat, substantially planar criterion as I

have defined it.

As I pointed out earlier, the amplitude of the recess is an exact replica of the amplitude of the recess in the groove.

Q. Could you pull up RDX-482. Professor Antoniadis, do you have any comments regarding this slide from Professor Bravman's presentation?

A. So this slide is -- I think he used it to compare the features of nonplanarity. Or first let me point out what the patent really talks about is the surface of the poly, not the surface of the silicide.

So on the figure on the right, the blue line should be one level below, at the interface that we see below.

If we did that, it wouldn't change anything materially because the nonplanarity is the same both at the top and at the bottom.

We also can see very clearly here that the amplitude of the nonplanarity in the figure on the right, which is the patent in question, Sato '283, is the same as the recess -- as the groove that we started from. Pretty much the same as in the prior art figure 1C.

In figure 1C, we see that the recess shown there incorrectly in blue has the amplitude of -- which is the same as what is shown as the groove in red.

(Antoniadis, Tr. at 2618-23 (emphasis added).)

Respondents, in support of their argument that the '283 publication anticipates asserted claim 1 and 5, rely on testimony of their expert Bravman. (See RPFF 4611.) However, the administrative law judge finds that the testimony of Antoniadis is controlling.

In addition, as for alleged anticipation, there is no evidence what the polysilicon layer of the figures of the '283 publication would look like before any further processing, the

administrative law judge having determined that the "substantially flat" or "substantially planar" limitation of the polysilicon layer should be determined before any subsequent processing.

Based on the foregoing, the administrative law judge finds that respondents have not established, by clear and convincing evidence, that the '283 publication anticipates asserted independent claims 1 and 5.

c. The Yoshikawa Reference (The '466 Publication)

Respondents argued that the '466 publication (RX-33) anticipates independent claims 1 and 5 and dependent claims 2, 3 and 4 of the '178 patent; that complainant's expert Antoniadis only identified one element, "[grooves...] between said first gate electrodes," of claim 1 that he claimed was not disclosed in the '466 publication; that Antoniadis' argument equating "between" with coplanarity is inconsistent with the use of "between" in the '178 patent; and that respondents' argument with respect to "[grooves...] between said first gate electrodes" of claim 1 is equally applicable to claim 5 because the identical language appears in both claims 1 and 5 of the '178 patent. (RBr at 216-19.)

Complainant argued that the '466 publication discloses a device that would not work and it does not anticipate any of the asserted claims of the '178 patent; that as Antoniadis testified, Yoshikawa is a "somewhat odd publication" which relies on localized oxidation of poly 1 (the floating gate) to isolate the floating gates; that the '466 publication does not disclose "grooves" as that term is used in the '178 patent; and that even if the space between oxide films 18 and above region 17 could be considered "grooves," those "grooves" are not "between" the floating gates 13. (CBr at 209-10.)

The staff argued that the '466 publication discloses a groove that is above the floating

gates; and that to the extent that said reference has a groove, it is not between the floating gates.

(SBr at 48.)

The '466 publication discloses:

> The present invention relates to a method of manufacturing a semiconductor device such as an EPROM, in particular to a method of manufacturing a semiconductor device having a gate electrode structure with two or more layers." (RPFF 4687 (undisputed).) The '466 publication also states: "However, when metal layers are used for the above purpose, steps are formed during heat treatment on the aforementioned recess 9, and these steps lead to breakage. RIE (reactive ion etching) is normally used for patterning the aforementioned second polycrystalline silicon film 8, but when the high-melting-point metal layer or silicide layer is used, the etching process has low selectivity between the aforementioned layers and the silicon oxide film located underneath these layers, and this may result in excessive etching of the element separation regions 2. The same problem remains unsolved when a control gate electrode of a so-called polycide structure that comprises the polycrystalline silicon layer laminated with a high-melting-point metal layer is formed.

(RX-33 at HY93667 (emphasis added).)

Describing Figures 1(c) and 1(d), the '466 publication further discloses:

> As shown in Fig. 1(c), in this thermal oxidation process, the portion of the polycrystalline silicon layer 13 that is located in the area of the opening 14 in the silicon oxide film pattern 15 is completely oxidized, and conditions are created in which an element separation oxidation film 16 on the substrate and under the opening 14 is blown up to the thickness of about 4000 Å. As a result, the polycrystalline silicon layer 13 located in the area under the opening 14 is also oxidized and turned into the first silicon oxide film 17... Moreover, the first polycrystalline silicon layer 13 that remains in a nonoxidized state is turned into floating gate electrodes 13', and patterning is then carried out. Following this, as shown in Fig. 1(d), the entire surface of the unit is coated with a second polycrystalline silicon layer, which, after patterning, is formed into a control gate electrode, and then the aforementioned floating gate electrodes 13' are patterned for the second time.

(RX-33 at HY93669 (emphasis added).)

As seen, supra, the administrative law judge has interpreted each of the claimed phrases "grooves having substantially the same width between said first gate electrodes" of claim 1 and "grooves having a substantially same width between said first gate electrodes" of claim 5 to mean that grooves between said first gate electrodes have substantially the same separation that is not limited to a single width or a rectangular separation, and said "grooves" must be "between" said first gate electrodes, i.e., floating gate electrodes, in the sense that said grooves are in the spaces that separate said floating gate electrodes, where said grooves are substantially on the same plane as said floating gate electrodes.

Consistent with said claim interpretation that "grooves are substantially on the same plane as the floating gate electrodes," complainant's expert Antoniadis testified:

> Q. Okay. Could you turn to the next slide [CDX-300-12 showing a colorized version of Figure 1(d) of the '466 publication] and explain your conclusion as to why Yoshikawa does not disclose grooves as used within the '178 patent.
>
> A. So we can see here, we're reproducing the same picture, that all we have is a dielectric, this multilayer dielectric that runs on the poly floating gate 13, 13 prime. And then continues on onto the isolation area. So -- and then there is a separation between that insulating film edge until you go to the symmetrical structure on the other side. Because of the way this is fabricated, the -- that gap between the edges of the insulating film are well above the plane of the polysilicon floating gate 13 prime; and therefore it does not -- even if we wanted to construe this to be a groove, it certainly is not a groove between said first gate electrodes. It's actually at a level that's significantly above.
>
> Q. Did you find anything in the patent that supported your view that this does not disclose grooves between the first

gate electrodes?

A. I don't think it ever -- there was ever a reference of those grooves being between in the patent.

(Antoniadis, Tr. at 2612-13 (emphasis added).) Further, Antoniadis testified:

Q. Could you turn to CDX-300-13 [showing a colorized version of Figure 1(d) of the '466 publication], please.

A. We're here.

Q. And could you explain what this slide represents.

A. So this slide is still the same picture, colorized, that we were looking at earlier. This clearly shows that what is between the -- what occupies the space between the floating gates is this area of this blob of pink that I've identified here, which is the field oxide. And so there is no groove in between, according to the '178 patent.

(Antoniadis, Tr. at 2615 (emphasis added).) Hence, in the '466 publication, a field oxide, not a groove, occupies the entirety of the space between adjacent floating gate electrodes, and the groove is actually above the floating gate electrodes. Antoniadis also testified:

Q. Okay. Can we get RX-33C [the '466 publication]. Go to the figures, please. There you go. Can you highlight C and D at the bottom. You were discussing with Mr. McKeon some of the features of this Yoshikawa '466 publication. If you actually tried to make a device like this, what happens to what's indicated as layer 17?

A. If you tried to do this, layer 17 would certainly not be of the thickness that is indicated there. In fact, what you would wind up with is a -- is a ball by the time you finish this. That's what I meant earlier when I referred to this is a very unconventional structure.

Q. And --

A. By unconventional, of course I mean -- let me not use

> another qualifier. But an appropriate term would be goofy. So 17 thickness would have to be twice the thickness of the 13 prime from which it started. And if you did that, then you can see very clearly that what you would have is a ball in between with the -- where there would likely not even be a groove between the dielectric film.

(Antoniadis, Tr. at 2666-67 (emphasis added).) Hence, according to complainant's expert Antoniadis, if the process disclosed in the '466 publication were used, it would likely create a structure with no grooves at all. Moreover, Antoniadis' conclusion that "there would likely not even be a groove between the dielectric film," is consistent with respondents' expert Bravman's testimony that the '466 publication was attempting to "minimize the depth of the groove that must be filled." Thus, Bravman testified:

> Now if we turn to RDX-502 [respondents' overview slide of the '466 publication], I indicate that the Yoshikawa publication disclose solutions by generally forming the first silicon oxide film, which is 17 in their illustrations, to minimize the depth of the groove that must be filled.

(Bravman, Tr. at 2300 (emphasis added).)

Respondents argued that Antoniadis' testimony equating "between" with coplanarity is inconsistent with the use of "between" in the '178 patent. However, as the administrative law judge found in the claim interpretation of each of the claimed phrases "grooves having substantially the same width between said first gate electrodes" of claim 1 and "grooves having a substantially same width between said first gate electrodes" of claim 5, the "grooves" must be "between" the floating gate electrodes in the sense that said grooves are in the spaces that separate said floating gate electrodes, where said grooves are substantially on the same plane as said floating gate electrodes. Hence, he finds no inconsistency.

In addition, there is no indication in the Yoshikawa reference when the alleged "substantial flat" or "substantial planar" limitation was determined. The administrative law judge has determined that said limitation should be made as to the polysilicon layer, before any further processing.

Based on the foregoing, the administrative law judge finds that respondents have not established, by clear and convincing evidence, that the '466 publication anticipates asserted independent claims 1 and 5, and dependent claims 2, 3 and 4, each of which depends on claim 1.

d. The Mori 1987 IEDM Article (The 1987 Article)

Respondents argued that complainant's expert Antoniadis admitted that only the "substantially flat" and "substantially planar" limitations of claims 1 and 5, respectively, were not disclosed in the 1987 article (JX-32) (RBr at 219); that respondents' expert Bravman testified that the 1987 article, based in part on his review of a clear copy of the article's figures, anticipates claims 1 and 5 of the '178 patent (RRBr at 117); that because both complainant's expert Antoniadis and Bravman agreed that the copy of at least Figure 7 of the 1987 article in the certified copy of the '178 file history was of poor quality and sought out better reproductions in order to form their opinions about the reference, it is only reasonable to assume that the Examiner may have experienced similar difficulties, making a thorough examination of its disclosure difficult (Id.); and that it is obvious in the clearer copies of Figure 7(a) of the 1987 article that the upper surface of the control gate polysilicon above the grooves does not follow the contours of the grooves between floating gates (Id. at 118).

Complainant argued that the 1987 article was before the Examiner and said article does not anticipate any of the asserted claims of the '178 patent; that respondents' expert Bravman, in

his initial report, did not contend that the '178 patent is anticipated by the 1987 article; that at his deposition, Bravman took the position that the '178 patent is anticipated by the 1987 article based on his review of what he believed were more legible copies of Figure 7 from said article; that it is pure speculation for respondents to assume that the Examiner did not have a legible copy of the photograph in Figure 7; that Bravman admitted that the copy in the certified file history was probably multiple generations of copies removed from what was actually before the Examiner, and he did nothing to investigate the quality of the documents the Examiner had before him; that complainant's expert Antoniadis took the time to visit the Patent Office to review the official file history and he discovered that the version of the 1987 article that is maintained at the Patent Office, including Figure 7, is perfectly clear and legible; and that even in the copies of said article that are not the best quality, it is easy to see in Figure 7(a) that the surface of the polysilicon layer follows the contours of the groove between the floating gates and is neither "substantially flat" nor "substantially planar." (CBr at 201-02.)

The staff argued that the 1987 article discloses a slanted or sloped surface rather than a flat surface; that it is clear from Figure 7(a) of the 1987 article that the surface of the polysilicon is not substantially flat; that the 1987 article was before the Examiner during the prosecution of the '178 patent; and that it is impossible to determine from what is in the record, the quality of the copy that the Examiner actually had. (SBr at 47-48.)

At the outset, the 1987 article was before the Examiner and made of record during the prosecution of the '178 patent. (TFF 1760 (undisputed).)

The title of the 1987 article is "Novel Process and Device Technologies for Submicron 4Mb CMOS EPROMs." (JX-32 at TC-ITC-B 3398.) The 1987 article discloses:

> To obtain high speed operation, polycide gate technology has been developed. In case of EPROM wordline, there are steep steps at the floating gate edges. To prevent the generation of cracks due to stress as such steps during the high temperature heat treatment, floating gate poly-Si thickness should be reduced to around 100nm. When floating poly-Si gate of 200nm thickness is used, cracks can be generated as shown in Fig. 7. Such cracks lead to the increase of wordline resistance.

(JX-32 at TC-ITC-B 3399 (emphasis added).) Thus, a problem with the prior EPROM structure identified by the 1987 article is higher resistance and cracking in the high melting point metal silicide layer of a polycide control gate at the edges of the floating gates. (RPFF 4836 (undisputed).) Also, the 1987 article recognizes and seeks to solve the same problems of increased resistance and cracking in the metal silicide layer of the control gate of an EPROM that the '178 patent describes and seeks to solve. (RPFF 4839 (undisputed).)

At issue is whether the 1987 article discloses the "substantially flat" or the "substantially planar" limitation of claims 1 and 5.[54] As indicated, supra, the administrative law judge has interpreted the claimed phrases "substantially flat" of claim 1 and "substantially planar" of claim 5 to mean a surface which substantially eliminates the topographical features of the underlying structure and thus does not require perfect flatness or anatomic flatness, and that the "substantial flatness" or "substantial planarity" should be determined after the polysilicon layer is deposited but before any subsequent processing.

In support of complainant's argument that the 1987 article does not disclose the "substantially flat" limitation, Antoniadis testified:

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[54] Complainant's expert Antoniadis testified that the only portion of claim 1 of the '178 patent not present in the 1987 article is the "substantially flat" limitation. (RPFF 4852 (undisputed).)

Q. Okay. Does the Mori [1987] IEDM paper address the metal cracking problem?

A. The Mori IEDM, yes, it does address that.

Q. What was the solution in this paper?

A. The solution in this paper was to thin the underlying floating gate polysilicon.

Q. How does that compare to the '178 solution?

A. This is very different from the '178 solution. There is no limitation of the thickness of the poly in the '178 solution. And the groove is completely filled with poly in the '178, with the surface above it being substantially planar.

Q. So what was your conclusion as to whether the Mori 1987 IEDM paper anticipates the claims of the '178 patent?

A. My opinion is it does not anticipate.

Q. Other than what you just testified to, is there anything else that affected your conclusion that it does not anticipate the claims?

A. Well, the fact that it was in front of the examiner supports my conclusion.

Q. Can you explain how you applied your substantially flat claim construction to this reference.

A. Yes. So my definition of substantially flat is that the surface eliminates or substantially attenuates the underlying topography. If you look here carefully in this picture, the underlying topography, which is essentially that of -- is defined by the thickness of the floating gate -- by the way, for clarity I should point out that the floating gate is at the bottom of the oval, kind of the little contrast can be seen both to the left and to the right where the termination of the gap is. So there is a topography there. And it has a certain amplitude. That amplitude is replicated on the interface above, and it's clearly seen despite the additional random --

random texture that the interface possesses.

(Antoniadis, Tr. at 2605-07 (emphasis added).) Hence, the administrative law judge finds that the amplitude of the groove in the 1987 article shown in Figure 7(a) is replicated in the recess in the top of the polysilicon layer, and the upper surface of the polysilicon layer, as disclosed in the 1987 article, does not substantially eliminate the topography of the underlying structure.

In support of respondents' argument that the 1987 article discloses the "substantially flat" limitation, Bravman testified:

> Now if we turn to RDX-552 [a demonstrative slide showing respondents' anticipation argument for the 1987 article], we see a consideration I've given to the latter limitation on claim element 1f, once again, the substantially flat construction requirement. In this slide, once again comparing the before and after, if you will, the S1 and S3 structures in the '178 patent, 1C, and the type of groove structure or -- sorry, polysilicon to silicide interface shown by S2 in the Mori [1987] article. Again, under Toshiba's construction, it's my opinion that both the relatively flat and the substantially -- substantially attenuates limitations or descriptions are met.

(Bravman, Tr. at 2319 (emphasis added).) In contrast to his direct testimony, however, during the cross examination at the hearing, Bravman agreed that the 1987 article shows a topographical feature remaining in the polysilicon layer of the control gate (Bravman, Tr. at 2435). Moreover, there is no evidence what the polysilicon layer of Figure 7 looked like at an intermediate stage of processing. Thus, the administrative law judge in the claim interpretation section determined that the "substantial flatness" should be determined after the polysilicon layer is deposited but before any subsequent processing. Bravman admitted that he would not be able to determine whether a reference anticipates the '178 patent with respect to "substantial flatness" solely by viewing a TEM, photograph, or drawing of the final structure. (Id. at 2434-35.)

Based on the foregoing, the administrative law judge finds that respondents have not established, by clear and convincing evidence, that said 1987 article anticipates asserted independent claims 1 and 5.

2. Obviousness

Respondents argued that claims 1 and 5 are obvious in view of any one of the four allegedly anticipatory references[55] combined with any one of three other references showing substantially flat/planar control gate polysilicon surfaces, i.e., (1) a United States Patent No. 4,616,402 (the '402 patent), issued to Mori on October 14, 1986 (RX-46); (2) a Japanese patent publication S61-216480 (the '480 publication), issued to Mori and published on September 26, 1986 (RX-30); and (3) a 1990 article (the 1990 article), written by Mori and others, and published in the April 1990 edition of IEEE Transactions on Electron Devices (RX-37). (RBr at 223-28.) Respondents further argued that claims 1-5 are obvious in view of any one of said four allegedly anticipatory references combined with any one of three additional references showing substantially flat/planar control gate polysilicon surfaces along with a specific teaching to use a material thickness greater than ½ the width of the grooves in order to produce a flat surface above the groove, i.e., (1) the '480 publication (RX-30); (2) a Japanese patent publication H1-103841 (the '841 publication), issued to Kobayashi and published on April 20, 1989 (RX-25); and (3) a United States Patent No. 4,751,557 (the '557 patent), issued to Sunami on June 14, 1988. (RBr at 228-35.)

Each of complainant and the staff argued that respondents have not established by clear

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[55] As seen, supra, the four references are: the '478 publication (RX-32), the '283 publication (RX-29), the '466 publication (RX-33), and the 1987 article (JX-32).

and convincing evidence that any of the asserted claims of the '178 patent are obvious. (CRBr at 154-59; SBr at 48-49.)

a. The '402 patent with any of the '478 publication, the '283 publication, the '466 publication, and the 1987 article

Respondents argued that claims 1 and 5 are obvious in view of the combination of: the '402 patent (RX-46) (secondary) and the '478 publication (primary), the '402 patent and the '283 publication (primary), the '402 patent and the '466 publication (primary), and the '402 patent and the 1987 article (for claim 5) (primary); that the motivation to combine the '402 patent and the '478 publication arises from the fact that they describe multi-gate semiconductor memories that attempt to solve the same problem in the metal silicide of the control gate polycide structure; that a person of ordinary skill in the art combining the '402 patent and the '478 publication would use the structure described in the '478 publication with respect to Figure 1 except that he or she would change the control gate polysilicon layer so that it's upper surface was planarized above the grooves as described in the '402 patent and shown in Figure 1E in order to eliminate any chances of cracking in the metal silicide layer; and that the reasoning for the motivation to combine the '402 patent and the '283 publication, the '466 publication, or the 1987 article and the way in which it would be carried out by a person of ordinary skill in the art are similar to those for the combination of the '402 patent and the '478 publication. (RBr at 224-25.)

Complainant argued that the '478 publication is in all relevant respects cumulative to the 1987 article (JX-32), which was of record to the prosecution of the '178 patent; that the disclosure of the '402 patent is contained within the '965 publication (JX-22) where the '965 publication was considered in the '178 patent prosecution; that the '283 publication is also

contained within the '965 publication; that respondents failed to explain how the references would be combined and what would be the results of the combinations; that for example, in the combination of the '466 publication with the '402 patent, the teachings of these two references are largely the same; that the primary difference is that the field region 16 in the '466 publication is formed later in the process than the field region 12 in the '402 patent; and that it is not clear how respondents intend these teachings to be combined or what the result would be. (CRBr at 154-55.)

The staff argued that the '402 patent when combined with any of the four "anticipation references" does not render the asserted claims obvious because the '402 patent uses a different process to achieve planarity, for example, an oxide plug. (SBr at 48.)

At the outset, as seen, supra, the administrative law judge found that the asserted claims of the '178 patent are not anticipated by the four primary references, i.e., the '478 publication (RX-32), the '283 publication (RX-29), the '466 publication (RX-33), and the 1987 article (JX-32).

The '402 patent states: "This invention relates to a method of manufacturing a semiconductor device and, in particular, a method of manufacturing a semiconductor device having a stacked-gate-electrode structure." (RX-46 at 1:7-10.) The '402 patent further states: "It is accordingly an object of this invention to provide a method of manufacturing a semiconductor device with a stacked-gate-electrode structure, which can improve critical field strength across gate electrodes and can prevent a breakage in the stepped portion of two or more gate

electrodes." (RX-46 at 1:51-56.) Also, describing Figures 1D and 1E,[56] the '402 patent discloses:

> Then, as shown in FIG. 1D, a thermal oxidation step is carried out with a silicon nitride film pattern 22 as a mask, under the condition that the portion of the first polycrystalline silicon layer 18 within the opening 20 [shown in FIG. 1C] of the silicon nitride film pattern 22 is completely oxidized. As a result, the first polycrystalline silicon layer portion below the opening 20 of the silicon nitride pattern 22 is thermally oxidized to provide a second silicon oxide film 24 and a third silicon oxide film 52 on the silicon nitride film pattern 22. In this way, the whole surface of the silicon substrate 10 is substantially planarized. The remaining unoxidized first polycrystalline silicon layer 18 provides a first polycrystalline silicon layer pattern 26 as a floating gate with its end 28 smoothly formed.
>
> As shown in FIG. 1E, a second polycrystalline silicon layer is deposited on the whole surface of the resultant structure and, after being subjected to a patterning step, provides a control gate 38.

(RX-46 at 3:10-27 (emphasis added).) Thus, as shown in Figures 1D and 1E of the '402 patent, "the portion of the first polycrystalline silicon layer 18 within the opening 20 [shown in FIG. 1C] of the silicon nitride film pattern 22 is completely oxidized," with the result that "the first polycrystalline silicon layer portion below the opening 20 of the silicon nitride pattern 22 is thermally oxidized to provide a second silicon oxide film 24." The '402 patent teaches a different process to achieve substantial flatness or substantial planarity than does the '178 patent. Thus, it uses "oxide fillers" or "plugs" to provide substantial planarity (shown as "second silicon oxide film 24" in Figures 1D and 1E of the '402 patent), rather than using a polysilicon layer to achieve substantial planarity (as required by claims 1 and 5 of the '178 patent in issue). As complainant's expert Antoniadis testified:

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[56] The '402 patent states: "FIGS. 1A to 1E are cross-sectional views for explaining a method of manufacturing a semiconductor device according to a first embodiment of this invention." (RX-46 at 2:32-34.)

Q. And what was your general reaction to his [Bravman's] conclusions on obviousness?

A. I disagree obviously that this patent is obvious. We have -- what this patent does is it changes completely the mind-set of the community quite clearly. There is, on one hand, the approach which has to do with the thinning of the poly. On the other hand, we have the approach that's associated with the filling of the groove with a dielectric or an oxide in order to planarize that. For all the very important reasons that were in place for manufacturing of EPROMs at the time of the invention and even after that, it would not have been obvious for people to thicken the poly to the degree that the ['178] patent suggests. And what the patent did is essentially it created -- it decoupled the thickness of the underlying poly from problems of planarity. It allowed for significantly more flexibility for the design of the coupling factor between -- the coupling ratio as it's called, between the control gate and the underlying gate. It was a brilliant idea. And nobody had thought about it earlier. And, actually, it's the only way by which memories of this kind are made today. So it stood the test of time.

Q. Can you pull up RDX-566 [a slide showing respondents' obviousness argument for the "substantially flat" and "substantially planar" limitations for RX-46 (the '402 patent), RX-30 (the '480 publication) and RX-37 (the 1990 article)]. Let's look at some of the specific combinations that Professor Bravman identified. What are the three references that are listed as references to be combined with the [section] 102 references?

A. So these are all references that use a silicon dioxide plug or filler to provide planarity. And, yes, that's what they are.

Q. What is the significance of that in your mind?

A. I'm not sure about your question.

Q. Do any of these references use polysilicon to fill the groove?

A. None of those is using polysilicon to fill the groove. These

> are all publications that use oxide fillers, the same as the publication that was in the face -- the publications, actually, that are in the face of the patent.

(Antoniadis, Tr. at 2626:6-2628:13 (emphasis added).)

As indicated, supra., motivation is critical to establish obviousness. Here, contrary to what is shown in the '178 patent, the '402 patent teaches "oxide fillers" or "plugs" to provide substantial planarity or substantial flatness.

Based on the foregoing, the administrative law judge finds that respondents have not established, by clear and convincing evidence, that the asserted independent claims 1 and 5 are obvious in view of the combination of 'the '402 patent with any of the '478 publication, the '283 publication, the '466 publication, and the 1987 article.

b. The '480 publication with any of the '478 publication, the '283 publication, the '466 publication, and the 1987 article

Respondents argued that claims 1 through 5 are obvious in view of the combination of: the '480 publication (RX-30) (secondary) and the '478 publication (primary), the '480 publication and the '283 publication (primary), the '480 publication and the '466 publication (primary), and the '480 publication and the 1987 article (for claim 5) (primary); that the motivation to combine the '480 publication and the '478 publication arises from the fact that they describe multi-gate semiconductor memories that attempt to solve the same problem in the metal silicide of the control gate polycide structure; that a person of ordinary skill in the art combining the '480 publication and the '478 publication would use the structure described in '478 with respect to Figure 1 except that he or she would change the control gate polysilicon layer so that it's upper surface was flattened above the grooves as described in the '480 publication and shown

in Figure 1(f) in order to eliminate any chances of cracking in the metal silicide layer; and that the reasoning for the motivation to combine the '480 publication and the '283 publication, '466 publication, or 1987 article and the way in which it would be carried out by a person of ordinary skill in the art are similar to those for the combination of the '480 publication and the '478 publication. (RBr at 226.)

Complainant argued that the relevant subject matter of the '480 publication (RX-30) was before the Patent Office in the form of the '567 publication (JX-24); the subject matter of the '478 publication (RX-32) is in all relevant respects the same as the subject matter of the 1987 article (JX-32) that is on the face of the '178 patent; that the relevant subject matter of the '283 publication (RX-29) was before the Patent Office in the prosecution of the '178 patent; that the teachings of the combination of the '466 publication (RX-33) with the '480 publication (RX-30) provide incompatible ways of forming oxide plugs; and that it is not clear how respondents intend said teachings to be combined or what the result would be. (CRBr at 155-57.)

The staff argued that the '480 publication when combined with any of the four "anticipation references" does not render the asserted claims obvious because the '480 publication uses a process to achieve planarity different from what is disclosed in the '178 patent in issue. (SBr at 48.)

At the outset, as seen, supra, the administrative law judge has found that the asserted claims of the '178 patent are not anticipated by the four primary references, i.e., the '478 publication (RX-32), the '283 publication (RX-29), the '466 publication (RX-33), and the 1987 article (JX-32).

The '480 publication states: "The present invention relates to a method of manufacturing

a non-volatile semiconductor memory device, in particular, to a method of manufacturing a non-volatile semiconductor memory device such as EPROM, E2PROM, or the like, having a floating gate." (RX-30 at HY93617.) The '480 publication further discloses:

> However, since in the method described above the floating gates 6 are formed by patterning after coating the entire surface with the first polycrystalline silicon layer 5, recesses 9 are formed between the floating gates 6. ... [A]s has been mentioned above, the control gate 8 is made from polycrystalline silicon, but recently, and in order to accelerate operation of the elements, polycrystalline silicon layers are often replaced by high-melting-point metal layers or high-melting point metal silicide layers. However, when high-melting-point layers are used during heat treatment, they are subject to breakage by aforementioned step-like recesses between the floating gates.

(Id. (emphasis added).) Referring to Figures 1(e) and 1(f),[57] the '480 publication states:

> The entire unit is subjected to annealing in an N_2 atmosphere at 900°C; the CVD-SiO_2 film 29 [shown in Figure 1(d)] is etched-back, the thin oxide film that exists on the second polycrystalline silicon layer 27 is removed, and portions of SiO_2 designated by references 30_1 and 30_2 inside the grooves 28_1 and 28_2 are flattened, as shown in Fig. 1(e).
>
> * * *
>
> As a result, the following elements are formed one after another: the gate oxide film 31 which is the first in the direction from the surface of the substrate 21; the floating gate 32 which is made from the first polycrystalline silicon; the second gate oxide film 33; and the control gate 36 that has a three layer structure formed by the second polycrystalline silicon layer 27, the third polycrystalline silicon layer 34, and the molybdenum silicide layer 35.

(Id. at HY93619 (emphasis added).) Thus, as shown in Figures 1(e) and 1(f) of the '480

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[57] The '480 publication states: "Figs. 1(a) to 1(f) are cross-sectional views that illustrate sequential steps of manufacturing an EPROM-memory cell by the method of the present invention." (RX-30 at HY93620.)

publication, "portions of SiO_2 designated by references 30_1 and 30_2 inside the grooves 28_1 and 28_2 are flattened." Referring to the '480 publication, complainant's expert Antoniadis explained, as seen in section IX.B.2.a, (see supra, Tr. at 2626:6-2628:13) that said '480 publication discloses using "oxide fillers" or "plugs" to provide planarity. Hence, the administrative law judge finds that the '480 publication teaches the use of "oxide fillers" or "plugs" to provide substantial planarity (shown as "portions of SiO_2 designated by references 30_1 and 30_2" in Figures 1(e) and 1(f) of the '480 publication), rather than using a polysilicon layer to achieve substantial planarity (as required by claims 1 and 5 of the '178 patent in issue).

Based on the foregoing and the administrative law judge's findings with respect to non-obviousness of the combination of the '402 patent with any of the '478 publication, the '283 publication, the '466 publication, and the 1987 article, supra, the administrative law judge finds that respondents have not established, by clear and convincing evidence, that the asserted independent claims 1 through 5 are obvious in view of the combination of 'the '480 publication with any of the '478 publication, the '283 publication, the '466 publication, and the 1987 article.

c. The 1990 article with any of the '478 publication, the '283 publication, the '466 publication, and the 1987 article

Respondents argued that claims 1 and 5 are obvious in view of the combination of: the 1990 article (RX-37) (secondary) and the '478 publication (primary), the 1990 article and the '283 publication (primary), the 1990 article and the '466 publication (primary), and the 1990 article and the 1987 article (for claim 5) (primary); that the motivation to combine the 1990 article and the '478 publication arises from the fact that they describe multi-gate semiconductor memories that attempt to solve the same problem in the metal silicide of the control gate polycide

structure; that a person of ordinary skill in the art combining the 1990 article and the '478 publication would use the structure described in '478 with respect to Figure 1 except that he or she would change the control gate polysilicon layer so that it's upper surface was flattened above the grooves as described in the 1990 article and shown in Figure 1 in order to eliminate any chances of cracking in the metal silicide layer; and that the reasoning for the motivation to combine the 1990 article and the '283 publication, '466 publication, or 1987 article and the way in which it would be carried out by a person of ordinary skill in the art are similar to those for the combination of the 1990 article and the '478 publication. (RBr at 227-28.)

Complainant argued that the 1990 article describes an entirely unusual EPROM cell that is incompatible with the EPROM cells of the '478 publication (RX-32), the '283 publication (RX-29), the '466 publication (RX-33), and the 1987 article (JX-32); that respondents offer no explanation for how these incompatible disclosures would be combined; that respondents assert that the 1990 article was published in April 1990; that respondents concede that the priority date of the '178 patent is April 24, 1990; and that with no proof of a more precise publication date, respondents failed to prove that the 1990 article is prior art. (CRBr at 157-58.)

The staff argued that the 1990 article when combined with any of the four "anticipation references" does not render the asserted claims obvious because the 1990 article uses a different process to achieve planarity, for example, an oxide plug. (SBr at 48.)

At the outset, the administrative law judge finds that respondents have not met their burden in establishing that the 1990 article is prior art by clear and convincing evidence. Respondents agreed that the priority date of the '178 patent is April 24, 1990. (RBr at 227; JX-1.) However, respondents also argued that the 1990 article was "published in the April 1990 edition

of IEEE Transactions on Electron Devices," with no further details as to the exact date of publication. (RBr at 227.)

Assuming arguendo that the 1990 article is prior art, as indicated, supra, the administrative law judge found that the asserted claims of the '178 patent are not anticipated by the four primary references, i.e., the '478 publication (RX-32), the '283 publication (RX-29), the '466 publication (RX-33), and the 1987 article. (JX-32).

The 1990 article states: "In order to realize ultra-high-density EPROM's, such as 16 Mb or beyond, technology innovations both cell structure and cell array architecture, will be required for high performance without increasing the die size." (RX-37 at HY88248.) The 1990 article also states: "A novel BPSG [boro-phospho-silicate glass] planarization process was developed to prevent interpoly insulator degradation and planarized surface morphology to reduce metallization failures."[58] (Id. at HY88249 (emphasis added).) The 1990 article further discloses:

> After formation of the active area and gate oxide, the poly 2/oxide-nitride-oxide (ONO)/poly 1 stacked layer is defined to form floating gates and part of the control gates in a self-aligned manner. ... After activation for cell junctions, the BPSG layer was deposited and thermally flowed to fill the cell-to-cell polycide word-line spacing. Thus the surface was planarized by the RIE [reactive ion etching] process with individual poly 2 surfaces exposed at this step. After that, the polycide word line connecting the poly 2's was formed, which runs perpendicular to the bit lines. ... Almost flat planarized surface morphology has been achieved. Therefore it is possible to improve the manufacturability of polycide word lines and reduce the metallization-induced failures.

(Id. (emphasis added).) Hence, as disclosed above and shown in Figure 1 of the 1990 article, the

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[58] BPSG is defined as: "boro-phospho-silicate glass; silicon dioxide (silica) with boron and phosphorus added to lower temperature at which glass (oxide) starts to flow from about 950 oC for pure SiO2 to about 500 oC for BPSG; used to planarize the surface; deposited by CVD. (Source: http://semiconductorglossary.com.)

"the BPSG layer," i.e., the oxide layer, "was deposited and thermally flowed to fill the cell-to-cell polycide word-line spacing," achieving surface planarization. The administrative law judge finds that the 1990 article teaches the use of "oxide fillers" or "plugs" to provide substantial planarity (described as the BPSG layer filling the polycide word-line spacing), rather than using a polysilicon layer to achieve substantial planarity (as required by claims 1 and 5 of the '178 patent in issue). Thus, referring to the 1990 article, complainant's expert Antoniadis testified, (see supra, Tr. at 2626:6 - 2628:13) that said 1990 article discloses using "oxide fillers" or "plugs" to provide planarity.

Based on the foregoing and the administrative law judge's findings with respect to non-obviousness of the combination of the '402 patent with any of the '478 publication, the '283 publication, the '466 publication, and the 1987 article, supra, the administrative law judge finds that respondents have not established, by clear and convincing evidence, that the asserted independent claims 1 and 5 are obvious in view of the combination of the 1990 article with any of the '478 publication, the '283 publication, the '466 publication, and the 1987 article.

d. The '841 publication with any of the '478 publication, the '283 publication, the '466 publication, and the 1987 article

Respondents argued that claims 1 through 5 are obvious in view of the combination of: the '841 publication (RX-25) (secondary) and the '478 publication (primary), the '841 publication and the '283 publication (primary), the '841 publication and the '466 publication (primary), and the '841 publication and the 1987 article (for claim 5) (primary); that the motivation to combine the '841 publication and the '478 publication arises from the fact that the '841 publication describes a way to further flatten the control gate polysilicon in the '478

structure in accordance with the teaching of the '478 that such flattening is beneficial for solving the cracking in the control gate polysilicon layer; that a person of ordinary skill in the art combining the '841 publication and the '478 publication would use the structure described in the '478 publication with respect to Figure 1 except that he or she would change the control gate polysilicon layer so that it's thickness was greater than ½ the width of the grooves, resulting in upper control gate polysilicon surface that is flat above the grooves as described in the '841 publication and shown in Figures 1(b) and 3(b); and that the reasoning for the motivation to combine the '841 publication and the '283 publication, '466 publication, or 1987 article and the way in which it would be carried out by a person of ordinary skill in the art are similar to those for the combination of the '841 publication and the '478 publication. (RBr at 231-33.)

Complainant argued that the '841 publication is about the top plate of a DRAM (Dynamic Random Access Memory) trench capacitor; that the '841 publication states that filling a trench by depositing a thick layer of polysilicon is unreliable and that it is necessary to deposit a second material, polyvinyl alcohol, to achieve reliable planarization after depositing a thick layer of polysilicon and thus the '841 publication teaches away from trying to fill openings only with polysilicon and thus teaches away from any combination with an EPROM reference; that the '841 publication does not suggest changing the silicon oxide or floating gate thinning planarization strategies of the primary references cited by respondents; that thus the '841 publication does not teach one to form an insulating film that defines grooves and does not teach filling those grooves with a thick polysilicon layer; and that none of the asserted claims of the '178 patent would have been obvious over such a combination. (CRBr at 158.)

At the outset, as seen, supra, the administrative law judge found that the asserted claims

of the '178 patent are not anticipated by the four primary references, i.e., the '478 publication (RX-32), the '283 publication (RX-29), the '466 publication (RX-33), and the 1987 article (JX-32).

The '841 publication states: "This invention is related to a manufacturing method for a semiconductor device, wherein the polysilicon, which is accumulated in order to fill in the holes and grooves that are created on the polysilicon, and in particular the silicon substrate, that is one formative film of the semiconductor device, is flattened." (RX-25 at HY93547.) The '841 publication also states:

> In conjunction with the demands of the high integration of semiconductor integrated circuits, for example, with dynamic random access memory ("DRAM"), in order to attain the necessary cell capacity with a small cell area, a cell structure that would also utilized surfaces vertical to the substrate by digging holes in the silicon substrate, for example, trench capacitors, have been considered.

(Id.) Describing the problems that the invention is to solve, the '841 publication further discloses:

> However, in this case, as indicated in Figure 3(b), the CVD-polysilicon 3 to be filled and flattened creates a small indentation 5 in the center of the filling. In addition, because the center 4 of the CVD-polysilicon 3 filling becomes the seam of the film, the etch rate during etching is fast. Therefore, as shown in Figure 3(c), the problem occurs that a step difference 6 from the stopper oxidized film 2 occurs after etching. ... This invention provides a manufacturing method for semiconductor devices that solves the following problems in the aforementioned conventional techniques: the problem that step differences created during flattening using polysilicon fillers of trench holes and grooves and the like, subsequently causes defects such as step disconnections and incomplete etching during wiring layer formation; and the problem that using flattening materials to flatten the step difference causes the time required for etching to be long, and also makes

uniform etching difficult.

(Id. at HY93548-49 (emphasis added).) Describing the means for solving the above problems, the '841 publication also discloses:

> In this invention, in order to solve the aforementioned problems, the grooves are filled with polysilicon with film thickness that is ½ or more of the groove opening width, a PVA [polyvinyl alcohol] layer is formed on the entire surface of the polysilicon layer so that the surface is flattened, and subsequently the entire surface is plasma etched.

(Id. (emphasis added).) Thus, it is clear that the invention of the '841 publication provides a solution to the "defects" that "step differences created during flattening using polysilicon fillers" causes, "such as step disconnections and incomplete etching." That solution is to form a "PVA layer" "on the entire surface of the polysilicon layer so that the surface is flattened."

In support of complainant's non-obviousness argument, complainant's expert Antoniadis testified:

> Q. Okay. And then you were about to start discussing the DRAM references. Could you discuss the '841 Kobayashi publication?
>
> A. Yes. The '841 Kobayashi publication dealing with the planarization of a DRAM capacitor, as I said earlier. It's, the DRAM capacitor is a very different structure than anything we've discussed here for the groove in our memory devices. The capacitor is actually a deep trench into the silicon. That trench is -- has an aspect ratio which is significantly different. It's almost one micron deeper than the groove that is at issue here. And the specific Kobayashi application publication talks about or is concerned, as it was pointing out, with the planarization and the application of an additional sacrificial layer, PVA layer for the application of subsequent etching to provide the planar surface. So it's a rather complicated process which is associated with an element that is very different

from the elements that we're talking about here.

Q. What's the significance of the PVA that you mentioned?

A. The significance of the PVA is that, as that paper discusses, even with a filling of the trench of the capacitor which is following this one-half width of the groove with poly, still the surface is not quite planar and requires this application of a PVA. And this is the point, actually, of that publication.

(Antoniadis, Tr. at 2630-31 (emphasis added).) Thus, consistent with the disclosure of the '841 publication, supra, Antoniadis explained that said '841 publication discloses that even after filling the trench of the capacitor with the polysilicon, the polysilicon surface still requires the PVA layer to achieve planarity. Moreover, Antoniadis explained that EPROMs are very different from DRAMs, providing a specific example. The administrative law judge finds no evidence to the contrary.

Hence, the administrative law judge finds that the '841 publication teaches that using polysilicon fillers actually causes defects such as step disconnections, and thus a PVA layer is required to be formed on the polysilicon to achieve flatness, rather than using a polysilicon layer to achieve substantial flatness or substantial planarity (as required by claims 1 and 5 of the '178 patent in issue). Hence, assuming arguendo that there exists a motivation to combine the '841 publication with the primary references, the combination would not result in the claimed invention in issue.

Based on the foregoing, the administrative law judge finds that respondents have not established, by clear and convincing evidence, that the asserted claims 1-5 are obvious in view of the combination of the '841 publication with any of the '478 publication, the '283 publication,

the '466 publication, and the 1987 article.

e. The '557 patent with any of the '478 publication, the '283 publication, the '466 publication, and the 1987 article

Respondents argued that claims 1 through 5 are obvious in view of the combination of: the '557 patent (RX-47) (secondary) and the '478 publication (primary), the '557 patent and the '283 publication (primary), the '557 patent and the '466 publication (primary), and the '557 patent and the 1987 article (for claim 5) (primary); that the motivation to combine the '557 patent and the '478 publication arises from the fact that the '557 patent describes a way to further flatten the control gate polysilicon in the '478 structure in accordance with the teaching of the '478 that such flattening is beneficial for solving the cracking in the control gate polysilicon layer and the similar teaching of the '557 that such flattening is beneficial for avoiding processing problems with a silicide or metal layer deposited above an unfilled recess; that a person of ordinary skill in the art combining the '557 patent and the '478 publication would use the structure described in '478 with respect to Figure 1 except that he or she would change the control gate polysilicon layer so that it's thickness was greater than ½ the width of the grooves, resulting in an upper control gate polysilicon surface that is flat above the grooves as described in the '557 patent; and that the reasoning for the motivation to combine the '557 patent and the '283 publication, '466 publication, or 1987 article and the way in which it would be carried out by a person of ordinary skill in the art are similar to those for the combination of the '841 publication and the '478 publication. (RBr at 233-35.)

Complainant argued that the '557 patent does not suggest changing the silicon oxide or floating gate thinning planarization strategies of the four primary references cited by respondents

and does not teach one to form an insulating film that defines grooves and does not teach filling those grooves with a thick polysilicon layer; that respondents provide no explanation as to why one of ordinary skill in the art would use the trench capacitor upper plate of the '557 patent for any purpose in a floating gate transistor, nor an explanation of how any of the combinations would be made or why they would produce operable devices; and that the asserted claims of the '178 patent would not have been obvious over any proposed combination of an EPROM reference with the '557 patent. (CRBr at 158-59.)

At the outset, as indicated, supra, the administrative law judge found that the asserted claims of the '178 patent are not anticipated by the four primary references, i.e., the '478 publication (RX-32), the '283 publication (RX-29), the '466 publication (RX-33), and the 1987 article (JX-32).

The title of the '557 patent is "DRAM with FET [field effect transistor] stacked over capacitor." (RX-47 (emphasis added).) The Abstract of the '557 patent states: "A semiconductor memory wherein a part of each capacitor is formed on side walls of an island region surrounded with a recess formed in a semiconductor substrate, and the island region and other regions are electrically isolated by the recess." (Id. (emphasis added).) The '557 patent also states: "The present invention relates to semiconductor memories, and more particularly to a semiconductor memory which permits a remarkable increase in the capacitance of a storage capacitor portion without the necessity of increasing a plane area." (Id. at 1:9-13 (emphasis added).) The SUMMARY OF THE INVENTION section of the '557 patent discloses:

> An object of the present invention is to solve the problems of the prior art arrangements, and to provide a semiconductor memory well-suited to an integrated circuit which requires a very small area

and which has an extraordinarily high density of integration.

Another object of the present invention is to provide a semiconductor memory having capacitors and isolation regions the required areas of which are very small.

In order to accomplish the objects, according to the present invention, the side walls of an island region enclosed with a recess are utilized as a part of a capacitor, and the recess is used for the electrical isolation between the island region and another region as well.

(Id. at 2:31-45 (emphasis added).) Hence, the above disclosure shows that the '557 patent is directed to a semiconductor memory which includes capacitors, i.e., DRAMs.

Describing Figures 12-15, the '557 patent states:

The width of the etched recess 17 is W_M. Therefore, when $W_M > 2 T_{S1}$ holds where T_{S1} denotes the thickness of the polycrystalline Si film 8, a recess 80 as shown in FIG. 12 is left unfilled, so that the top surface of the device does not become flat. Since the recess 80 adversely affects the processing and the deposited states of the insulating film and the word line 4 to be deposited thereon, it should better be filled to flatten the surface. In the present embodiment, polycrystalline Si is deposited on the whole surface to a thickness T_{S2}, whereupon the whole area of the deposited polycrystalline Si is removed by the thickness T_{S2} from above by the well-known plasma etching which employs CF_4 or SF_6 gas. Then, as shown in FIG. 12, the polycrystalline Si 81 remains in the form in which it is just buried in the recess 80, and the upper surface becomes flat. In a case where the polycrystalline Si film 8 is thickened thereby to fill up the recess, the second deposition of the polycrystalline Si is not necessary. Since, however, the plate 8 is also used as an interconnection part, a suitable thickness is 100-500 nm or so. When the recess is not filled up with the plate of such thickness, the polycrystalline Si 81 is deposited as described above, to entirely fill the recess and to flatten surface.

When the polycrystalline Si film 8 left intact is overlaid with the second polycrystalline Si 81 which is thereafter etched over the entire area, the end point of the etching becomes indefinite because both fuse into one at their boundary. Therefore, the surface of the

first layer of polycrystalline Si 8 is thermally oxidized by 5-30 nm so as to interpose an SiO_2 layer between both the layers. Thus, the SiO_2 film on the first layer of polycrystalline Si 8 is exposed in the state in which the second layer of polycrystalline Si has been etched over the entire area. Herein, the plasma etching rate of polycrystalline Si is 10 or more times as high as that of SiO_2. Therefore, even when overetching is somewhat performed, the first layer of polycrystalline Si 8 is protected by the SiO_2 and is not etched.

Next, the unnecessary part of the polycrystalline silicon film 8 is removed by the photoetching process so as to finish up the plate 8. Thereafter, as shown in FIG. 13, the surface of the plate 8 is oxidized to form the first inter-layer oxide film 13 which is 100-400 nm thick. At this time, the Si_3N_4 film 19 is scarcely oxidized. Thereafter, using the first inter-layer oxide film 13 as a mask, the exposed part of the Si_3N_4 film 19 and the underlying SiO_2 film 18 are removed by etching. The exposed surface of the resultant Si substrate 100 is oxidized in an oxidizing atmosphere of dry oxygen at 800°-1150° C. containing 1-5% of HCl, whereby the gate oxide film 12 being 10-50 nm thick is formed. Thereafter, a predetermined dose of boron is ion-implanted in order to attain a desired threshold voltage V_{TH}. Subsequently, as shown in FIG. 14, the gates (word lines) 4 each of which is made of a single layer of polycrystalline Si, silicide (e.g., Mo_2Si) or the like or stacked films thereof; a refractory metal such as W and Mo; or the like are selectively deposited on predetermined parts.

Thereafter, when As or phosphorus is ion-implanted by approximately $5X10^{15}$-$2X10^{16}/cm^2$ at an acceleration voltage of 60-120 keV, the n+ -type source and drain layers 15 are formed in the parts on which neither the plate 8 nor the gate 4 is deposited, as shown in FIG. 15. Further, the second inter-layer insulating film 14 which is represented by a CVD SiO_2 film containing 4-10 mol-% of phosphorous (abbreviated to CVD.PSG) is deposited to a thickness of 300-1000 nm, and it is heat-treated at 900°-1000° C. so as to be densified. Thereafter, the electrode connection holes 9 which reach the n+ layers 15, gates 4 and plates 8 of the substrate are formed, and the electrodes 3 which are made of a material represented by Al or an Al alloy are selectively deposited. Thus, the 1-transistor type dynamic memory cell is constructed which uses the side wall of the etched recess 17 as a part of the capacitor.

(Id. at 7:5-8:12 (emphasis added).) Thus, as disclosed above and shown in Figure 13, "the surface of the plate 8 [which respondents argued is the same as the polysilicon layer of the '178 patent (RPFF 5248)] is oxidized to form the first inter-layer oxide film 13"; thereafter, as disclosed above and shown in Figure 15, a "second inter-layer insulating film 14 which is represented by a CVD SiO_2 film" is deposited on the first inter-layer oxide film 13; and thereafter, as disclosed above and shown in Figure 15, "the electrodes 3 which are made of a material represented by Al or an Al alloy are selectively deposited," at which point, a "1-transistor type dynamic memory cell is constructed which uses the side wall of the etched recess 17 as a part of the capacitor." Hence, the administrative law judge finds that in the '557 patent, a "metal layer or a silicide layer" is not "formed on the polysilicon layer" where the surfaces of those portions of said polysilicon layer above the grooves are substantially flat (as required by the asserted claims of the '178 patent). Rather, as disclosed supra, and shown in Figure 14, the parts which are made of metal or silicide are actually "the gates (word lines) 4," which are "selectively deposited on predetermined parts [i.e., 'the gate oxide film 12,' and not 'plate 8']."

Significantly, in support of complainant's non-obviousness argument, complainant's expert Antoniadis testified:

> Q. What about the Sunami reference [the '557 patent]?
>
> A. The Sunami paper is another transcapacitor filling paper. And in this case this one is concerned with the void that may form in filling with a single layer of poly, and discusses the application of double poly deposition in order to fill and then subsequently back etch to achieve planarity.
>
> Q. At the bottom of this slide [RDX-570], Professor Bravman

has identified certain motivations to combine. Can you address your conclusion as to whether those -- there would be motivation to combine these references with the 102 references Professor Bravman has relied upon?

A. Well, my opinion is that these are not good motivations. If we take the first one, multigate semiconductor devices, the devices that we're talking about here for the memory structures in our case, the EPROMs, and the DRAM are very different. DRAMs are -- have transistors that are single gate, for example. Second, there is the issue of cracking, and disconnection is a problem that was identified with the particular structure of the EPROM and the stress associated with a silicide there, and not necessarily found in the DRAM case....

(Antoniadis, Tr. at 2631-32 (emphasis added).) Thus, Antoniadis explained that the '557 patent concerns an application of a double polysilicon deposition in order to fill the void that may form in filling with a single layer of polysilicon. Moreover, Antoniadis testified that EPROMs are very different from DRAMs. The '178 patent is directed to EPROMs, not to DRAMs.

Based on the foregoing, the administrative law judge finds that respondents have not established, by clear and convincing evidence, that the asserted claims 1 through 5 are obvious in view of the combination of the '557 patent with any of the '478 publication, the '283 publication, the '466 publication, and the 1987 article.

X. Validity ('449 Patent - Double Patenting)

Respondents argued that the '449 patent claims priority through a chain of continuation applications which include U.S. Patent No. 5,148,394 (the '394 patent); and that their expert Pashley provided a detailed analysis of his conclusion that one of ordinary skill in the art would find asserted claims 1 and 4 of the '449 patent identical to, or obvious variations of, claims 19 and 20, respectively, of the '394 patent. Hence, it was argued that claims 1 and 4 of the '449

patent are invalid based on double patenting. (RBr at 200.)

Complainant argued that while Pashley sought to justify his over-reliance on the specification of the '449 patent by pointing out that some of the elements of the claims under consideration were written in Section 112 ¶ 6 means-plus-function format, he never accounted for the fact that some of the limitations were not in that format, nor did he conduct a proper analysis to determine the recited function of each means-plus-function term; that structural limitations from embodiments in said specification can be read into patent claims only to the extent they actually perform the functions expressly recited in the claims; and that because Pashley failed to identify the recited functions of the means-plus-function elements under comparison and to focus his analysis of structure disclosed in the specification, his observations regarding those structures are flawed. (CBr at 196-7.)

The staff argued that respondents have not met their heavy burden of proving, by clear and convincing evidence, that claims 1 and 4 of the '449 patent are invalid based on non-statutory obviousness-type double-patenting over claims 19 and 20 of the '394 patent. In support, the staff argued that all of the asserted claims of the '449 and the '394 patents are directed to a semiconductor memory device with a "data programming means," a "row selection means," and a "first and second switching means;" that the asserted claims of the '449 patent recite additional functions of the "row selection means" and "second switching means;" that the "second switching means" of claim 19 of the '394 patent is limited to "selecting the cell transistor;" that the '449 patent recites "whether or not the signal from the row selection means should be applied to the cell transistor;" that the term "selection" in the '394 patent is broader than "activating a cell" in the context of the '449 patent; and that while respondents' construction

equates "designating" with "activating" in association with the row selection means under the staff's claim construction and Toshiba's construction, designating and selecting are broader than activating because they do not require a signal to be applied to the cell transistor. Thus, the staff argued that the limitations of the '449 patent are narrower and significantly different than simply selecting a row. (SBr at 56-57.)

The affirmative defense of double patenting requires respondents to prove double patenting by clear and convincing evidence. RCA Corp. v. Applied Digital Data Sys., Inc., 730 F.2d 1440, 1444 (Fed. Cir. 1984) (invalidity requires clear and convincing proof, and the burden remains at all times with the patent challenger); Carman Indus., Inc. v. Wahl, 724 F.2d 932, 940, 220 USPQ 481, 487 (Fed. Cir. 1983) ("[t]here is a heavy burden of proof on one seeking to show double patenting"). There are two type of double patenting. Thus statutory double patenting is found when the same invention is being claimed twice. Obviousness-type double patenting is found when any claim in an application defines merely an obvious variation of an invention claimed in the patent asserted as supporting double patenting. General Foods Corp. v. Studiengesellschaft Kohle mbH, 972 F.2d 1272, 1278 (Fed. Cir. 1992).

At the pre-hearing conference, respondents made reference to a terminal disclaimer recently filed with the Patent Office and argued that it is "certainly substantial evidence of a concession by Toshiba that in fact the '449 patent is invalid for double patenting." (Tr. at 62.) Complainant admitted that a request for a terminal disclaimer was filed with the Patent Office on July 3, 2006, but argued that a terminal disclaimer is not a concession of double patenting. (Tr. at 72.) Moreover, complainant argued that it expects to go forward, as stated in its pre-hearing statement, and demonstrate that there is no double patenting and that if the terminal disclaimer is

granted, the law is that there is no double patenting defense under the statute. (Tr. at 72-3.) Respondents thereafter argued that if in the future, complainant wants to raise the issue of the terminal disclaimer, respondents "request this document to be out of the case." (Tr. at 78.) The administrative law judge ruled that any such request is premature since no terminal disclaimer has been offered into evidence. (Tr. at 78.)

On September 26, 2006, complainant sent a letter to the administrative law judge arguing that the Hynix respondents' double-patenting defense is moot because of a terminal disclaimer that was granted by the Patent Office. On that same day, Order No. 22 treated said letter as a summary determination motion and ordered that respondents and the staff respond to the motion.

In a response filed September 29, respondents opposed the motion for summary termination. The staff, in a response, also filed on September 29, supported said motion. Complainant, by letter dated October 4, 2006, to the administrative law judge, responded to respondents' letter of September 29.

It is a fact that on September 12, 2006, a terminal disclaimer was granted by the Patent Office limiting the term the '449 patent to the extent of the term of the '394 patent (Motion at 1). A terminal disclaimer moots an obviousness-type double patenting defense. Certain Dynamic Random Access Memories, Components Thereof, and Products Containing Same, Inv. No. 337-TA-242, Initial Determination (June 8, 1987) at 459-60 (DRAMs).

In DRAMs, complainant filed terminal disclaimers after the evidentiary hearing had commenced but before evidence relating to the patents at issue was heard. Id. at 460. Respondents in DRAMs, asserted that the terminal disclaimers were untimely filed and should not be given effect. Id. However, the ID determined that the filing of terminal disclaimers after an

infringement suit has commenced is "accepted practice" and that the disclaimers were effective. Id.

Respondents argued that Commission rule 210.18(a) precludes post-trial summary judgment motions filed by a party. Complainant however did not file any summary determination motion. Rather, it was the administrative law judge, in view of the nature of complainant's letter of September 26, 2006, who treated said letter as a motion for summary determination. Moreover, the administrative law judge could have treated the letter as a motion to strike, which if granted would have had the same effect as granting the motion for summary determination. The purpose of Order No. 22 was to provide the opportunity for respondents and the staff to respond to the substance of the September 26 letter. Hence, respondents' argument that the letter was untimely is rejected.

Regarding the substance of complainant's letter of September 26, 2006, respondents argued that the administrative law judge should deny Toshiba's request that its disclaimer be given effect in this investigation, i.e., retroactivity; that first, under Southwest Software, Inc. v. Harlequin Inc., 226 F.3d 1280, 1292-95 (Fed. Cir. 200), he should rule that Toshiba's terminal disclaimer has no effect in this investigation because it was requested and issued after Toshiba filed its complaint, after discovery closed, and after trial; and that second, Toshiba's post-hearing and post-discovery request should be given no retroactive effect because it unfairly prejudices Hynix and the public.

Southwest however did not involve a terminal disclaimer. While respondents argued that Perricone v. Medicis Pharm. Corp., 432 F.3d 1368 (Fed. Cir. 2005), relied on by complainant in its September 26 letter, made no decision on whether a terminal disclaimer could receive

retroactive effect, it is a fact that Dr. Perricone had not filed any terminal disclaimer as the Court indicated. Hence, the terminal disclaimer was not before the Court.

It is also a fact that the term of the '449 patent, subsequent to the expiration of the '394 patent, has been disclaimed through the Patent Office's decision to grant the terminal disclaimer published in the Official Gazette, dated September 12, 2006 (Exh. B to the September 26, letter). Respondents do not deny that the Patent Office action moots any obviousness-type double patenting defense at least on September 12, 2006, and thereafter. Moreover the granting of the motion in issue will at least relieve this administrative law judge and possibly the Commission and the Federal Circuit from expanding resources in determinating the merits of the substantive arguments set forth supra. Hence, the motion in issue is granted. Also, the record in this investigation is reopened and said Exh. B is admitted into evidence as ALJ Exh. 1.

XI. Validity ('178 Patent - Indefiniteness)

Respondents argued that claims 1 and 5 of the '178 patent each contain a limitation that requires a second gate electrode with surface portions of a polysilicon layer having grooves "being substantially flat" or "being substantially planar," respectively; and that if complainant's claim construction[59] is adopted, then said claims 1 and 5 are indefinite because one of ordinary skill has no way to determine the scope of these claim terms, and therefore whether the claims is infringed. (RBr at 236.) Respondents further argued that claim 5 is indefinite for an additional, independent reason since claim 5 includes terms that, as issued, were ambiguous because their

[59] As indicated, supra, complainant has proposed that the "substantially flat/planar" limitation in claims 1 and 5 of the '178 patent be construed to mean: "relatively flat as compared to the conventional structure described in the patent in which the polysilicon contained a recess above the separating groove. In other words, a layer that is substantially flat eliminates or substantially attenuates the topographical features of the underlying structures."

meaning was subject to reasonable debate by persons of ordinary skill in the art, even with resort to the specification; that even though complainant attempted to correct the claim language through a Certificate of Correction issued by the Patent Office, errors in the claim language remain; that after the correction, the last clause of claim 5 now reads "one of either a high melting point metal layer and a silicide layer of a high melting point metal"; that the language remains unclear, however, because one of ordinary skill cannot determine whether the clause should read "either . . . and" or "either . . . or"; and that since the patent specification provides no guidance as to which choice to make, claim 5 is invalid for indefiniteness even with the Certificate of Correction. (Id. at 237.)

Complainant argued that respondents improperly seek to require a construction of "substantially flat" that has absolute mathematical precision; that Federal Circuit has repeatedly held that when a word of degree such as "substantially" is used, an empirical standard providing mathematical precision is not required, but rather, only a reasonable degree of particularity and definiteness is necessary; and that the patent specification does provide a standard for determining the meaning of "substantially flat" and "substantially planar," and one of ordinary skill in the art would understand what is claimed when the claim is read in light of the specification. (CRBr at 162; CBr at 217.) Complainant further argued that the Patent Office made a mistake in transcribing the language of claim 5 that formed the basis for the Patent Office's Notice of Allowance into the text of claim 5 in the printed patent; that on November 22, 2005, complainant filed a Request for a Certificate of Correction with the Patent Office seeking to change "eight" to "either" and "melting" to "metal" in claim 5 of the '178 patent; that on March 7, 2006, the Patent Office issued a Certificate of Correction; that respondents cannot

prevail on their argument that claim 5 is indefinite because it uses "either . . . and" rather than "either . . . or"; and that while claim 5 would be more accurate grammatically if it used "or" instead of "and," the applicant's use of the conjunctive form instead of the disjunctive form does not render claim 5 indefinite. (CBr at 213-15.)

The staff argued that a person of ordinary skill in the art would have understood the conditions described in the '178 patent to constitute the method by which the inventor generated the flat surface and the form that the surface must take; that a person of ordinary skill would already have some understanding of "substantially flat" and "substantially planar"; and that the '178 patent adequately shows that the inventor was in possession of the "substantially flat" and "substantially planar" aspects of the invention. (SBr at 54.)

A decision on whether a claim is invalid under 35 U.S.C. § 112, requires, inter alia a determination of whether those skilled in the art would understand what is claimed when the claim is read in light of the specification. Orthokinetics, Inc. v. Safety Travel Chairs, Inc., 806 F.2d 1565, 1576 (Fed. Cir. 1986). Section 112, ¶ 2 provides that "[t]he specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention." A patentee's failure to do so renders the patent indefinite and invalid. See Default Proof Credit Card Sys., Inc. v. Home Depot U.S.A., Inc., 412 F.3d 1291, 1298 (Fed. Cir. 2005). A determination of claim indefiniteness is a legal conclusion that is drawn from the court's performance of its duty as the construer of patent claims. Id. citing Atmel Corp. v. Information Storage Devices, 198 F.3d 1374, 1378 (Fed. Cir. 1999).

The administrative law judge has found based on the claims, the written disclosures and

the figures of the specification, and the hearing testimonies of the experts that "substantially flat" and "substantially planar" is a "surface which substantially eliminates the topographical features of the underlying structure and thus does not require perfect flatness or anatomic flatness..." See supra. On this point, reference is made in particular to Figures 2B and 2C and the associated statements in the "Detailed Description of the Patented Invention" section of the '178 patent which describes the "substantially flat" limitation. See also Antoniadis Tr. at 451-53 and Bravman Tr. at 2338-39. Moreover, the Federal Circuit has held that when a word of degree such as "substantially" is used, an empirical standard providing mathematical precision is not required.[60]

Based on the foregoing, the administrative law judge finds that a person of ordinary skill would not find the claimed phrases "substantially flat" and "substantially planar", as recited in claims 1 and 5, indefinite.

Regarding respondents' argument that claim 5 is indefinite because it includes terms that, as issued, were ambiguous, it is a fact that the Patent Office made a mistake in transcribing claim 5 in the printed patent from the language of claim 9 in the application that formed the basis for the PTO's Notice of Allowance. (Compare JX-2 at TC-ITC-B000230 with JX-1, claim 5.) However, on November 22, 2005, Toshiba filed a Request for a Certificate of Correction with the

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[60] See Playtex Products, Inc. Procter & Gamble Co., 400 F.3d 907 (Fed. Cir. 2005) (holding "that the term 'substantial', a term of degree, should not be interpreted as having a strict numerical limitation."); Cordis Corp. v. Medtronic AVE, Inc., 339 F.3d 1352, 1361 (Fed. Cir. 2003) (refusing to impose a precise numeric constraint on the term "substantially uniform thickness"); Anchor Wall Sys. V. Rockwood Retaining Walls, Inc., 340 F.3d 1298 (Fed. Cir. 2003) (holding that "words of approximation, such as 'generally' and 'substantially' are descriptive terms commonly used in patent claims to avoid a strict numerical boundary to the specified parameter.").

Patent Office seeking to change "eight" to "either" and "melting" to "metal" in the last element of claim 5 of the '178 patent. (TFF2009 (undisputed).) On March 7, 2006, the Patent Office issued a Certificate of Correction. (TFF2009 (undisputed).) Thus, the typographical errors that originally appeared in claim 5 of the '178 patent have been corrected. (CX-747.) Moreover, respondents' expert Bravman agreed that the issued '178 patent contained typographical errors in claim 5 and further testified:

> Now, when I studied it [the '178 patent] carefully and compared the claim 5 to other claims in the text, I believe I was able to intuit correctly the mistakes that had been made. It's clear initially such as "eight" should be "either," and melting layer and silicide layer and how they're used. But when you study it, it becomes clear.

(Tr. at 2339-40 (emphasis added).)

As to whether the last clause of claim 5 still remains unclear because one of ordinary skill cannot determine whether the clause should read "either . . . and" or "either . . . or," the fourth clause of claim 5 recites in part: "a second gate electrode ... (2) one of either a high melting point metal layer and a silicide layer of a high melting point metal..." (JX-1 at 5:29-35 (emphasis added).) Hence, the fact that said claim language recites "one of"indicates that only one, and not both, of either the metal layer or the silicide layer is required.

Furthermore, the claims and the specification in the '178 patent repeatedly refer to a choice between using a high melting point metal or a silicide layer of a high melting point metal as the top layer in the control gate. (JX-1 at 1:13-16; 1:51-53; 1:66-2:13; 2:17-20; 2:38-41; 2:55-58; 2:66-3:1; 3:57-60; 4:41-42; 4:46-47; Antoniadis, Tr. at 2625.) For example, the Background of the Invention section of the '178 patent explains that the invention was necessitated by the fact that "[i]n recent years, in order to increase the operation speed of an

element, a refractory metal layer (a high melting point metal layer) or the silicide layer thereof is formed on the second polysilicon layer." (TFF 2024 (undisputed).) Also, the Summary of the Invention section of the '178 patent states:

> The present invention has been made in consideration of the above problem, and has as its object to flatten the refractory metal or the refractory metal silicide layer of the gate of the second level layer to avoid occurrence of cracks thereof and reduce an increase in resistance thereof.

(JX- at 2:17-21 (emphasis added).) Further, during cross examination, Bravman acknowledged that the patent repeatedly refers to a choice between using a metal layer or a silicide layer as the top layer in the control gate. (Bravman, Tr. at 2443.) Hence, the administrative law judge finds that one of ordinary skill in the art would understand that claim 5 requires a metal layer or a silicide layer, and thus would not find said claim 5 indefinite.

Based on the foregoing, the administrative law judge finds that respondents have not met their burden in establishing, by clear and convincing evidence, that claims 1 and 5 are indefinite.

XII. Validity ('178 Patent - Best Mode)

Respondents argued that asserted claims 1-5 are invalid because the inventor failed to disclose the best mode regarding the "insulating film." In support, it is argued that the claimed "insulating film" is limited to a single film structure;[61] that the use of an ONO structure is preferred over a single oxide film implementation because it provides for an increase in capacitive coupling between the gates of the memory structure; and that at the time the

[61] The administrative law judge however has found, supra, based on the claims, the written disclosures and the figures of the specification, the hearing testimony of respondents' expert, and published articles at the time of the invention of the '178 patent, that an "insulating film" as recited in asserted claims 1 and 5 may be multi-layered.

application that led to the '178 patent was filed, inventor Mori knew of and failed to disclose the better, preferred insulating ONO structure. (RBr at 239-40.)

Complainant argued that the "insulating film" claimed in the '178 patent is not limited to the single layer oxide mentioned in the specification, but rather would be understood by one skilled in the art to include either an oxide film or an ONO multilayered film;{

} that Mori backed that testimony up by identifying a number of specific reasons why ONO would not have been considered better than a single oxide for all applications in 1990; that Mori's testimony is corroborated by RX-943, the very document identified by respondents as establishing Mori's subjective beliefs just before he filed the application that led to the '178 patent in 1990; that there is no evidence that Mori concealed the benefits of ONO films during prosecution of the '178 patent; that the documents on which respondents rely include numerous published articles and patents authored by Mori between 1984 and 1990 in which ONO films were disclosed and their benefits described; that all of these documents were publicly available and known by 1990; and that the 1987 article was provided to the Patent Office by Mori during the prosecution of the '178 patent and is specifically cited as a prior art reference on the face of the patent. (CRBr at 164-66.)

The staff argued that in asserting that the '178 patent is invalid, respondents rely on an article in which the inventor states that inter-poly dielectrics such as ONO are preferable to poly-oxide film, suggesting that this was the inventor's best mode for the "insulating film" recited in claims 1-5. However, it is argued that since articles reciting similar benefits of ONO were supplied to the Patent Office by the applicant during the prosecution of the '178 patent, this mode

was publically available and, in any event, was not being concealed. The staff also argued that respondents have not provided evidence of an intent to conceal, which is an essential element of a best mode violation. (SBr at 56-57.)

Section 112, ¶1 provides that:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same, and shall set forth the best mode contemplated by the inventor of carrying out his invention.

The purpose of this "written description requirement" is to "ensure that the scope of the right to exclude, as set forth in the claims, does not overreach the scope of the inventor's contribution to the field of art as described in the patent specification." Reiffin v. Microsoft Corp., 214 F.3d 1342, 1345 (Fed. Cir. 2000). A finding of invalidity for failure to disclose the best mode requires proof, by clear and convincing evidence, that the inventor knew of and concealed a better mode of carrying out the invention than was set forth in the specification. Scripps Clinic & Research Found. v. Genentech, Inc., 927 F.2d 1565, 1578 (Fed. Cir. 1991). The best mode inquiry focuses "on the inventor's state of mind at the time he filed his application." Glaxo Inc. v. Novopharm Ltd., 52 F.3d 1042, 1050 (Fed. Cir. 1995).

Referring to respondents' argument that{

} For example, use of ONO in a

UV-EPROM[62] makes it difficult to erase the EPROM or can make it take a long time to erase the EPROM. (TFF 2048 (undisputed).) Mori's testimony is corroborated by RX-943, an article published in 1990 (for which Mori is listed as one of the authors), which states that "UV erase speed for EPROM cells with ONO inter-poly dielectric usually becomes slower than that with poly-oxide interpoly dielectric." (TFF 2056 (undisputed).) {

} Hence, the administrative law judge finds that the evidence establishes that inventor Mori, at the time of the filing of the application for the '178 patent, did not believe that an ONO film was superior. Thus, the administrative law judge finds that Mori had no intent to deceive. Moreover, it is undisputed that the 1987 article, which discloses the use of an ONO film as an interpoly dielectric (TFF 2083 (undisputed)) and lists Mori as one of its authors, was before the Examiner and made of record during the prosecution of the '178 patent.

Based on the foregoing, the administrative law judge finds that respondents have not established, by clear and convincing evidence, that the asserted claims 1-5 are invalid for failing to disclose the best mode.

XIII. Domestic Industry

There can be a violation of section 337 "only if an industry in the United States, relating to articles protected by the patent ... exists or is in the process of being established." 19 U.S.C. §

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[62] The '178 patent is applicable to both a UV-EPROM, an EPROM that is erased using ultraviolet (UV) light, as well as an EEPROM. (TFF 2047 (undisputed).)

1337(a)(2); see also Certain Methods of Making Carbonated Candy Products, Inv. No. 337-TA-292, USITC Pub. 2390, (Mar. 1990). The existence of a domestic industry is measured at the time the complaint is filed. See Bally/Midway Mfg. Co. v. U.S. Int'l Trade Comm'n, 714 F.2d 1117, 1121-22 (Fed. Cir. 1983).

The Commission has established a two-prong test for determining whether a complainant has satisfied the domestic industry requirement. The technical prong considers "whether the complainant is exploiting or practicing the patent in controversy," while the economic prong addresses "whether there is significant or substantial commercial exploitation." Certain Microsphere Adhesives, Process for Making Same, and Products Containing Same, Including Self-Stick Repositionable Notes, Inv. No. 337-TA-366, USITC Pub. 2949 (Jan. 1995). As complainant, Toshiba bears the burden of proving that it has satisfied both the technical prong and the economic prong.

Only the technical prong of domestic industry remains relevant in this investigation, as complainant has satisfied the economic prong of the domestic industry requirement through a summary determination motion granted by the administrative law judge. See Order No. 13 which issued on May 22, 2006.

A. The '969 And '449 Patents

Complainant asserted that the conventional designated representative domestic industry products{ } practice claims 1, 6 and 7 of the '969 patent and asserted that all designated representative domestic industry products{ } practice claim 4 of the '449

patent, and thus, satisfy the technical prong of the domestic industry requirement. (CBr at 79; RBr at 241-242; SBr at 44.)

1. Claim 1 of the '969 patent

With respect to claim 1 of the '969 patent, while the administrative law judge finds that complainant has established that its representative domestic industry products are "nonvolatile semiconductor memory devices" that have:

> a memory cell array comprising memory cells arranged in matrix form having rows and columns and row lines and column lines, each memory cell including cell transistors connected in series, and each of the cell transistors having a control gate, a floating gate, a channel region and an insulation film between the floating gate and the channel region, for electrically storing data by using charges stored in the floating gate, each memory cell having a first terminal and a second terminal, the first terminals of the memory cells in the same column being commonly connected to one of the column lines, the second terminals of the memory cells being connected to a reference potential, and the control gates of the cell transistors in the same row being commonly connected to one of the row lines, [memory cell array limitation][63]

"data latching means for storing data, connected to each of the column lines," and "column selection means for designating one of the columns of the memory cells in response to a column selection signal," he finds, as set forth infra, that complainant has not met its burden in establishing that its representative domestic industry products have:

> data programming means for selectively programming the cell transistors, wherein a selected cell transistor is programmed in accordance with data corresponding to the stored data of the data latching means, the cell transistor holds an injected state of electrons which are injected through the insulation film into the

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[63] Respondents argued that complainant adopted a new interpretation for the claim term "channel region" of the memory cell array limitation. (RBr at 132.) The administrative law judge rejects this argument. See Section VIII.A, supra.

floating gate by utilizing a tunnel effect by the data programming means when the stored data of the data latching means is a first logic level, and the cell transistor holds an emitted state of electrons which are emitted through the insulation film from the floating gate by utilizing a tunnel effect by the data programming means when the stored data of the data latching means is a second logic level,

and "row selection means for designating one of the rows of the memory cells in response to a row selection signal." Hence, he finds that complainant has not established that it satisfies the technical prong of domestic industry with respect to claim 1 of the '969 patent.

a. "data programming means for selectively programming the cell transistors, wherein a selected cell transistor is programmed in accordance with data corresponding to the stored data of the data latching means, the cell transistor holds an injected state of electrons which are injected through the insulation film into the floating gate by utilizing a tunnel effect by the data programming means when the stored data of the data latching means is a first logic level, and the cell transistor holds an emitted state of electrons which are emitted through the insulation film from the floating gate by utilizing a tunnel effect by the data programming means when the stored data of the data latching means is a second logic level"

Complainant argued that the "data programming means" element is met by the{ } transistors in its representative domestic industry{ } products. (CBr at 87; TFF 1435-1436, 1450-1451.) Complainant further argued that each of the identified{ } transistors in complainant's representative domestic industry products performs the function of selectively programming the cell transistors as is recited by the "data programming means" element of claim 1. (CBr at 87.) Complainant also argued that these{ } transistors allow the programming voltage to be selectively applied to the selected cell transistors. (TFF 1435-1436, 1450-1451.) Complainant in addition argued that each of the{ } transistors is the same as the corresponding structure that complainant identified (i.e., transistor 81 in Figure 18A of the '969 patent's specification). (CBr at 87.)

Complainant also argued that its representative domestic industry products{

} Complainant further argued that said products also selectively leave cell transistors in a state created by{ } where the "selectively" is determined in accordance with the data stored in{ } latches, (CBr at 87; TFF 1432-1439, 1441-1445, 1448-1451); and that its representative domestic industry products meet the claim limitations of the "wherein clause" in claim 1 of the '969 patent. (CBr at 88; TFF 1436, 1451.)

Respondents argued that under the proper construction of the term "programming," the '969 patent programs through a two-step process involving a blanket injection followed by selective emission. (RBr at 243; RPFF 2755.) However, respondents argued that complainant's representative domestic industry products program{

} (RBr at 243; RPFF 2756-2757.)

Respondents also argued that said products{

} not selective emission as required by the '969 patent. (RBr at 243; RPFF 2758.) Respondents also argued that said products' programming and erasing operations are separate and independent, as shown by the{ } function. (RBr at 243; RPFF 2762.) Respondents further argued that said products{

} (RBr at 244.)

Respondents argued that even if "programming" was interpreted otherwise, complainant's representative domestic industry products would still perform such function in at

least two substantially different ways:{

}

Respondents also argued that in said products,{

} In contrast, it is argued that the embodiments disclosed in the '969 patent can selectively change the state of the cell transistor through emission, where the selected cell transistor's control gate receives 0 V from the wordline, while the bitline/drain may receive either 0 V or a high Vpp voltage depending on Signal D1 in Circuit 10 of the '969 patent. (RBr at 244; RPFF 2770, 2773-2774.) Respondents further argued that said products{

}

Respondents argued that complainant's representative domestic industry products cannot maintain the strict relationship required by the "wherein clause" of the '969 patent's "data programming means" (i.e., when the latch is at a first logic level, the cell transistor must be in an injected state, and when the latch is at a second logic level, the cell transistor must be in an emitted state) because{

} (RBr at 245; RPFF 2793-2813.)

Respondents further argued that complainant's representative domestic industry products do not contain any structure identical or equivalent to the agreed-upon corresponding structures of the '969 patent (i.e., circuit 10, Figure 7, Figure 8 and Figure 9 of the '969 patent). (RBr at 245-246; RPFF 2814-2817, 2819-2823.) Respondents also argued that said products do not

contain any structure identical or equivalent to the group of structures that respondents identified are necessary to perform the function of the "data programming means" (i.e., latch 89, booster circuit 82 as disclosed in Figure 18B, wordlines, column lines, and selective transistors). (RBr at 246; RPFF 2826.)

The staff argued, that as to its analysis on whether the technical prong of the domestic industry requirement is satisfied, with respect to the '969 patent, is very similar to the staff's infringement analysis that it applied to respondents' accused products. (SBr at 44.) Thus, it argued that complainant's representative domestic industry products satisfy the technical prong of the domestic industry requirement as to the asserted claims of the '969 patent. (SBr at 44.)

As found supra, the entire circuit of Figure 18A of the '969 patent, not merely transistor 81 of Figure 18A, is the corresponding structure for the recited function of the "data programming means" limitation of claim 1 of the '969 patent. However, complainant solely relied on transistor 81 as the corresponding structure for the recited function of the "data programming means" limitation of claim 1 of the '969 patent. (RPFF 2006 (undisputed).) It is a fact that complainant's expert Reed, testified that he only relied on transistor 81 of Figure 18A of the '969 and '449 patents for his domestic industry opinion with respect to the "data programming means" limitation as indicated by Reed's testimony quoted in Section VIII.A, supra. Thus, the administrative law judge finds, with respect to whether complainant's representative domestic industry products contain identical structure to the corresponding structure of the "data programming means" of claim 1 of the '969 patent, that complainant relied only on whether complainant's products contain structure identical to transistor 81 of Figure 18A of the '969 patent. (See CBr at 86-89; TFF 1432, 1434-1436, 1441, 1450.) Hence, the

administrative law judge finds that complainant has not established, by a preponderance of the evidence, that any of its representative domestic industry products contain structure identical to the entire circuit of Figure 18A of the '969 patent.

Based on the foregoing, the administrative law judge finds that complainant has not established that its representative domestic industry products meet the claimed phrase in issue.

b. "row selection means for designating one of the rows of the memory cells in response to a row selection signal"

Complainant argued that each of its representative domestic industry{ } NAND flash products include row selection circuitry that performs the function of designating one of the rows of memory cells in response to a row selection signal. (CBr at 83.) Complainant further argued that in its representative domestic industry{ } products, the address signals,{ } are a "row selection signal" to which the row selection circuitry responds. (CBr at 83; TFF 1402, 1409.) Complainant further argued that the circuitry then decodes the address signals{ } to designate one of the rows of the memory cells. (CBr at 83.)

Respondents argued that the{ } circuits present in complainant's representative domestic industry products are quite different from row decoder 53 in the '969 patent because the patent only requires one decoder (row decoder 53) from which all the row lines (connected to memory cell transistors or selection gate transistors) branch out to run through every block of the disclosed memory cell array and row decoder 53 is a single decoder that can assert only two signals (0V or Vpp) on the selected block and all the blocks to the left of the memory cell array, whereas said representative domestic industry products use{

}

(RBr at 250; RPFF 2895-2904.)

The staff made the same argument as it did with reference to limitation a., supra. (SBr at 44.)

The issue is whether the circuitry identified by complainant in complainant's representative domestic industry products are equivalent to row decoder 53 of the '969 patent.

The administrative law judge finds that complainant's identified circuitry consists of {

}(Kanazawa, Tr. at 705-706; Quader, Tr. at 885-891; Reed, Tr. at 1227-1229; CDX-144-31 - CDX-141-36.) The administrative law judge further finds that said circuitry is not equivalent structure to row decoder 53 of the embodiment of the '969 patent that solely uses the circuit of Figure 10 because in said embodiment of the '969 patent, row decoder 53 applies a signal directly to the row lines, and does not require an additional signal to open any pass transistors, whereas in complainant's representative domestic industry products,{

} (JX-4 at 9:1-10; Kanazawa, Tr. at 705-706; Quader, Tr. at 885-891; Reed, Tr. at 1227-1229; CDX-144-31 - CDX-141-36.) Likewise, the administrative law judge finds that said circuitry is not equivalent structure to row decoder 53 of the embodiment that combines the circuit of Figure 10 and the circuit of Figure 17 because said embodiment requires a triple-indexed W signal which comprises a double-index W signal generated by row decoder 53 and a single-indexed Z signal

generated by column decoder 55[64] applied to a row line, whereas in complainant's representative domestic industry products,{

}He further finds that complainant has failed to show any combination at all of the{

} as called for in the specification of the '969 patent disclosing the corresponding structure of the "row selection means" of the '969 patent.

Based on the foregoing, the administrative law judge finds that complainant has not established that its representative domestic industry products have the limitation in issue.

2. Dependent Claims 6 and 7 of the '969 patent

Complainant argued that its representative domestic industry{ } flash memories include{

} (CBr at 89.) Complainant further argued that the gates of the select drain transistors for a row are connected to one of the row lines. (CBr at 89; TFF 1452-1453, 1455, 1461.) Complainant also argued that the select drain transistors, which receive the{ } signal as their respective control gates, are the same as or equivalent to the corresponding structure disclosed in the specification, specifically, the "ST" transistors in the Figure 1 of the '969 patent's specification. (CBr at 89; TFF 1452-1454, 1456-

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[64] Because the embodiment that comprises Figure 10 and Figure 17 of the '969 patent is an optional embodiment of claim 1 of the '969 patent, and because both the embodiment that solely uses the circuit of Figure 10 and the embodiment that uses Figures 10 and 17 of '969 patent use row decoder 53, the administrative law judge finds row decoder 53 to be the corresponding structure of the "row selection means" of claim 1 of the '969 patent instead of both row decoder 53 and column decoder 55. See Section VIII.A, supra.

1461.)

Complainant, in addition, argued that its representative domestic industry{ } NAND flash products include{ } connected between the second terminals of the memory cells and the reference potential. (CBr at 90; TFF 1462-1465.) Complainant further argued that{ } perform the recited function and are the same as or equivalent to the transistor 80 in Figure 16 of the '969 patent's specification. (CBr at 90; TFF 1463, 1471.) Complainant also argued that{

} (CBr at 90; TFF 1462-1463, 1467-1471.)

Respondents referenced their arguments in Section XIII.A.1, supra, with respect to the technical prong of the domestic industry requirement, to all asserted claims of the '969 patent. (See RBr at 241-252.)

The staff made the same argument as it did with respect to limitation a., supra. (SBr at 44.)

Claim 6 depends on claim 1[65] and recites a further limitation "selection transistors respectively inserted between the first terminals of the memory cells and the column lines, gates of the selection transistors being connected to one of the row lines." (JX-4 at 25:26-32.) Claim 7

[65] The language of claim 6 of the '969 patent reads: "A nonvolatile semiconductor memory device according to any one of claims 1 to 5..." (JX-4 at 26-27.) However, claim 6 is asserted by complainant only to the extent of its dependence on claim 1 of the '969 patent. (CBr at 89.)

depends on claim 1[66] and recites a further limitation "switching means respectively inserted between the second terminals of the memory cells and the reference potential, and controlled so as to be in an off state when the data programming means stores data." (JX-4 at 25:33-38.)

As seen, supra, the administrative law judge found that complainant has not established that the accused products satisfy the technical prong of domestic industry with respect to independent claim 1 of the '969 patent.

Based on the foregoing, the administrative law judge finds that complainant has not established that the accused products satisfy the technical prong of domestic industry with respect to dependent claims 6 and 7 of the '969 patent.

3. Claim 4 of the '449 patent

With respect to independent claim 4 of the '449 patent, while the administrative law judge finds that complainant has established, by a preponderance of the evidence, that its representative domestic industry products are "nonvolatile semiconductor memory devices" that have:

> a memory cell array comprising memory cells arranged in matrix form having first row lines, second row lines, and column lines, each memory cell including cell transistors and a selection transistor for selecting the memory cell, and each of the cell transistors having a control gate, a floating gate, a channel region and a tunnel insulation film including a portion having a thickness sufficient to cause a tunnel effect between the channel region and the floating gate, for electrically storing data by using charges stored in the floating gate, each memory cell having a first terminal and a second terminal, the first terminals of the memory cells in the

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[66] The language of claim 7 of the '969 patent reads: "A nonvolatile semiconductor memory device according to any one of claims 1 to 5..." (JX-4 at 33-34.) However, claim 7 is asserted by complainant only to the extent of its dependence on claim 1 of the '969 patent. (CBr at 90.)

> same column being commonly connected to one of the column lines, the second terminals of the memory cells being connected to a reference potential, the control gates of the cell transistors in the same row being commonly connected to one of the first row lines, and the gate of the selection transistor being connected to one of the second row lines, [memory cell array limitation][67]

and "first switching means connected between each of the second terminals of the memory cells and the reference potential, for disconnecting the memory cell from the reference potential when the data programming means stores data," he finds that complainant has not met its burden in establishing that its representative domestic industry products have

> "data programming means for selectively storing data into the cell transistors by one of injecting electrons through the tunnel insulation film into the floating gate, and emitting electrons through the tunnel insulation film from the floating gate,"

and

> "row selection means for applying a signal to one of the first row lines and applying a signal to one of the second row lines in response to a row selection signal, thereby selecting a cell transistor connected to the first row line and a selection transistor connected to one of the second row lines,"

and

> "second switching means for controlling whether or not the signal from the row selection means should be applied to the cell transistor in the memory cell, the second switching means being connected between the row selection means and the memory cell, wherein the second switching means is turned off when the memory cell which is connected to the second switching means is not selected."

Hence, he finds that complainant has not established that it satisfies the technical prong of

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[67] Respondents argued that complainant adopted a new interpretation for the claim term "channel region" of the memory cell array limitation. (RBr at 132.) The administrative law judge rejects this argument. See Section VIII.A, supra.

domestic industry with respect to claim 4 of the '449 patent.

a. "data programming means for selectively storing data into the cell transistors by one of injecting electrons through the tunnel insulation film into the floating gate, and emitting electrons through the tunnel insulation film from the floating gate"

Complainant argued that each of its representative domestic industry ABL, and non-ABL, NAND flash products includes either an{ } that performs the recited function of selectively storing data into the cell transistors. Complainant further argued that these{ } are the same as or equivalent to the corresponding structure disclosed in the specification, specifically the transistor 81 in Figure 18A of the '969 patent. (CBr at 93; TFF 1516-1533.) Complainant also argued that each of its representative domestic industry products{ } (CBr at 94; TFF 1517, 1523-1525.)[68]

Respondents' arguments for the '449 patent are substantially the same as their arguments for the '969 patent as to domestic industry except for the fact that respondents did not make any argument as to any "wherein" clause because said claim 4 of the '449 patent does not have the language of the "wherein" clause of claim 1 of the '969 patent.

The staff made the same argument as it did with limitation a., supra.

For the reasons stated supra, for the "data programming means" limitation of the '969 patent, the administrative law judge finds that complainant has not established that any of its representative domestic industry products contain structure identical to the entire circuit of Figure 18A of the '449 patent. Hence, the administrative law judge finds that complainant has not

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[68] Complainant's arguments for the '449 patent are substantially the same as its arguments for the '969 patent as to domestic industry except for the fact that complainant did not make any argument with respect to the "wherein" clause.

established that its representative domestic industry products meet the limitation of the claimed phrase in issue.

b. "row selection means for applying a signal to one of the first row lines and applying a signal to one of the second row lines in response to a row selection signal, thereby selecting a cell transistor connected to the first row line and a selection transistor connected to one of the second row lines"

Complainant argued that each of its representative domestic industry ABL, and non-ABL, NAND flash devices includes row selection circuitry that performs the recited function of applying a signal to one of the first row lines and applying a signal to one of the second row lines in response to a row selection signal. (CBr at 95.) Complainant also argued that each of the representative domestic industry ABL, and non-ABL, NAND flash devices includes row selection circuitry that is the same as or equivalent to the corresponding structure disclosed in the specification, specifically, row decoder 53, particularly as it is employed in Figure 17 of the '449 patent. (CBr at 95; TFF 1534-1547.) Complainant further argued that in the representative domestic industry flash products,{ } (CBr at 95.) Complainant further argued that said row selection circuitry{

} (CBr at 95.)

Respondents argued that the proper interpretation of the "row selection means" requires the use of the nonstandard decoder column decoder 55, either directly or indirectly through Figure 17 which calls for the triple index W signals generated in part by column decoder 55's Z signals. (RBr at 251; RPFF 2913-2918.) Respondents further argued that column decoder 55

does not exist in complainant's representative domestic industry products. (RBr at 251; RPFF 2919.) Respondents also argued that when considering either{

} circuits in complainant's representative domestic industry products, none of these circuits provide the necessary functionality of column decoder 55. (RBr at 251; RPFF 2920-2925.) Respondents in addition argued that the{ }transistor, and as a result, the signals on the global wordlines in complainant's representative domestic industry products cannot be applied to the wordlines so as to select a single wordline, as required by the '449 patent. (RBr at 251; RPFF 2927, 2928.)

The staff argued as it did with limitation a., supra. (SBr at 44.)

For the reasons stated supra, for the "row selection means" limitation of the '969 patent, the administrative law judge finds that complainant's identified circuitry in its representative domestic industry products is not identical structure to row decoder 53 and column decoder 55 of the embodiment of the '449 patent that uses the combination of the circuits of Figures 10 and 17.[69] Hence, the administrative law judge finds that complainant has not established that its representative domestic industry products meet the limitation of the claimed phrase in issue.

c. "second switching means for controlling whether or not the signal from the row selection

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[69] Because of the added limitation of the "second switching means" limitation in the '449 patent, as opposed to the '969 patent, either the embodiment that comprises the circuit of Figure 10 combined with the circuit of Figure 17, or the embodiment that comprises the circuit of Figure 10 combined with the circuit of Figure 17 combined with the circuit of Figure 18A, is required, and thus, the corresponding structure for the "row selection means" is both row decoder 53 and column decoder 55. See Section VII.B.1.b.ii, supra. However, the administrative law judge finds that complainant's identified circuitry in complainant's representative domestic industry products are not identical or equivalent to row decoder 53 and column decoder 55 for the reasons stated for the "row selection means" of the '969 patent. See Section XIII.A.1, supra.

means should be applied to the cell transistor in the memory cell, the second switching means being connected between the row selection means and the memory cell, wherein the second switching means is turned off when the memory cell which is connected to the second switching means is not selected"

Complainant argued that each of the representative domestic industry ABL, and non-ABL, NAND flash devices, include transistors that perform the function of controlling whether or not the signal from the row selection means should be applied to the cell transistor in the memory cell. (CBr at 98.) Complainant further argued that said transistors are the same as the corresponding structure disclosed in the specification, specifically, the QT transistors in Figure 17. (CBr at 98; TFF 1560, 1566-1568.) Complainant also argued that the "second switching means" element corresponds to the{

} in

complainant's representative domestic industry products. (CBr at 98; TFF 1560-1563, 1566-1568.) Complainant in addition argued that each of the 32 pass transistors is the same as the QT1 transistors shown in Figure 17 of the '449 patent and set forth in the specification. (CBr at 98.)

Respondents argued that while the '449 patent discloses that the QT transistors require W triple index signals as their inputs, there is no signal analogous to the W triple index signals in any of complainant's representative domestic industry products as required. (RBr at 252; RPFF 2932-2935.) Respondents further argued that without the W triple index signals, there is no structure performing the "second switching means" limitation in complainant's representative domestic industry products. (RBr at 252; RPFF 2936.)

The staff argued the same as it did with limitation a., supra.

As found in Section VIII.B, supra, the administrative law judge finds that the QT transistors (i.e., the second switching means) are turned on and off by the X1, X2, ... signal generated by row decoder 53. The administrative law judge further finds that the QT transistors interprets a combined W1n1, ... W121, W111 signal which is generated by the combination of signal Z2 to Zm generated by column decoder 55 and signal W11, W12, ... generated by row decoder 53. The administrative law judge also finds, based on the conductive state of the QT transistor, that the QT transistor either allows said combined signal to, or blocks said combined signal from, passing through to the corresponding cell transistor. While the administrative law judge finds that the pass transistor in complainant's representative domestic industry products is controlled by the block selection signal, and the pass transistor either allows the global wordline signal to, or blocks said global wordline signal from, passing through to the corresponding cell transistor, the administrative law judge finds that, because complainant's identified circuitry in its representative domestic industry products generates the global wordline signal in a substantially different way than how the row decoder generates the combined W1n1, ... W121, W111 signal, complainant's pass transistor likewise interprets the global wordline signal in a substantially different way than the way the QT transistor interprets the combined W1n1, ... W121, W111 signal.

Based on the foregoing, the administrative law judge finds that complainant has not established that its representative domestic industry products meet the claimed phrase in issue.

B. The '178 Patent

The parties agreed that the Toshiba representative domestic industry products for the '178 patent are the Toshiba/SanDisk{ } NAND flash device that is representative of all

Toshiba/SanDisk products manufactured at{ }nm design rules, and the Toshiba/SanDisk { } NAND flash device that is representative of all Toshiba/SanDisk products manufactured at{ } design rules. (TFF 1594 (undisputed).) At the hearing, complainant's expert Antoniadis provided testimony as to his opinion that the Toshiba/SanDisk { } practiced claims 1-5 of the '178 patent, and that this opinion and his associated analysis applied equally to the Toshiba/SanDisk{ } (Antoniadis, Tr. at 488-98.)

While the administrative law judge finds that complainant has established that its representative domestic industry products have the limitations "element forming regions" (claim 1), "first gate electrodes formed on said element forming regions, the first gate electrodes being separated from each other by a predetermined width" (claim 1), "an insulating film formed to define grooves having substantially the same width between said first gate electrodes" (claim 1), "first gate electrodes" (claim 5), "an insulating film formed on said first gate electrodes and defining grooves having a substantially same width between said first gate electrodes" (claim 5), and "a second gate electrode formed on said insulating film" (claim 5), he finds, as set forth infra, that complainant has not met its burden in establishing that its representative domestic industry products have the limitations "a field oxidation film of a predetermined pattern" (claim 1), "surfaces of those portions of said polysilicon layer which are above said grooves being substantially flat" (claim 1), "semiconductor element regions" (claim 5), and "a surface portion of said polysilicon layer at positions corresponding to said grooves being substantially planar" (claim 5). Hence, he finds that complainant has not established that its representative domestic industry products practice the asserted independent claims 1 and 5, and dependent claims 2-4.

1. Independent Claim 1

a. "a field oxidation film of a predetermined pattern"

Complainant, to meet its burden, argued that the each of Toshiba/SanDisk NAND flash products includes a field oxidation film in the form of what is commonly known as{ } (CBr at 184-5.)

Respondents argued that Toshiba/SanDisk NAND flash products do not have the limitation "a field oxidation film of a predetermined pattern" because they have{ } and not the claimed "field oxidation film." (RBr at 253.)

The staff argued that for the same reasons set forth in Section VIII.C.1, supra, with respect to respondents' accused products, complainant's{ }products do not practice claim 1 of the '178 patent. (SBr at 43.)

It is undisputed that the Toshiba/SanDisk NAND flash products have{ } (RPFF 3930 (undisputed).)

Moreover, complainant's expert Antoniadis agreed that the Toshiba/SanDisk NAND flash products do not practice the limitation "field oxidation film" if that term means a film formed by a thermal oxidation process. (RPFF 3933 (undisputed).) As seen in Section VII.C.1.a, supra, the administrative law judge has interpreted the claimed phrase "field oxidation film of a predetermined pattern" to mean "a field oxide layer formed by field oxidation, which is a process by which the field oxide is grown in the field region of the semiconductor substrate by the

thermal oxidation of the substrate."

Based on the foregoing, the administrative law judge finds that complainant has not established that its representative domestic industry products have the limitation "a field oxidation film of a predetermined pattern."

b. "surfaces of those portions of said polysilicon layer which are above said grooves being substantially flat"

Complainant, to meet its burden, argued that the surface of the polysilicon layer above the grooves in the Toshiba/SanDisk NAND flash devices is "substantially flat" within the meaning of the '178 patent. (CBr at 189.)

Respondents argued that the Toshiba/SanDisk NAND flash products do not have the limitation "surfaces of those portions of said polysilicon layer which are above said grooves being substantially flat" for many of the same reasons that the accused Hynix NAND flash do not infringe said limitation; and that the correct time to determine whether the surface of the control gate polysilicon film above the grooves is "substantially flat" is after deposition of the polysilicon film and before subsequent processing given that subsequent processing alters the surface of polysilicon film. (RBr at 258.)

The staff argued that complainant relies on finished product SEM and TEM photos to show the "substantially flat" limitation of claims 1; and that because the only time it is possible to evaluate the flatness is before any subsequent layer is deposited, complainant has not established the technical prong of the domestic industry requirement as to the asserted claim 1 of the '178 patent. (SBr at 43-44.)

As seen in Section VII.C.1.g, supra, the administrative law judge has interpreted the

claimed phrase "substantially flat" to mean a surface which substantially eliminates the topographical features of the underlying structure and thus does not require perfect flatness or anatomic flatness, and that the substantial flatness should be determined after the polysilicon layer is deposited but before any subsequent processing. The record is absent of any evidence showing in the representative domestic industry products what the surface of the polysilicon layer looks like after deposition of said polysilicon layer and before subsequent processing.

Based on the foregoing, the administrative law judge finds that complainant has not established that its representative domestic industry products have the limitation "surfaces of those portions of said polysilicon layer which are above said grooves being substantially flat."

2. Independent Claim 5

a. "a semiconductor substrate having semiconductor element regions"

Complainant, to meet its burden, argued that each of the Toshiba/SanDisk NAND flash devices includes "semiconductor element regions," which are active regions topped by a nonconductive film and separated by field regions on the semiconductor substrate. (CBr at 182.)

Respondents argued that Toshiba/SanDisk NAND flash products do not practice the limitation "a semiconductor substrate having semiconductor element regions" because said products do not have the claimed "field oxidation film" that is required to isolate each active region. (RBr at 261.)

As indicated with respect to claim 1, supra, it is undisputed that complainant's representative domestic industry products have{ } As seen, in Section VII.C.2.a, supra, the administrative law judge has interpreted the claimed phrase "semiconductor element regions" to mean active regions separated by isolation regions and topped by a non-conductive

film, where said isolation regions include 'field oxidation film" but said isolation regions are not formed by a trench isolation process such as STI. Hence, the administrative law judge finds that complainant has not established that its representative domestic industry products have the limitation "a semiconductor substrate having semiconductor element regions" of claim 5.

b. "a surface portion of said polysilicon layer at positions corresponding to said grooves being substantially planar"

Complainant, to meet its burden, argued that the polysilicon above the grooves in the Toshiba/SanDisk NAND flash devices is "substantially planar." (CBr at 184.)

Respondents argued that the Toshiba/SanDisk NAND flash products do not practice the limitation "a surface portion of said polysilicon layer at positions corresponding to said grooves being substantially planar" of claim 5 for the same reasons that said products do not practice the limitation "surfaces of those portions of said polysilicon layer which are above said grooves being substantially flat" of claim 1. (RBr at 263.)

The staff argued that complainant relies on finished product SEM and TEM photos to show the "substantially planar" limitation of claim 5; and that because the only time it is possible to evaluate the flatness is before any subsequent layer is deposited, the evidence relied on by complainant does not establish the technical prong of the domestic industry requirement as to claim 5 of the '178 patent. (SBr at 43-44.)

The record is devoid of any evidence showing what the surface of the polysilicon layer would look like in the representative domestic industry products after deposition of said polysilicon layer and before subsequent processing. Hence, the administrative law judge finds that complainant has not established that its representative domestic industry products have the

limitation "a surface portion of said polysilicon layer at positions corresponding to said grooves being substantially planar" of claim 5.

3. Dependent Claims 2-4

Complainant, to meet its burden, argued that the Toshiba/SanDisk NAND flash products practice each of the dependent claims 2, 3 and 4 of the '178 patent since said products meet the limitations of each of said claims. (CBr at 190-92.)

Respondents argued that the Toshiba/SanDisk NAND flash products do not practice each of the dependent claims 2, 3 and 4 for the same reasons they do not practice independent claim 1. (RBr at 260-61.)

The staff raised the same argument as it did with respect to the representative domestic industry products not meeting independent claim 1. (SBr at 43.)

As indicated, supra, claim 2 depends on claim 1; claim 3 depends on claim 1 or claim 2; and claim 4 depends on claim 1 or claim 2. As seen, supra, the administrative law judge found that complainant has not established that its representative domestic industry products practice the limitations of independent claim 1. Hence, the administrative law judge finds that complainant has not so established that its representative domestic industry products practice dependent claims 2, 3 and 4.

XIV. Remedy

Toshiba argued that the appropriate remedy is an exclusion order barring the direct importation of any Hynix accused products and at least the following downstream products containing said accused products, viz., USB flash drives; memory cards{

}flash-based MP3 players{

} personal digital assistants (PDAs); digital cameras and mobile telephones, to the extent that they are sold with separate, non-embedded, i.e. bundled, flash memory cards.[70] (CBr at 226, 228.)

Toshiba further argued that the evidence clearly demonstrates that Hynix maintains a sufficient inventory of infringing NAND flash chips in the United States to warrant the issuance of a cease and desist order;{

} (CBr at 254.)

Respondents argued, assuming a violation of section 337 is found, that factors militate in favor of not including downstream products in any limited exclusion order (RBr at 264.) However, it was argued that "[a]t the very least, the exclusion order should not apply to bundled products or to MP3 players." (RRTFF 2267 B.) In addition, it was argued that Toshiba has not demonstrated or put forth any evidence that respondents have a commercially significant U.S. inventory of the accused products. (RBr at 270.)

The staff argued that any limited exclusion order remedy should extend to respondents' downstream flash memory cards and USB flash drives but not to MP3 players and other

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[70] Referring to "bundled products," a bundled product is a stand-alone product that is often sold together with another product but can also be marketed and sold independently. Examples of bundled products in the flash memory market are cellular phones, digital cameras and PDAs, which are frequently sold with a removable flash memory card that is not embedded or hard-wired into the device. (TFF2738, 2740 (all undisputed).)

downstream products. (SBr at 60, 62.) The staff does not support entry of any cease and desist orders against respondents. (SBr at 63.)

A. Exclusion Order

Under Commission rules 210.36(a) and 210.42(a)(1)(ii), the administrative law judge is to consider evidence and argument on the issues of remedy and issue a recommended determination thereon. Under Section 337(d), 19 U.S.C. § 1337(d), the Commission may issue a limited exclusion order against a respondent that has been determined to be in violation of section 337. Such an order directs the U.S. Customs Service to exclude from entry into the United States articles that are covered by, and thus infringe, the intellectual property rights at issue. Certain Flash Memory Circuits and Products Containing Same, Inv. No. 337-TA-382, USITC Pub. No. 3046, Comm'n Op. at 26 (June 1997).

An exclusion order may cover not only articles specifically found to infringe, but also so-called downstream products, i.e., those products that incorporate the infringing articles as components, if the Commission decides that exclusion of downstream products is necessary to give a complainant complete and effective relief. On the other hand, including downstream products has the potential to expand the coverage of the exclusion order, thus increasing the risk of interfering with legitimate commerce. Hence, a balancing of factors may be appropriate.

To assist in any balancing, the Commission, in Certain Erasable Programmable Read-Only Memories Inv. No. 337-TA-276, Comm'n Op. at 124-26, 136 U.S.I.T.C., Pub. 2196 (May 1989) (EPROMs), aff'd sub nom Hyundai Electronics Industries Col., Ltd. v. U.S. Intern'l Trade Comm'n, 899 F.2d 1204 (Fed. Cir. 1990) (Hyundai Electronics), identified the following relevant factors for consideration:

1. the value of the infringing articles compared to the value of the downstream products in which they are incorporated;

2. the identity of the manufacturer of the downstream products, i.e., whether it can be determined that the downstream products are manufactured by a respondent or by a third party;

3. the incremental value to a complainant of the exclusion of downstream products;

4. the incremental detriment to a respondent from exclusion of such products;

5. the burdens imposed on third parties resulting from exclusion of downstream products;

6. the availability of alternative downstream products that do not contain the infringing articles;

7. the likelihood that the downstream products actually contain the infringing articles and are thereby subject to exclusion;

8. the opportunity for evasion of an exclusion order that does not include downstream products; and

9. the enforceability of an order by Customs.

The so-called "EPROMs factors"[71] are not meant to be exclusive of other considerations, as "the Commission may identify and take into account any other factors which it believes bear on the question of whether to extend remedial exclusion to downstream products, and if so to what specific products." EPROMs at 125-26. Thus, the Commission may exclude downstream

[71] The Federal Circuit in Hyundai Electronics described the EPROMs factors to be "a careful and common-sense balancing of the parties' conflicting interests as well as other relevant factors." 899 F.2d at 1209.

products even though not all of the factors weigh in favor of doing so. See EPROMs at 127.

The major manufacturers of NAND flash memory today include Samsung, which has a little greater than{ }percent of the market share, Toshiba, which has{ }percent of the market share,{ }and manufacturers like{ } which have smaller market shares but are very aggressive in ramping up production for this year and next year. (TFF 2220 (undisputed).) Toshiba manufactures the second largest share of the NAND flash memory market, manufacturing a{ } share. (TFF 2222 (undisputed).) Market information and Toshiba's internal analysts have determined that{ }

(TFF 2223 (undisputed).)

It is undisputed that{ } (TFF 2220, 2223; undisputed). Hence, assuming a violation is found, the administrative law judge recommends a limited exclusion order directed to Hynix or any or its affiliated companies, parents, subsidiaries, licensees, or other related business entities, or their successors or assigns.

It is further undisputed that Hynix NAND flash memory chips have no commercial purposes other than being incorporated into downstream products. (TFF2373 (undisputed).) In issue is what the downstream products are, if any, that should be included in any limited exclusion order. Complainant argued that the EPROMs factors weigh in favor of a limited exclusion order including certain downstream products, as argued supra. Respondents argued that any limited exclusion order should not relate to downstream products or if so, said downstream products included in said order should not encompass complainant's request. The staff argued

that any limited exclusion order should include certain downstream products.

EPROMs Factor 1 (value comparison of infringing articles and downstream products)

Hynix' NAND flash chips represent{ }

(TFF2540 (undisputed).) For example,{

} (TFF2558 (undisputed).) {

} (TFF 2561(undisputed).) As a result, the

NAND flash chips in higher capacity memory cards { }[73] represent an even

higher percentage of the cost of the card than the { } (Kaplan, Tr. at

1584-85; CX-821C, at 2.)

In USB flash drives, Hynix' NAND flash chips likewise represent {

} For example, the value of the Hynix chip

used in a{ } of the total manufacturing cost of the flash drive.

(TFF2612 (undisputed).) As with memory cards, costs other than the chip remain relatively

fixed. (Kaplan, Tr. at 1584.) Thus, as the memory capacity of the USB flash drives increases,

{ } NAND flash chip will represent an even higher percentage of

the total manufacturing cost of the product due to the increased cost of the Hynix NAND flash

chip. (Kaplan, Tr. at 1584-85; CX-821C, at 1 JX-65C, at 43-44.)

Hynix' NAND flash chips represent a comparable percentage of the total manufacturing

cost of MP3 players. As with memory cards and USB drives, it is well-known in the industry

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[72] The abbreviation 'MB" refers to megabytes.

[73] The abbreviation "GB" refers to gigabytes.

that NAND flash chips represent more than half of the value of MP3 players. {

} (TFF2667, 2668, 2670, 2671 (all undisputed).) The NAND flash chips represent more than{ } of the costs of flash-based MP3 players made by{ } (TFF2735; (undisputed).)

The administrative law judge finds no evidence in the record that{ } of any of the downstream products, as memory cards, USB drives or MP3 players.

Every Hynix' major customer testified that the NAND flash chip is integral to the operation of their flash-based products. (TFF2745 (undisputed).) { } (TFF2746; (undisputed).) Similarly,{ } (TFF2747 (undisputed).) {

} (TFF2749, 2751 (all undisputed).)

Based on the foregoing, the administrative law judge finds that EPROMs factor 1 weighs strongly in favor of an exclusion order including memory cards, USB drives, MP3 players, and other consumer products such as cellular phones, digital cameras and PDAs sold bundled with memory cards and containing Hynix NAND flash memory chips because the Hynix chip is the

most significant cost component and an integral component to the operation of flash-based downstream products. However, while NAND flash chips are utilized in other more expensive downstream products, such as oil refinery drilling bits, Global Position System devices and network routers, the relative value of the NAND flash memory in those products is not significant. (TFF2753 (undisputed).) Hence the administrative law judge finds that the record does not support including those products in an exclusion order.

EPROMs Factor 2 (identity of the manufacturer of the downstream products)

{

} In this investigation, however, there is no dispute as to the identity of the manufacturers of downstream products containing Hynix NAND flash chips, or as to the specific product model numbers incorporating such devices. All of Hynix customers have been identified in the record. (TFF2212 (undisputed).) Evidence was adduced at the hearing regarding those customers that manufacture the downstream products at issue overseas for importation into the U.S. market. For example,{

} (TFF2499, 2500; (undisputed).) {

} (TFF2274, 3040 (all undisputed).) Also, there is evidence regarding each company's specific product model numbers incorporating Hynix NAND flash chips that are imported to the United States (See EPROMs factor 4, infra). Hence, given the ability to identify the manufacturers of downstream products

containing the accused chips, the administrative law judge finds that EPROMs factor 2 weighs in favor of an exclusion order covering certain downstream products.

EPROMs Factor 3 (incremental value to complainant of the exclusion of certain downstream products)

{

}

(TFF3033-3044 (all undisputed).) Those chips have no commercial use other than incorporation into downstream products. For example,{

} (TFF2280-2281, TFF2759 (all undisputed).) Those downstream products are then sold around the world, including the United States. Thus, one of Hynix' top customers,{

} (Kaplan, Tr. at 1571-72, CX-843C and CDX-108C.) Moreover, the quantity of Hynix

NAND flash chips purchased by{

} (TFF3000-3001 (all undisputed).)

In addition, the volume of Hynix' sales to U.S. based companies{

} is dwarfed by the quantity of Hynix's total NAND flash sales worldwide

{ } (TFF3029-3030 (all undisputed).) While Hynix' foreign customers were not subject to discovery in this investigation, those foreign companies also import downstream products incorporating Hynix flash chips into the United States (TFF3029-3030 (all undisputed); Kaplan, Tr. at 1607.) For example, one of {

} (TFF3030 (undisputed).)

The administrative law judge, based on the foregoing, finds that the evidence demonstrates an incremental benefit that would accrue to Toshiba if certain downstream products were excluded from the United States. Accordingly, he finds that EPROMs factor 3 weighs in favor of a limited exclusion order, including certain downstream products.

EPROMs Factor 4 (incremental detriment to Hynix of the exclusion of certain downstream products)

Complainant's expert Kaplan acknowledged that if an exclusion order covering any downstream products is entered, it is possible that Hynix could lose foreign sales to downstream product manufacturers who chose to avoid implementing or maintaining tracking systems for accused products. (Tr. at 1654.) However, he also testified that there was no evidence in the

record to that effect. (Tr. at 1616.)

Hynix' major customers already utilize sophisticated tracking and marking procedures to identify and segregate downstream products based on the manufacturer of the incorporated flash memory chip. For example,{

} (TFF2911(undisputed).) In addition,

{

} (TFF2913-2915 (all undisputed).)

{

} (TFF2941 (undisputed)) and when products are imported in bulk form, there is always an indication on the packaging (in the bill of materials) or on the product itself that would indicate whether the products contain Hynix NAND flash chips. (TFF2943, TFF2945 (all undisputed).) {

} (TFF2946-2948 (all undisputed).) Hence, Hynix' major customer can identify their products containing Hynix' infringing chip going to the United States and not going to the United States.

Based on the foregoing, since the administrative law judge finds no evidence that Hynix would suffer any incremental detriment from an exclusion order encompassing certain downstream products, other than the exclusion of infringing chips from the United States market, the administrative law judge finds no evidence of any relevant detriment to Hynix. Accordingly,

EPROMs factor 4 weighs in favor of an exclusion order that includes certain downstream products.

EPROMs Factor 5 (burden on third parties)

{ }testified that there would be no burden if Hynix NAND flash chips were unavailable because they have prequalified other NAND flash chip suppliers and hence they are able to substitute those other supplier's products into the downstream products, and there would be no cost to make such substitution. (TFF 2867; (undisputed).) {

} (TFF 2868 (undisputed).) {

}

Hynix flash memory chip. (TFF 2869 (undisputed).) {

} (TFF 2870 (undisputed).)

The other manufacturers that supply or can supply NAND or NAND equivalent flash memory chips to Hynix' customers, in addition to Hynix, include Toshiba Corp., Samsung Electronics, Renesas Technology Corporation, Infineon Technologies, A.G., Micron Technology, Inc. and STMicroelectronics, N.V. (TFF 2878-2879 (all undisputed)); Kaplan, Tr. at 1618.) Moreover, since Hynix's customers have the ability to determine which of their end products use Hynix chips, (see supra), said customers can certify as to whether products shipped to the United

States contain or do not contain infringing chips.

Based on the foregoing, the administrative law judge finds that EPROMs factor 5 weighs in favor of issuing an exclusion order covering certain downstream products.

EPROMs Factor 6 (availability of alternative downstream products that do not contain the infringing articles)

Non-infringing NAND flash chips are available from many other suppliers in the market, and thus downstream products using non-infringing chips are also widely available. (TFF 2966-78, 2980-84 (undisputed).) {

} and many manufacturers of the relevant downstream products would not be impacted at all since they do not purchase any NAND flash chips from Hynix. (TFF 2980 (undisputed).) Moreover,{

} yet does not source any flash memory from Hynix. (TFF 2980 (undisputed).) Also, Toshiba sells memory cards and USB flash drives. (TFF 2981-2982 (all undisputed).)

Based on the foregoing, the administrative law judge finds that EPROMs factor 6 weighs in favor of an exclusion order including certain downstream products.

EPROMS Factor 7 (likelihood that downstream products actually contain the infringing articles)

As found in connection with EPROMs factor 3, there is evidence that millions of Hynix' NAND flash chips enter the U.S. market in downstream products. For example,{

} (TFF 2501, TFF2772 (all disputed)), {

} (TFF 2502 (undisputed).) This percentage is much higher, up to{ } for the specific product lines. (TFF 2508 (undisputed).) Also, according to the evidence provided by{

} (TFF 2330, TFF 2763 (all undisputed).)

In addition,{

} (TFF 3000 (undisputed)) and like other manufacturers,{

} (TFF 2936 (undisputed).) Accordingly, it is statistically evident that{

} (TFF 3004 (undisputed).)

Because the evidence establishes that millions of memory cards, USB flash drives, and MP3 players are imported into the United States every year containing Hynix NAND flash chips, the administrative law judge finds that EPROMs factor 7 weighs in favor of an exclusion order including certain downstream products.

EPROMs Factor 8 (evasion of an exclusion order that includes no downstream products)

It is undisputed that because Hynix' NAND flash chips have no commercial purpose other than incorporation into downstream products, it is not a question of whether Hynix' infringing chips will be incorporated into downstream products but rather only a question of

whether they are incorporated into downstream products and whether said products are imported into the United States. {

} (TFF 3031 (undisputed).) Given these facts, the administrative law judge finds that there is an extremely high likelihood that an exclusion order that only encompasses chips would be of no value. Hence, he finds that EPROMs factor 8 weighs in favor of an exclusion order encompassing certain downstream products.

EPROMs Factor 9 (enforceability of an order including certain downstream products by Customs)

Hynix' customers already have (or could readily obtain) the ability to track which downstream products contain Hynix NAND flash chips. See EPROMs factor 4 supra. Also, Customs can identify large quantities of downstream products containing Hynix NAND flash chips because most of Hynix' largest U.S. customers mark downstream products with identification numbers that indicate the manufacturer of the flash memory chip contained in that product. {

}(TFF 2943 (undisputed).) {

} (TFF 2945 (undisputed).) {

} (TFF 2955 (undisputed).) With that number, products containing Hynix NAND flash chips can be identified. Accordingly, customs officials would be able to identify whether the imported products contain a Hynix NAND flash device. (TFF 3108-3110 (all undisputed).) Moreover, a certification procedure is available to Customs.

Based on the foregoing, the administrative law judge finds that EPROMs factor 9 favor the issuance of a limited exclusion order covering certain downstream products.

Conclusion

Based on the foregoing, the administrative law judge recommends that any limited exclusion order also have certain downstream products that include memory cards, USB drives, MP3 players, and like consumer products such as cellular phones, digital cameras and PDAs sold bundled with memory cards containing Hynix' NAND flash chips. However, the excluded downstream products should not exclude more expensive downstream products such as oil refinery drilling bits, Global Position System devices and network routers containing Hynix NAND flash chips.

B. Cease And Desist Order

Under Section 337(f)(1), the Commission may issue a cease and desist order in addition to, or instead of, an exclusion order. 19 U.S.C. § 1337(f)(1). A factor to consider here is whether a respondent is maintaining a "commercially significant" inventory of infringing

products in the United States, the sale of which could undercut the effect of any exclusion order. See Certain Abrasive Products Made Using a Process for Powder Preforms, and Products Containing Same, Inv. No. 337-TA-449, USITC Pub. 3530, Comm'n Op. at 7 (August 2002). Complainant bears the burden of proving that a respondent has a commercially significant inventory of the accused products in the United States. Certain Integrated Repeaters, Switches, Transceivers, and Products Containing Same, Inv. No. 337-TA-435, USITC Publication No. 3547, Comm'n Op. at 27 (October 2002).

As of the beginning of February 2006,{

} (TFF 3119C (undisputed).)

Also, at least at the time TFF 3119A was submitted there were additional chips being imported into the United States.

Based on the foregoing, the administrative law judge recommends issuance of a cease and desist order covering Hynix' NAND flash chips, assuming the Commission determines that there is a violation.

XV. Bond

Pursuant to 19 U.S.C. § 1337(e)(1) and (j)(3) if an exclusion order issues, the Commission must determine the amount of the bond that respondents must post if they wish to continue entry of the accused articles from the date of the Commission's final order of violation of section 337 until expiration of the 60-day Presidential review period. In determining the amount of respondents' bond, the Commission should take into account the amount that would

offset any competitive advantage resulting from the unfair acts of respondents. See 19 C.F.R. § 210.50(a)(3); Certain Dynamic Random Access Memories, Components Thereof and Products Containing Same, Inv. No. 337-TA-242, Comm'n Op. (Sept. 21, 1987).

Complainant argued that the amount of bond should be set at 100% of the entered import value. It was argued that this bond amount has frequently been used by the Commission where direct price comparisons between the parties' respective products are not possible. (CBr at 254-5.)

Respondents argued that if they are found in violation of section 337, the Commission typically sets the bond at a "reasonable royalty," or a percentage of the value of the infringing goods sufficient to eliminate the price differential between the domestic and the imported infringing products; that here, the "reasonable royalty" is relatively easily obtainable given the numerous licensing agreements Toshiba has entered, and in view of the common practices in the semiconductor industry; and that accordingly, the appropriate bond for the accused NAND Flash circuits upon a finding of a violation of section 337 would be five (5) percent product revenues for the semiconductor parts. (RBr at 270-71.)

The staff argued that no evidence has been presented regarding the difference in price between Hynix' and Toshiba's flash memory chips and thus a bond set on a price differential is not appropriate; that a reasonable royalty of 5% should be applied; and that for downstream products, this bond amount should be applied to the value of the infringing chip, not to the products as a whole.

Respondents Hynix failed to introduce any evidence at the hearing that would support a five (5) percent royalty rate. Thus, Hynix did not introduce into any evidence any Toshiba

license agreements, did not introduce evidence of common practices in the semiconductor industry, and did not introduce any testimony from any economics expert. A bond at 100% of the entered import value has been frequently used by the Commission where direct price comparisons between the parties' respective products are not possible. See, e.g., Certain Microsphere Adhesives, Inv. No. 337-TA-366, 1996 WL 1056095, Comm Op. (Jan. 16, 1996). Thus, should a violation be found, the administrative law judge recommends a bond at 100% of the entered import value of the infringing chip.

XVI. Additional Findings OF Fact

A. Parties

1. Complainant Toshiba is a Japanese corporation. (Amended Complaint, ¶ 4.)

2. Toshiba is a leading provider of NAND Flash memory. (Amended Complaint, ¶ 5.)

3. Toshiba's principal place of business is located at 1-1 Shibaura 1-Chome, Minato-Ku Tokyo 105-8001 Japan. (Amended Complaint, ¶ 4.)

4. Toshiba has facilities worldwide, including offices in the United States, Japan, Canada, China, Great Britain, Korea, and Taiwan. (Amended Complaint, ¶ 4.)

5. Toshiba America Electronic Components, Incorporated (TAEC) is the division or subsidiary of Toshiba America, Incorporated, Toshiba Corporation. (Marlow, Tr. at 963-4.) TAEC is responsible for taking Toshiba's portfolio of products in intellectual property, both hardware and components and chips, as well as platforms or software, and aligning the portfolio with the needs and wants and desires of Toshiba's customer set. A fundamental job and task of TAEC is to secure design wins in products that are designed in the Americas, which can turn into revenue either in America or anywhere else in the world. (Marlow, Tr. at 965.)

6. TAEC sells and manufactures NAND products from NAND chips to finished cards to sub-assemblies of some card products and all the way through USB products. (Marlow, Tr. at 966.)

7. Respondent Hynix Semiconductor Inc. is a Korean corporation, with its principal place of business at San 136-1, Ami-Ri Bubal-eub Ichon-si Kyoungki-do, Korea 467-860. Hynix Semiconductor Inc. is a manufacturer of semiconductor products, including NAND Flash

memory devices, and is the parent corporation of respondent Hynix Semiconductor America Inc. (HSA). (Complaint, ¶ 10; Respondents' Response to Notice of Investigation, ¶ 10-11.)

8. HSA is a subsidiary of Hynix Semiconductor, Inc. HSA is one of eight subsidiaries globally in the capacity of sales and marketing. (Park, Tr. at 1505-07.)

B. Witnesses Appearing At Hearing

9. Complainant's Kayuhisa Kanazawa is currently the head of a NAND flash design group in Toshiba. Kanazawa's been involved in NAND flash memory technology with Toshiba for over 15 years. (Tr. at 661.)

10. Kanazawa co-authored the article entitled "A 120-mm2 64-Mb NAND Flash Memory Achieving 180 ns/Byte Effective Program Speed" published in IEEE Journal of Solid-State Circuits, Vol. 32, No. 5, May 1997. The NAND flash memory described in the article was jointly developed by Toshiba and Samsung each of which manufactured it in its own factories. (Tr. at 662-665; CX-353.)

11. Kanazawa has been personally involved in the joint design work between SanDisk and Toshiba. (Tr. at 693.)

12. Stephen Domain Marlow is the executive vice president of TAEC. (Tr. at 964.)

13. Marlow is knowledgeable of information relating to the NAND flash market. (Marlow, Tr. at 985.)

14. Marlow based his testimony on his 16 years of direct involvement with flash technologies, his management of TAEC's flash-related business groups, and his oversight of TAEC's memory business unit. (Tr. at 995.)

15. Jae Park is president of Hynix Semiconductor America in San Jose, California.

He has held that position since May 2004. (Tr. at 1505, 1506.)

16. Third party witness Khandker Quader received his M.S. degree in electrical engineering from Georgia Tech, and his Ph.D from U.C. Berkeley. (JX-56C, p. 13.)

17. Quader is the vice president of the NAND flash memory design organization at SanDisk. (Tr. at 852.)

18. Quader is responsible for NAND flash memory strategy, research, design and production of NAND flash memory for SanDisk, including the joint development between SanDisk and Toshiba. (Tr. at 852; JX-56C, p.13 and 14.)

CONCLUSIONS OF LAW

1. The Commission has in rem jurisdiction and in personam jurisdiction.

2. There has been an importation of accused NAND flash chips which are the subject of the alleged unfair trade allegations.

3. An industry does not exist in the United States that exploits the '178, '969 and '449 patents in issue, as required by subsection (a)(2) of section 337.

4. Respondents' accused products do not infringe the asserted claims of the '178, '969 and '449 patents.

5. The asserted claims of the '178, '969 and '449 patents are not invalid.

6. There is no violation of section 337.

7. Should the Commission determine that there is a violation, the record supports (1) issuance of a limited exclusion order directed to infringing NAND flash chips produced by respondents, as well as certain downstream products produced by third parties and containing said chips, (2) the issuance of a cease and desist order and (3) the imposition of a bond in the amount of 100 percent of the entered value of any infringing chips, during the Presidential review period.

ORDER

Based on the foregoing, and the record as a whole, it is the administrative law judge's Final Initial Determination that there is no violation of section 337 in the importation into the United States, sale for importation, and the sale within the United States after importation of certain flash memory devices and components thereof. It is also the administrative law judge's recommendation, should the Commission determine that there is a violation, that (1) a limited

exclusion order should issue directed to infringing NAND flash chips produced by respondents, as well as certain downstream products produced by third parties containing said chips, (2) a cease and desist order should issue, and (3) a bond of 100 percent of the entered value of any infringing NAND flash chips should be imposed during the Presidential review period.

The administrative law judge hereby CERTIFIES to the Commission his Final Initial and Recommended Determinations together with the record consisting of the exhibits admitted into evidence. He also CERTIFIES ALJ Exh. 1 (9/12/06 OG publication relating to terminal disclaimer of the '449 patent). The pleadings of the parties filed with the Secretary, and the transcript of the pre-hearing conference and the hearing, as well as other exhibits, are not certified, since they are already in the Commission's possession in accordance with Commission rules.

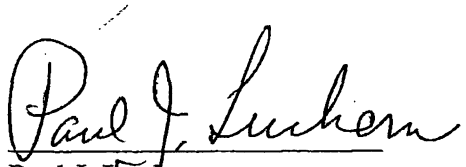
Further, it is ORDERED that:

1. In accordance with Commission rule 210.39, all material heretofore marked in camera because of business, financial and marketing data found by the administrative law judge to be cognizable as confidential business information under Commission rule 201.6(a), is to be given in camera treatment continuing after the date this investigation is terminated.

2. Counsel for the parties shall have in the hands of the administrative law judge those portions of the final initial and recommended determinations which contain bracketed confidential business information to be deleted from any public version of said determinations, no later than November 30, 2006. Any such bracketed version shall not be served via facsimile on the administrative law judge. If no such bracketed version is received from a party, it will mean that the party has no objection to removing the confidential status, in its entirety, from

these initial and recommended determinations.

3. The initial determination portion of the Final Initial and Recommended Determinations, issued pursuant to Commission rule 210.42(h)(2), shall become the determination of the Commission forty-five (45) days after the service thereof, unless the Commission, within that period shall have ordered its review of certain issues therein, or by order, has changed the effective date of the initial determination portion. The recommended determination portion, issued pursuant to Commission rule 210.42(a)(1)(ii), will be considered by the Commission in reaching a determination on remedy and bonding pursuant to Commission rule 210.50(a).



Paul J. Luckern
Administrative Law Judge

Issued: November 6, 2006

CERTAIN FLASH MEMORY DEVICES AND COMPONENTS THEREOF, AND PRODUCTS CONTAINING SUCH DEVICES AND COMPONENTS

Investigation No. 337-TA-552

CERTIFICATE OF SERVICE

I, Marilyn R. Abbott, hereby certify that the attached **Public Version Final Initial and Recommended Determinations** was served by hand upon Commission Investigative Attorney Bryan F. Moore, Esq. and upon the following parties via first class mail, and air mail where necessary, on April 26, 2007.

Marilyn R. Abbott

Marilyn R. Abbott, Secretary
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CERTAIN FLASH MEMORY DEVICES AND COMPONENTS THEREOF, AND PRODUCTS CONTAINING SUCH DEVICES AND COMPONENTS

Investigation No. 337-TA-552

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CERTAIN FLASH MEMORY DEVICES AND COMPONENTS THEREOF, AND PRODUCTS CONTAINING SUCH DEVICES AND COMPONENTS

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